24AA1025/24LC1025/24FC1025

1024-Kbit I²C Serial EEPROM

Device Selection Table

Part Number	Vcc Range	Maximum Clock Frequency	Temperature Ranges	Packages
24AA1025	1.7V-5.5V	400 kHz(1)	I	P, SN, SM
24LC1025	2.5V-5.5V	400 kHz(2)	I, E	P, SN, SM
24FC1025	1.8V-5.5V	1 MHz(3)	I	P, SN, SM

Note 1: 100 kHz for Vcc < 2.5V

2: 100 kHz for Vcc < 4.5V, E-temp

3: 400 kHz for Vcc < 2.5V

Features

- Low-Power CMOS Technology:
  - Read current 450 µA, maximum
  - Standby current 5 µA, maximum
- Two-Wire Serial Interface, I²C Compatible
- Cascadable up to Four Devices
- Schmitt Trigger Inputs for Noise Suppression
- Output Slope Control to Eliminate Ground Bounce
- 100 KHz and 400 KHz Clock Compatibility
- 1 MHz Clock for FC Versions
- Page Write Time: 5 ms, Maximum
- Self-Timed Erase/Write Cycle
- 128-Byte Page Write Buffer
- Hardware Write-Protect
- ESD Protection >4000V
- More than 1 Million Erase/Write Cycles
- Data Retention >200 Years
- Factory Programming Available
- RoHS Compliant
- Temperature Ranges:
  - Industrial (I): -40°C to +85°C
  - Extended (E): -40°C to +125°C
- Automotive AEC-Q100 Qualified

Packages

- 8-Lead PDIP, 8-Lead SOIC and 8-Lead SOIJ

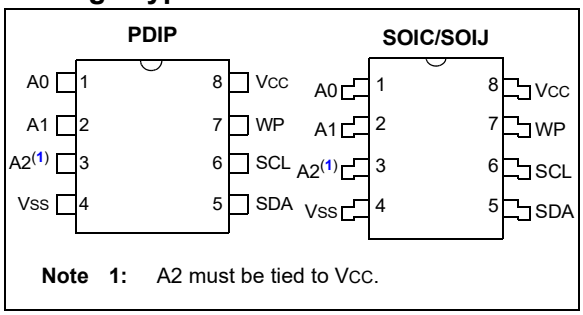
Description

The Microchip Technology Inc. 24XX1025(1) is a 1024-Kbit Electrically Erasable PROM (EEPROM). The device is organized as two block of 64K x 8 bit memory with a two-wire serial interface. Its low-voltage design permits operation down to 1.7V, with standby and active currents of 5 µA and 5 mA, respectively. The 24XX1025 also has a page write capability for up to 128 bytes of data.

This device is capable of both random and sequential reads. Reads may be sequential within address boundaries 0000h to FFFFh and 10000h to 1FFFFh. Functional address lines allow up to four devices on the same data bus. This allows for up to 4 Mbits total system EEPROM memory.

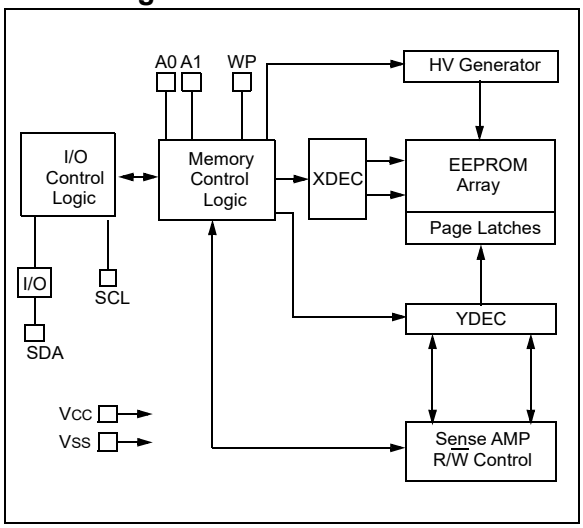
Note 1: 24XX1025 is used in this document as a generic part number for the 24AA1025/24LC1025/24FC1025 devices.

Package Type



Note 1: A2 must be tied to Vcc.

Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings(†)

VCC.....6.5V

All inputs and outputs w.r.t. VSS .....-0.6V to VCC+1.0V

Storage temperature .....-65°C to +150°C

Ambient temperature with power applied.....-40°C to +125°C

ESD protection on all pins .....≥ 4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			**Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): VCC = +2.5V to 5.5V TA = -40°C to +125°C**			
Param. No.	**Symbol**	**Characteristic**	**Minimum**	**Maximum**	**Units**	**Conditions**
		A1, A2, SCL, SDA and WP Pins:	—	—	—	
D1	VIH	High-level Input Voltage	0.7 VCC	—	V	
D2	VIL	Low-level Input Voltage	—	0.3 VCC	V	VCC ≥ 2.5V
			—	0.2 VCC	V	VCC < 2.5V
D3	VHYS	Hysteresis of Schmitt Trigger inputs (SDA, SCL pins)	0.05 VCC	—	V	VCC ≥ 2.5V **(Note 1)**
D4	VOL	Low-level Output Voltage	—	0.40	V	IOL = 3.0 mA @ VCC = 4.5V IOL = 2.1 mA @ VCC = 2.5V
D5	ILI	Input Leakage Current	—	±1	µA	VIN = VSS or VCC VIN = VSS or VCC
D6	ILO	Output Leakage Current	—	±1	µA	VOUT = VSS or VCC
D7	CIN, COUT	Pin Capacitance (all inputs/outputs)	—	10	pF	VCC = 5.0V **(Note 1)** TA = 25°C, FCLK = 1 MHz
D8	ICC Read	Operating Current	—	450	µA	VCC = 5.5V, SCL = 400 kHz
	ICC Write		—	5	mA	VCC = 5.5V
D9	ICCS	Standby current	—	5	µA	SCL, SDA, VCC = 5.5V A1, A2, WP = VSS

Note 1: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): Vcc = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): Vcc = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Minimum**	**Maximum**	**Units**	**Conditions**
1	FCLK	Clock Frequency	—	100	kHz	1.7V ≤ VCC ≤ 2.5V
			—	100	kHz	2.5V ≤ VCC ≤ 4.5V, E-temp
			—	400	kHz	2.5V ≤ VCC ≤ 5.5V
			—	400	kHz	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			—	1000	kHz	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
2	THIGH	Clock High Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
3	TLOW	Clock Low Time	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
4	TR	SDA and SCL Rise Time	—	1000	ns	1.7V ≤ VCC ≤ 2.5V **(Note 1)**
			—	1000	ns	2.5V ≤ VCC ≤ 4.5V, E-temp **(Note 1)**
			—	300	ns	2.5V ≤ VCC ≤ 5.5V **(Note 1)**
			—	300	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)** **(Note 1)**
			—	300	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)** **(Note 1)**
5	TF	SDA and SCL Fall Time	—	300	ns	All except 24FC1025 **(Note 1)**
			—	100	ns	1.8V ≤ VCC ≤ 5.5V **(24FC1025)** **(Note 1)**
6	THD:STA	Start Condition Hold Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
7	TSU:STA	Start Condition Setup Time	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
8	THD:DAT	Data Input Hold Time	0	—	ns	**Note 2**
9	TSU:DAT	Data Input Setup Time	250	—	ns	1.7V ≤ VCC ≤ 2.5V
			250	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			100	—	ns	2.5V ≤ VCC ≤ 5.5V
			100	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			100	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**

Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS (Continued)			Industrial (I): VCC = +1.7V to 5.5V TA = -40°C to +85°C Extended (E): Vcc = +2.5V to 5.5V TA = -40°C to +125°C			
Param. No.	**Symbol**	**Characteristic**	**Minimum**	**Maximum**	**Units**	**Conditions**
10	TSU:STO	Stop Condition Setup Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			250	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
11	TSU:WP	WP Setup Time	4000	—	ns	1.7V ≤ VCC ≤ 2.5V
			4000	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			600	—	ns	2.5V ≤ VCC ≤ 5.5V
			600	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			600	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
12	THD:WP	WP Hold Time	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
13	TAA	Output Valid From Clock	—	3500	ns	1.7V ≤ VCC ≤ 2.5V **(Note 2)**
			—	3500	ns	2.5V ≤ VCC ≤ 4.5V, E-temp **(Note 2)**
			—	900	ns	2.5V ≤ VCC ≤ 5.5V **(Note 2)**
			—	900	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)** **(Note 2)**
			—	400	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)** **(Note 2)**
14	TBUF	Bus Free Time: Time The Bus Must Be Free Before a New Transmission Can Start	4700	—	ns	1.7V ≤ VCC ≤ 2.5V
			4700	—	ns	2.5V ≤ VCC ≤ 4.5V, E-temp
			1300	—	ns	2.5V ≤ VCC ≤ 5.5V
			1300	—	ns	1.8V ≤ VCC ≤ 2.5V **(24FC1025)**
			500	—	ns	2.5V ≤ VCC ≤ 5.5V **(24FC1025)**
15	TSP	Input filter spike suppression (SDA and SCL pins)	—	50	ns	All except 24FC1025 **(Note 1 and Note 3)**
16	TWC	Write cycle time (byte or page)	—	5	ms	
17		Endurance	1,000,000	—	cycles	+25°C, 5.5V, Page Mode **(Note 4)**

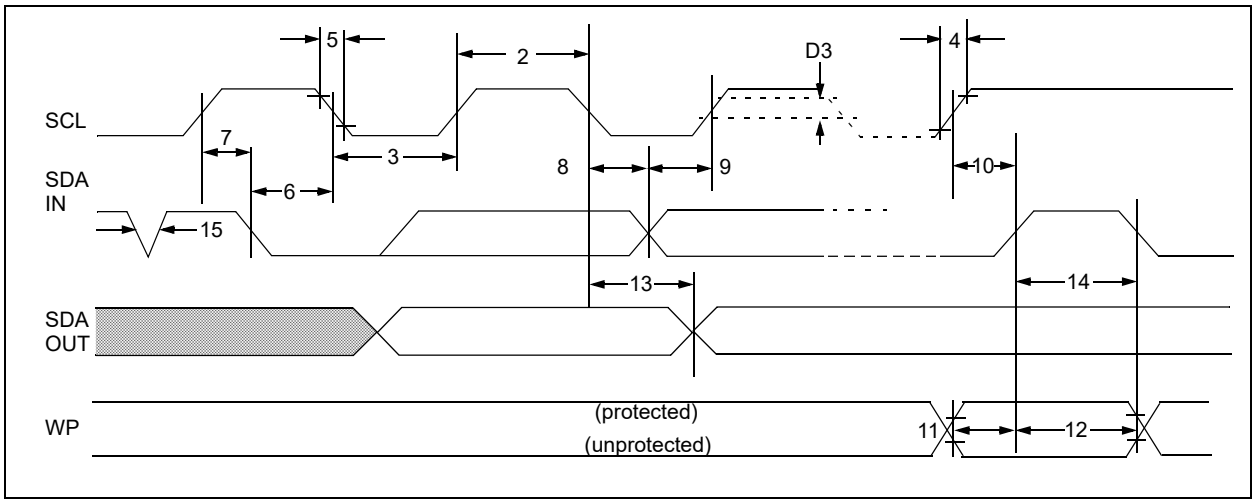
Note 1: Not 100% tested. CB = total capacitance of one bus line in pF.

2: As a transmitter, the device must provide an internal minimum delay time to bridge the undefined region (minimum 300 ns) of the falling edge of SCL to avoid unintended generation of Start or Stop conditions.

3: The combined TSP and VHYS specifications are due to new Schmitt Trigger inputs which provide improved noise spike suppression. This eliminates the need for a TI specification for standard operation.

4: This parameter is not tested but established by characterization.

FIGURE 1-1: BUS TIMING DATA



2.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Name	PDIP	SOIJ	SOIC	Function
A0	1	1	1	User Configurable Chip Select
A1	2	2	2	User Configurable Chip Select
A2	3	3	3	Non-Configurable Chip Select. This pin must be hard-wired to logical '1' state (VCC). Operation will be undefined with this pin left floating or held to logical '0' (VSS).
VSS	4	4	4	Ground
SDA	5	5	5	Serial Address/Data I/O
SCL	6	6	6	Serial Clock
WP	7	7	7	Write-Protect Input
VCC	8	8	8	Power Supply

2.1 A0, A1 Chip Address Inputs

The A0 and A1 inputs are used by the 24XX1025 for multiple device operations. The levels on these inputs are compared with the corresponding bits in the client address. The chip is selected if the comparison is true.

Up to four devices may be connected to the same bus by using different Chip Select bit combinations. In most applications, the chip address inputs A0 and A1 are hard-wired to logic '0' or logic '1'. For applications in which these pins are controlled by a microcontroller or other programmable device, the chip address pins must be driven to logic '0' or logic '1' before normal device operation can proceed.

2.2 A2 Chip Address Input

The A2 input is non-configurable Chip Select. This pin must be tied to VCC in order for this device to operate. If left floating or tied to VSS, device operation will be undefined.

2.3 Serial Address/Data Input/Output (SDA)

This is a bidirectional pin used to transfer addresses and data into and data out of the device. It is an open-drain terminal, therefore, the SDA bus requires a pull-up resistor to VCC (typical 10 kΩ for 100 kHz, 2 kΩ for 400 kHz and 1 MHz).

For normal data transfer SDA is allowed to change only during SCL low. Changes during SCL high are reserved for indicating the Start and Stop conditions.

2.4 Serial Clock (SCL)

This input is used to synchronize the data transfer from and to the device.

2.5 Write-Protect (WP)

This pin must be connected to either VSS or VCC.

If tied to VSS, normal memory operation is enabled (read/write the entire memory 00000h to 1FFFFh).

If tied to VCC, write operations are inhibited. The entire memory will be write-protected. Read operations are not affected.

3.0 FUNCTIONAL DESCRIPTION

The 24XX1025 supports a bidirectional two-wire bus and data transmission protocol. A device that sends data onto the bus is defined as a transmitter and a device receiving data as a receiver. The bus must be controlled by a host device which generates the Serial Clock (SCL), controls the bus access, and generates the Start and Stop conditions while the 24XX1025 works as a client. Both host and client can operate as a transmitter or receiver, but the host device determines which mode is activated.

4.0 BUS CHARACTERISTICS

The following **bus protocol** has been defined:

- Data transfer may be initiated only when the bus is not busy.
- During data transfer, the data line must remain stable whenever the clock line is high. Changes in the data line while the clock line is high will be interpreted as a Start or Stop condition.

Accordingly, the following bus conditions have been defined (Figure 4-1).

4.1 Bus Not Busy (A)

Both data and clock lines remain high.

4.2 Start Data Transfer (B)

A high-to-low transition of the SDA line while the clock (SCL) is high determines a Start condition. All commands must be preceded by a Start condition.

4.3 Stop Data Transfer (C)

A low-to-high transition of the SDA line while the clock (SCL) is high determines a Stop condition. All operations must end with a Stop condition.

4.4 Data Valid (D)

The state of the data line represents valid data when, after a Start condition, the data line is stable for the duration of the high period of the clock signal.

The data on the line must be changed during the low period of the clock signal. There is one bit of data per clock pulse.

Each data transfer is initiated with a Start condition and terminated with a Stop condition. The number of the data bytes transferred between the Start and Stop conditions is determined by the host device and is, theoretically, unlimited (although only the last 128 will be stored when doing a write operation). When an overwrite does occur, it will replace data in a First-In First-Out (FIFO) principle.

4.5 Acknowledge

Each receiving device, when addressed, is obliged to generate an Acknowledge after the reception of each byte. The host device must generate an extra clock pulse which is associated with this Acknowledge bit.

Note:	The 24XX1025 does not generate any Acknowledge bits if an internal programming cycle is in progress.

A device that acknowledges must pull-down the SDA line during the Acknowledge clock pulse in such a way that the SDA line is stable-low during the high period of the Acknowledge-related clock pulse. Moreover, setup and hold times must be taken into account. During reads, a host must signal an end of data to the client by NOT generating an Acknowledge bit on the last byte that has been clocked out of the client. In this case, the client (24XX1025) will leave the data line high to enable the host to generate the Stop condition.

FIGURE 4-1: DATA TRANSFER SEQUENCE ON THE SERIAL BUS

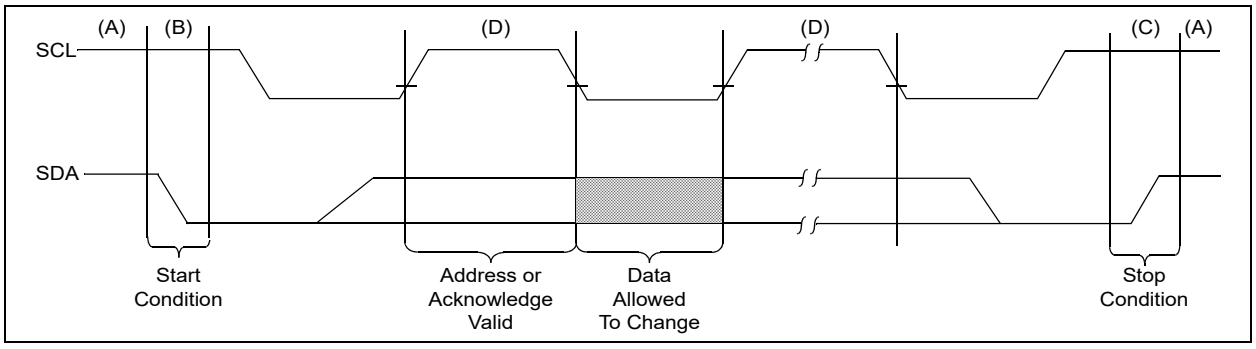
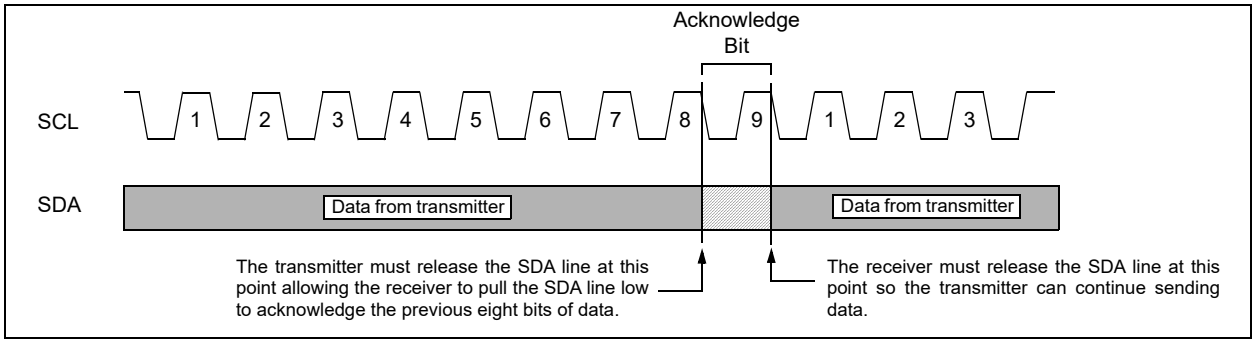


FIGURE 4-2: ACKNOWLEDGE TIMING



5.0 DEVICE ADDRESSING

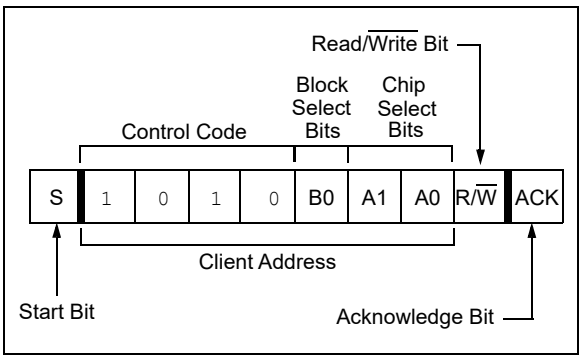
A control byte is the first byte received following the Start condition from the host device (Figure 5-1). The control byte consists of a 4-bit control code; for the 24XX1025, this is set as '1010' binary for read and write operations. The next bit of the control byte is the block select bit (B0). This bit acts as the A16 address bit for accessing the entire array. The next two bits of the control byte are the Chip Select bits (A1, A0). The Chip Select bits allow the use of up to four 24XX1025 devices on the same bus and are used to select which device is accessed. The Chip Select bits in the control byte must correspond to the logic levels on the corresponding A1 and A0 pins for the device to respond. These bits are in effect the two Most Significant bits (MSb) of the word address. The combination of the 4-bit control code and the next three bits are called the client address.

The last bit of the control byte is the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit and it defines the operation to be performed. When set to a '1', a read operation is selected. When set to a '0', a write operation is selected. The next two bytes received define the address of the first data byte (Figure 5-2). The upper address bits are transferred first, followed by the Least Significant bits (LSb).

Following the Start condition, the 24XX1025 monitors the SDA bus checking the device type identifier being transmitted. Upon receiving a valid client address and the R/$\overline{\text{W}}$ bit, the client device outputs an Acknowledge signal on the SDA line. Depending on the state of the R/$\overline{\text{W}}$ bit, the 24XX1025 will select a read or write operation.

This device has an internal addressing boundary limitation that is divided into two segments of 512-Kbits. Block select bit 'B0' to control access to each segment.

FIGURE 5-1: CONTROL BYTE FORMAT



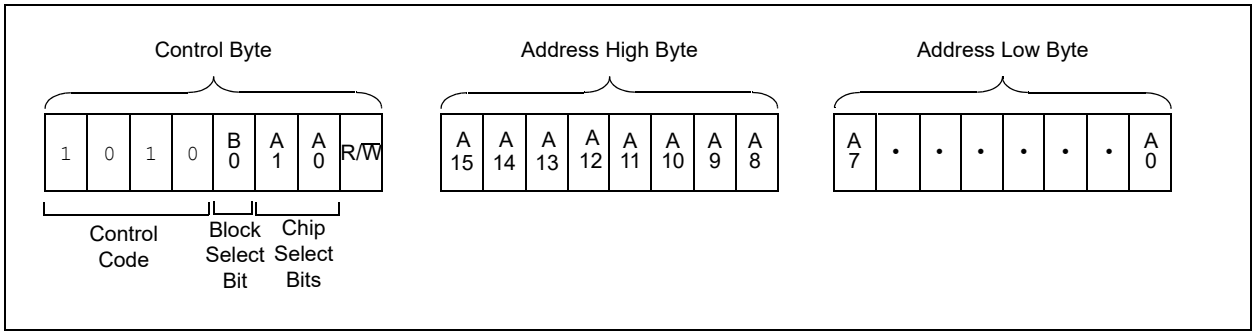
5.1 Contiguous Addressing Across Multiple Devices

The Chip Select bits A1 and A0 can be used to expand the contiguous address space for up to 4 Mbit by adding up to four 24XX1025's on the same bus. In this case, software can use A0 of the control byte as address bit A17 and A1 as address bit A18. It is not possible to sequentially read across device boundaries.

Each device has internal addressing boundary limitations. This divides each part into two segments of 512-Kbits. The block select bit 'B0' controls access to each "half".

Sequential read operations are limited to 512-Kbit blocks. To read through four devices on the same bus, eight random Read commands must be given.

FIGURE 5-2: ADDRESS SEQUENCE BIT ASSIGNMENTS



6.0 WRITE OPERATIONS

6.1 Byte Write

Following the Start condition from the host, the control code (four bits), the block select (one bit), the Chip Select (two bits), and the R/$\overline{W}$ bit (which is a logic low) are clocked onto the bus by the host transmitter. This indicates to the addressed client receiver that the address high byte will follow after it has generated an Acknowledge bit during the ninth clock cycle. Therefore, the next byte transmitted by the host is the high-order byte of the word address and will be written into the Address Pointer of the 24XX1025. The next byte is the Least Significant Address Byte. After receiving another Acknowledge signal from the 24XX1025, the host device will transmit the data word to be written into the addressed memory location. The 24XX1025 acknowledges again and the host generates a Stop condition. This initiates the internal write cycle and during this time, the 24XX1025 will not generate Acknowledge signals as long as the control byte being polled matches the control byte that was used to initiate the write (Figure 6-1). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command. After a byte Write command, the internal Address Pointer will point to the address location following the one that was just written.

Note:	When doing a write of less than 128 bytes the data in the rest of the page are refreshed along with the data bytes being written. This will force the entire page to endure a write cycle, for this reason endurance is specified per page.

6.2 Page Write

The write control byte, word address and the first data byte are transmitted to the 24XX1025 in the same way as in a byte write. But instead of generating a Stop condition, the host transmits up to 127 additional bytes, which are temporarily stored in the on-chip page buffer and will be written into memory after the host has transmitted a Stop condition. After receipt of each word, the seven lower Address Pointer bits, which form the byte counter, are internally incremented by one. The higher-order 9 bits of the word address remain constant. If the host should transmit more than 128 bytes prior to generating the Stop condition, the Address Pointer will roll over and the previously received data will be overwritten. As with the byte write operation, once the Stop condition is received, an internal write cycle will begin (Figure 6-2). If an attempt is made to write to the array with the WP pin held high, the device will acknowledge the command, but no write cycle will occur, no data will be written and the device will immediately accept a new command.

Note:	Page write operations are limited to writing bytes within a single physical page, regardless of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and end at addresses that are integer multiples of page size – 1. If a page write command attempts to write across a physical page boundary, the result is that the data wrap around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

6.3 Write Protection

The WP pin allows the user to write-protect the entire array (00000-1FFFF) when the pin is tied to VCC. If tied to VSS the write protection is disabled. The WP pin is sampled at the Stop bit for every Write command (Figure 1-1). Toggling the WP pin after the Stop bit will have no effect on the execution of the write cycle.

FIGURE 6-1: BYTE WRITE

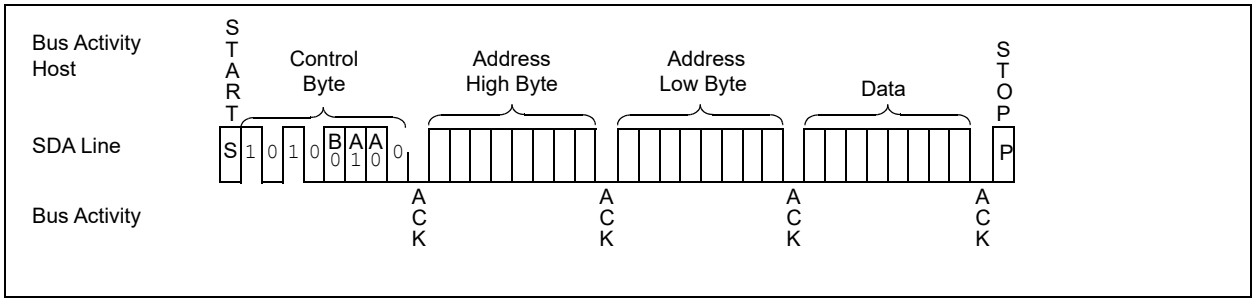
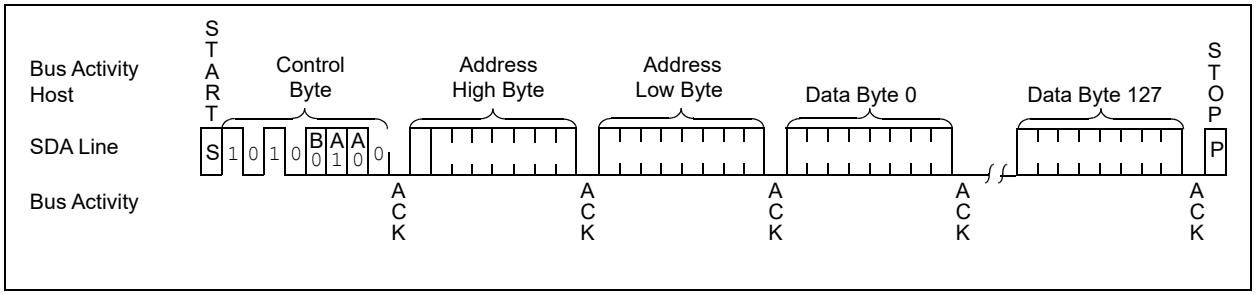


FIGURE 6-2: PAGE WRITE

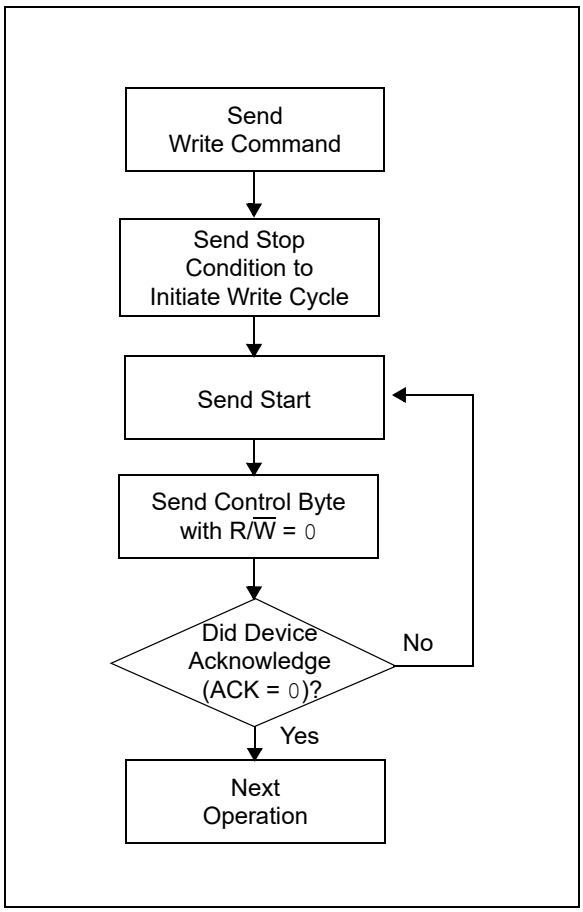


7.0 ACKNOWLEDGE POLLING

Since the device will not acknowledge during a write cycle, this can be used to determine when the cycle is complete. (This feature can be used to maximize bus throughput.) Once the Stop condition for a write command has been issued from the host, the device initiates the internally timed write cycle. ACK polling can be initiated immediately. This involves the host sending a Start condition, followed by the control byte for a write command (R/$\overline{W}$ = 0). If the device is still busy with the write cycle, then no ACK will be returned. If no ACK is returned, then the Start bit and control byte must be resent. If the cycle is complete, then the device will return the ACK and the host can then proceed with the next read or write operation. See Figure 7-1 for flow diagram.

Note:	Care must be taken when polling the 24XX1025. The control byte that was used to initiate the write needs to match the control byte used for polling.

FIGURE 7-1: ACKNOWLEDGE POLLING FLOW



8.0 READ OPERATION

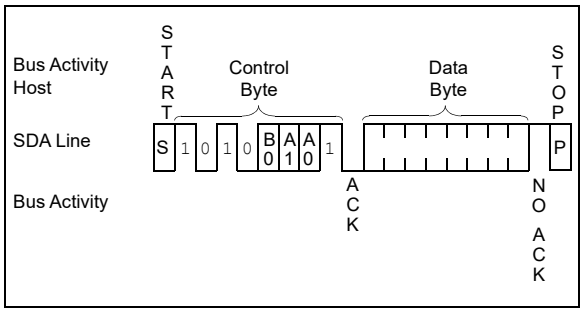
Read operations are initiated in the same way as write operations with the exception that the R/$\overline{W}$ bit of the control byte is set to one. There are three basic types of read operations: current address read, random read and sequential read.

8.1 Current Address Read

The 24XX1025 contains an Address Pointer that maintains the address of the last word accessed, internally incremented by one. Therefore, if the previous read access was to address n (n is any legal address), the next current address read operation would access data from address n + 1.

Upon receipt of the control byte with R/$\overline{W}$ bit set to one, the 24XX1025 issues an Acknowledge and transmits the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition and the 24XX1025 discontinues transmission (Figure 8-1).

FIGURE 8-1: CURRENT ADDRESS READ



8.2 Random Read

Random read operations allow the host to access any memory location in a random manner. To perform this type of read operation, first the word address must be set. This is done by sending the word address to the 24XX1025 as part of a write operation (R/$\overline{W}$ bit set to 0). After the word address is sent, the host generates a Start condition following the Acknowledge. This terminates the write operation, but not before the internal Address Pointer is set. Then, the host issues the control byte again, but with the R/$\overline{W}$ bit set to a one. The 24XX1025 will then issue an Acknowledge and transmit the 8-bit data word. The host will not acknowledge the transfer, but does generate a Stop condition which causes the 24XX1025 to discontinue transmission (Figure 8-2). After a random Read command, the internal Address Pointer will point to the address location following the one that was just read.

8.3 Sequential Read

Sequential reads are initiated in the same way as a random read except that after the 24XX1025 transmits the first data byte, the host issues an Acknowledge as opposed to the Stop condition used in a random read. This Acknowledge directs the 24XX1025 to transmit the next sequentially addressed 8-bit word (Figure 8-3). Following the final byte transmitted to the host, the host will NOT generate an Acknowledge, but will generate a Stop condition.

To provide sequential reads, the 24XX1025 contains an internal Address Pointer which is incremented by one at the completion of each operation. This Address Pointer allows half the memory contents to be serially read during one operation. Sequential read address boundaries are 00000h to 0FFFFh and 10000h to 1FFFFh. The internal Address Pointer will automatically roll over from address 0FFFFh to address 00000h if the host acknowledges the byte received from the array address 0FFFFh. The internal Address Pointer will automatically roll over from address 1FFFFh to address 10000h if the host acknowledges the byte received from the array address 1FFFFh.

FIGURE 8-2: RANDOM READ

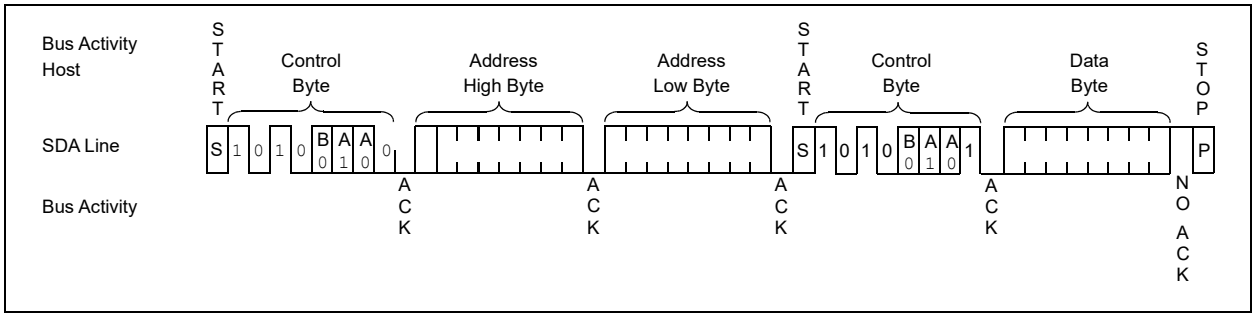
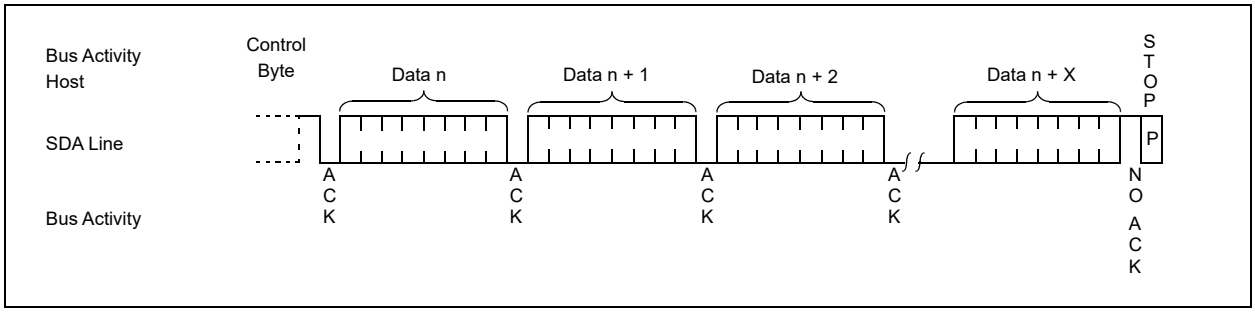


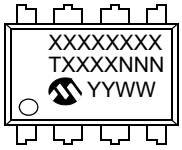
FIGURE 8-3: SEQUENTIAL READ



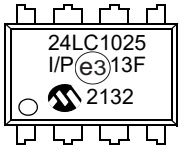
9.0 PACKAGING INFORMATION

9.1 Package Marking Information

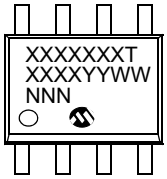
8-Lead PDIP (300 mil)



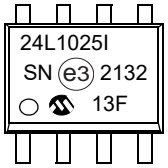
Example



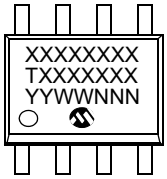
8-Lead SOIC (3.90 mm)



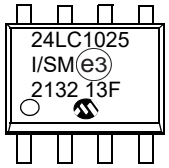
Example



8-Lead SOIJ (5.28 mm)



Example



Part Number	1st Line Marking		
	PDIP	SOIJ	SOIC
24AA1025	24AA1025	24AA1025	24A1025T(1)
24LC1025	24LC1025	24LC1025	24L1025T(1)
24FC1025	24FC1025	24FC1025	24F1025T(1)

Note 1: T = Temperature grade (I, E)

Legend:	XX...X	Part number or part number code
	T	Temperature (I, E)
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code (2 characters for small packages)
		JEDEC® designator for Matte Tin (Sn)

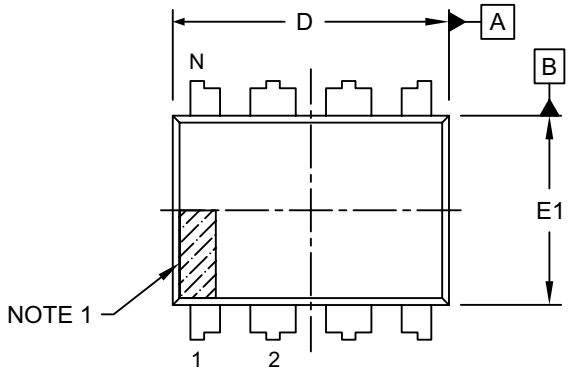
***** Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

Note: For very small packages with no room for the JEDEC® designator (e3), the marking will only appear on the outer carton or reel label.

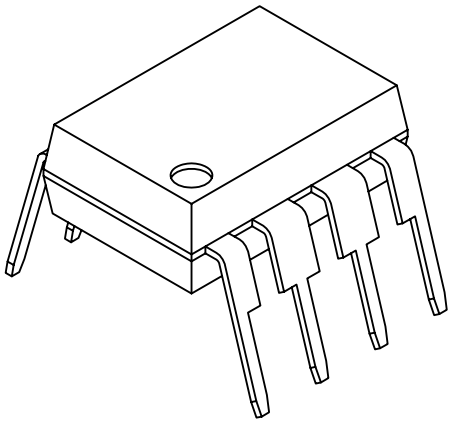
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

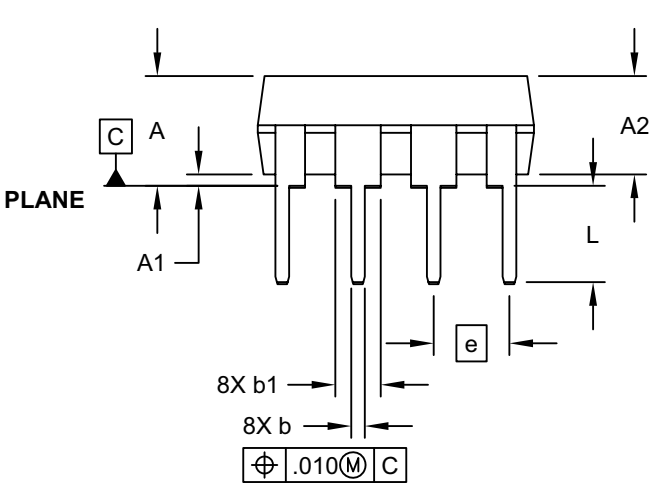
8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

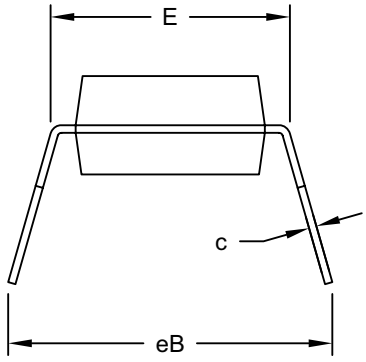


TOP VIEW





SIDE VIEW

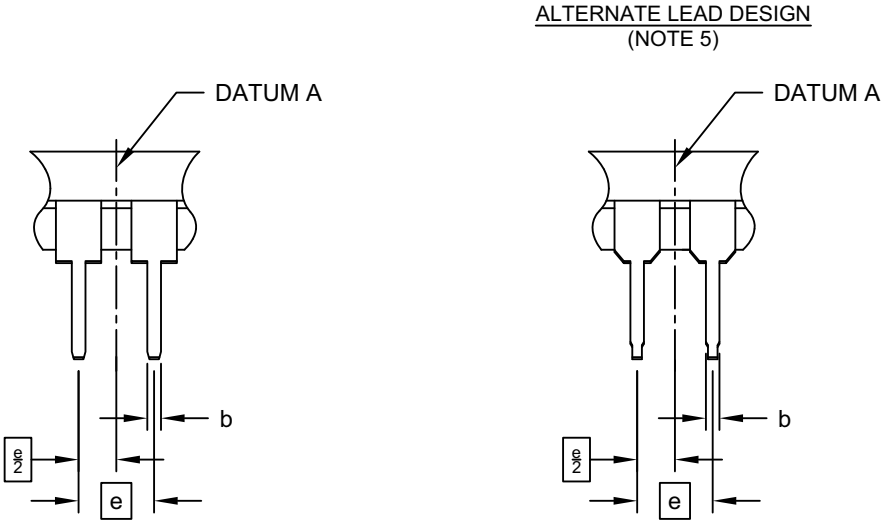


END VIEW

Microchip Technology Drawing No. C04-018-P Rev E Sheet 1 of 2

8-Lead Plastic Dual In-Line (P) - 300 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		INCHES		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		.100 BSC	
Top to Seating Plane	A	-	-	.210
Molded Package Thickness	A2	.115	.130	.195
Base to Seating Plane	A1	.015	-	-
Shoulder to Shoulder Width	E	.290	.310	.325
Molded Package Width	E1	.240	.250	.280
Overall Length	D	.348	.365	.400
Tip to Seating Plane	L	.115	.130	.150
Lead Thickness	c	.008	.010	.015
Upper Lead Width	b1	.040	.060	.070
Lower Lead Width	b	.014	.018	.022
Overall Row Spacing §	eB	-	-	.430

Notes:

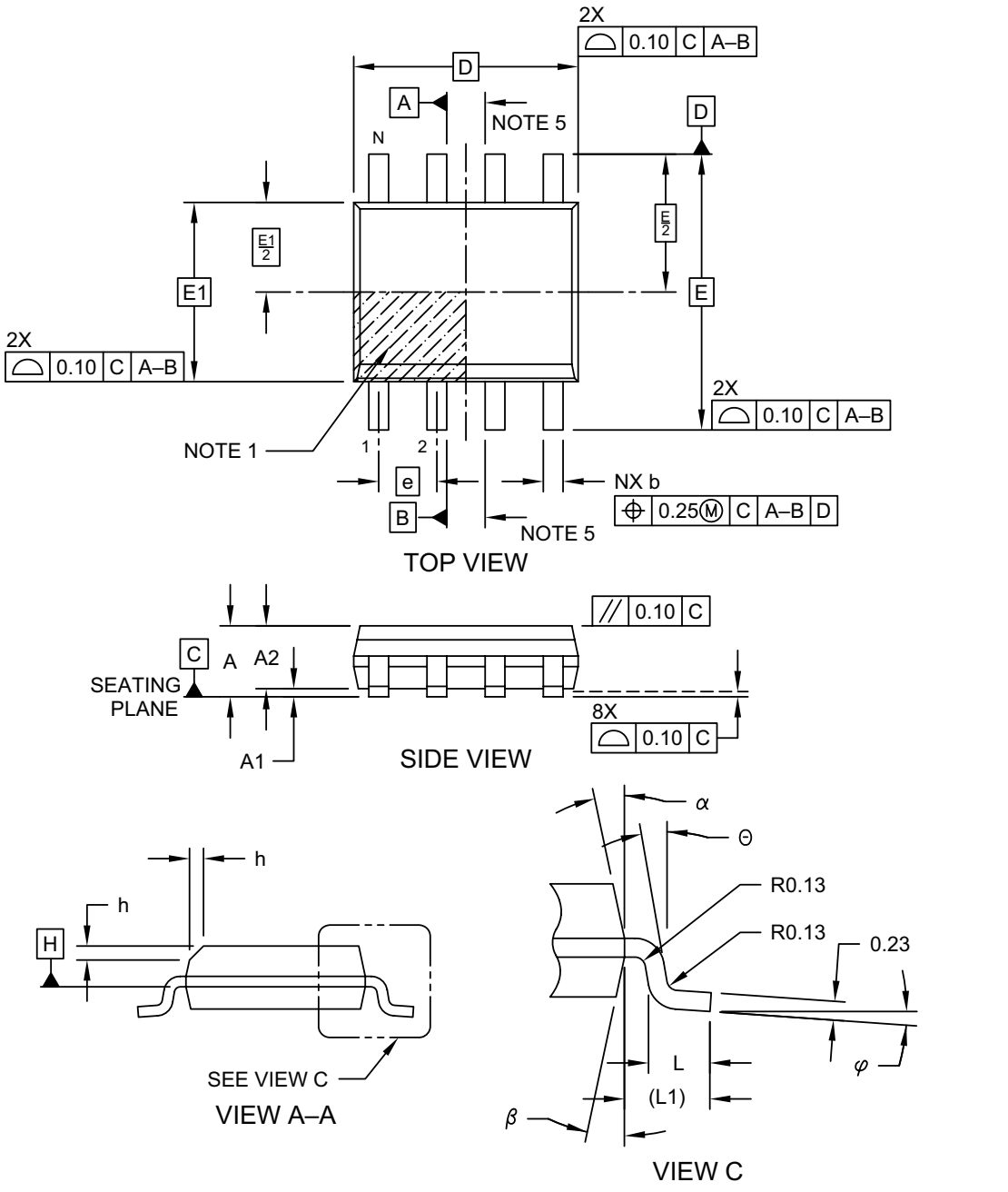
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
4. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
5. Lead design above seating plane may vary, based on assembly vendor.

Microchip Technology Drawing No. C04-018-P Rev E Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

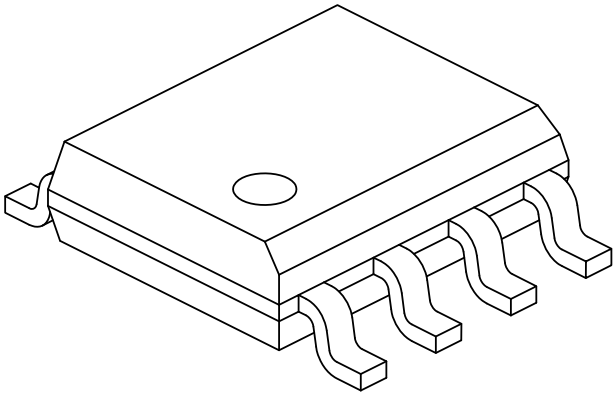
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing No. C04-057-SN Rev F Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

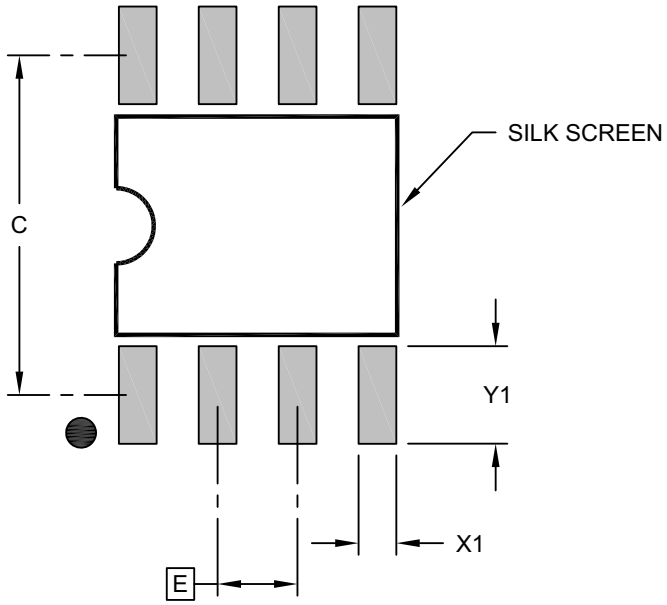
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-057-SN Rev F Sheet 2 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm (.150 In.) Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

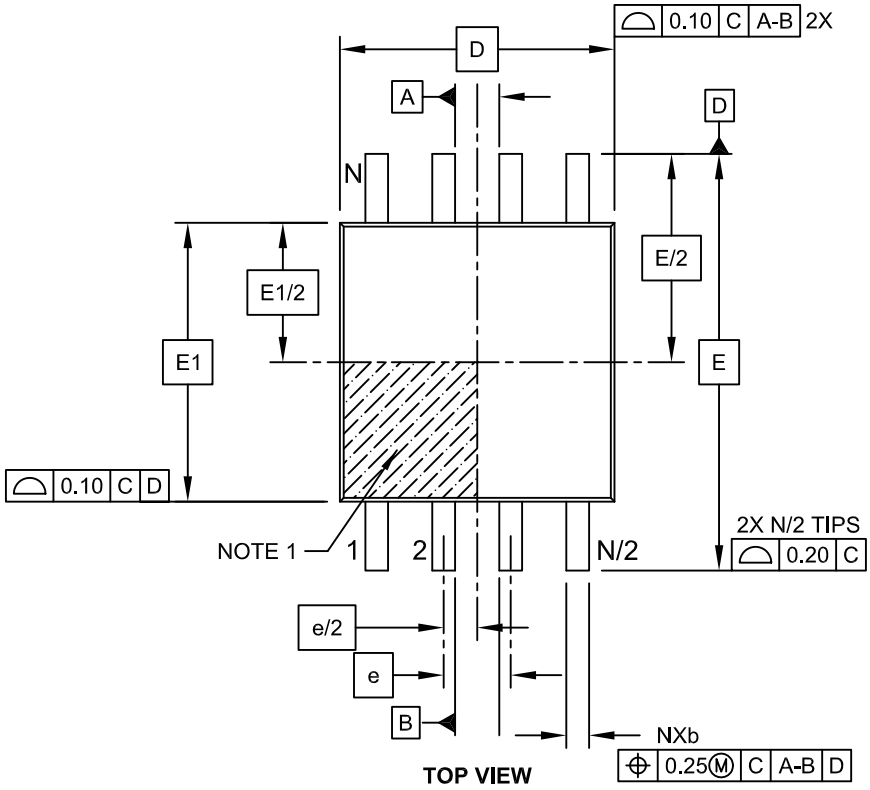
1. Dimensioning and tolerancing per ASME Y14.5M

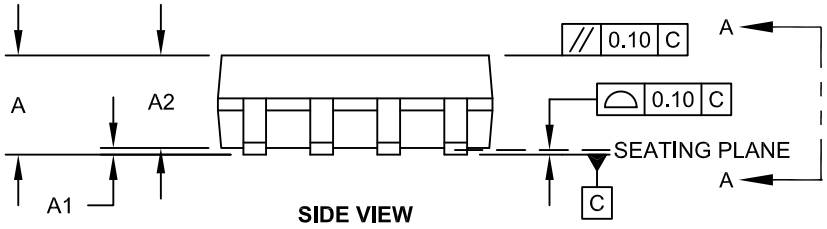
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

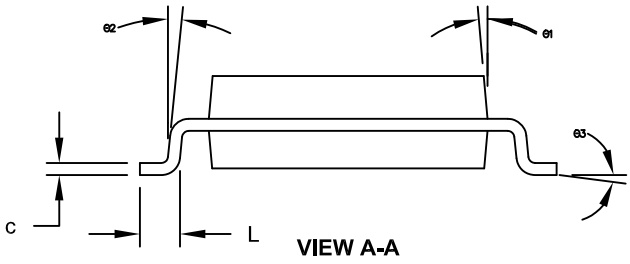
Microchip Technology Drawing C04-2057-SN Rev F

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



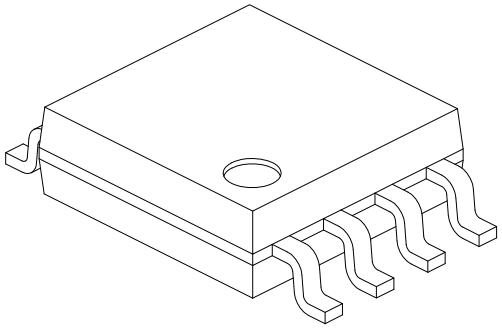




Microchip Technology Drawing C04-056C Sheet 1 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	1.77	-	2.03
Standoff §	A1	0.05		0.25
Molded Package Thickness	A2	1.75	-	1.98
Overall Width	E		7.94 BSC	
Molded Package Width	E1		5.25 BSC	
Overall Length	D		5.26 BSC	
Foot Length	L	0.51	-	0.76
Lead Thickness	c	0.15	-	0.25
Lead Width	b	0.36	-	0.51
Mold Draft Angle	θ1	-	-	15°
Lead Angle	θ2	0°	-	8°
Foot Angle	θ3	0°	-	8°

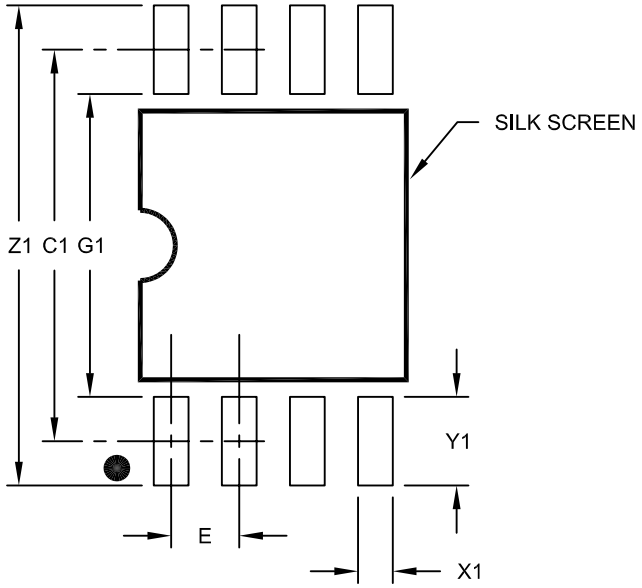
Notes:

1. SOIJ, JEITA/EIAJ Standard, Formerly called SOIC
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25mm per side.

Microchip Technology Drawing No. C04-056C Sheet 2 of 2

8-Lead Plastic Small Outline (SM) - Medium, 5.28 mm Body [SOIJ]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Overall Width	Z1			9.00
Contact Pad Spacing	C1		7.30	
Contact Pad Width (X8)	X1			0.65
Contact Pad Length (X8)	Y1			1.70
Distance Between Pads	G1	5.60		
Distance Between Pads	G	0.62		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2056C

APPENDIX A: REVISION HISTORY

Revision M (11/2021)

Updated formatting to current template; Replaced terminology “Master” and “Slave” with “Host” and “Client” respectively; Added Automotive Product Identification System; Updated PDIP and SOIC package drawings.

Revision L (08/2013)

Features Section: Revised ESD Protection to 4000V.

Revision K (04/2012)

Revised document title (removed CMOS); Revised Section 5.1.

Revision J (07/2011)

Revised Table 1-2: AC Characteristics.

Revision H (01/2011)

Revised PDIP Package Type Diagram; Revised Section 1.0 Electrical Characteristics; Revised SOIC Package Marking Information (3.90mm).

Revision G (01/2010)

Added 8-Lead SOIC Package.

Revision F (10/2008)

Corrections on the Device Selection Table; Corrections on the Description; Corrections on the AC Characteristics table; Corrections on the Pin Function Table; Corrections on the Product ID System; Updated Package Drawings.

Revision E (03/2007)

Replaced Package Drawings (Rev. AM).

Revision D (01/2007)

Revised Device Selection Table; Features Section; Changed 1.8V to 1.7V; Revised Tables 1-1, 1-2, 2-1; Revised Product ID System; Replaced Package Drawings.

Revision C (04/2006)

Revised Features, Maximum Read Current and Table 1-1, D9; Revised Table 2-1, V_{CC}; Revised Section 6.3.

Revision B (09/2005)

Section 1.0 Electrical Characteristics: revised Ambient Temperature; Revised Table 1-1; Revised Section 2.1 and Section 2.5.

Revision A (02/2005)

Original release.

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Technical support is available through the website at: http://microchip.com/support

PRODUCT IDENTIFICATION SYSTEM (NON-AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-X	/XX
Device	Tape and Reel	Temperature Range	Package

Device:	24AA1025 =	1.7V, 1024-Kbit, I^2C Serial EEPROM
	24LC1025 =	2.5V, 1024-Kbit, I^2C Serial EEPROM
	24FC1025 =	1.8V, 1024-Kbit, I^2C Serial EEPROM
Tape and Reel Option:	Blank =	Standard packaging (tube or tray)
	T =	Tape and Reel(1)
Temperature Range:	I =	-40°C to +85°C (Industrial)
	E =	-40°C to +125°C (Extended)
Package:	P =	Plastic Dual In-Line – 300 mil Body, 8-Lead (PDIP)
	SN =	Plastic Small Outline - Narrow, 3.90 mm Body, 8-Lead (SOIC)
	SM =	Plastic Small Outline – Medium, 5.28 mm Body, 8-Lead (SOIJ)

Examples:

a) 24AA1025T-I/SM: Tape and Reel, Industrial Temperature, SOIJ package.

b) 24LC1025-I/P: Industrial Temperature, PDIP package.

c) 24LC1025-E/SM: Extended Temperature, SOIJ package.

d) 24LC1025T-I/SM: Tape and Reel, Industrial Temperature, SOIJ package.

e) 24FC1025T-I/SN: Tape and Reel, Industrial Temperature, SOIC package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

PRODUCT IDENTIFICATION SYSTEM (AUTOMOTIVE)

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	X	/XX	XXX(2, 3)
Device	Tape and Reel Option	Temperature Range	Package	Variant

Device:	24LC1024	= 2.5V, 1024-Kbit, I^2C Serial EEPROM
	24FC1024	= 1.8V, 1024-Kbit, I^2C Serial EEPROM
Tape and Reel Option:	Blank	= Standard packaging (tube or tray)
	T	= Tape and Reel(1)
Temperature Range:	I	= -40°C to +85°C (AEC-Q100 Grade 3)
	E	= -40°C to +125°C (AEC-Q100 Grade 1)
Package:	SN	= Plastic Small Outline – Narrow, 3.90 mm Body, 8-Lead (SOIC)
	SM	= Plastic Small Outline – Medium, 5.28 mm Body, 8-Lead (SOIJ)
Variant(2, 3):	16KVAO	= Standard Automotive, 16K Process
	16KVXX	= Customer-Specific Automotive, 16K Process

Examples:

a) 24LC1025-E/SN16KVAO : Automotive Grade 1, 2.5V, SOIC Package.

b) 24LC1025T-E/SN16KVAO : Tape and Reel, Automotive Grade 1, 2,5V, SOIC Package.

c) 24FC1025T-I/SM16KVAO : Tape and Reel, Automotive Grade 3, 1.8V, SOIJ Package.

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: The VAO/VXX automotive variants have been designed, manufactured, tested and qualified in accordance with AEC-Q100 requirements for automotive applications.

3: For customers requesting a PPAP, a customer-specific part number will be generated and provided. A PPAP is not provided for VAO part numbers.

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- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
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ISBN: 978-1-5224-9157-6

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