SNx5176B Differential Bus Transceivers

1 Features

- Bidirectional transceivers
- Meets or exceeds the requirements of ANSI standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27
- Designed for multipoint transmission on long bus lines in noisy environments
- 3-state driver and receiver outputs
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- ±60mAm maximum driver output capability
- Thermal shutdown protection
- Driver positive and negative current limiting
- 12kΩ minimum receiver input impedance
- ±200mV receiver input sensitivity
- 50mV typical receiver input hysteresis
- Operates from a single 5V supply

2 Applications

- Chemical and gas sensors
- Digital signage
- Human machine interfaces (HMI)
- Motor controls
  - AC induction
  - Brushed and brush-less DC
  - Low- and high-voltage
  - Stepper motors
  - Permanent magnets
- TETRA base stations
- Telecommunication towers
  - Remote electrical tilt (RET) units
  - Tower mounted amplifiers (TMA)
- Weigh scales
- Wireless repeaters

3 Description

The SN65176B and SN75176B differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. The SN65176B and SN75176B are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

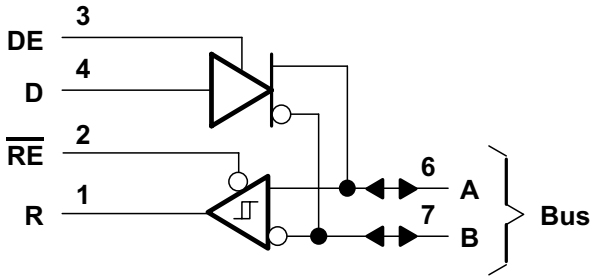
The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5V power supply. The driver has a active-high enable and the receiver has an active-low enable, that can connect together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device appropriate for party-line applications.

The driver is designed for up to 60mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12kΩ, an input sensitivity of ±200mV, and a typical input hysteresis of 50mV.

Package Information

PART NUMBER	PACKAGE (PIN)(1)	PACKAGE SIZE(2)
SNx5176	D (SOIC, 8)	4.90mm × 3.91mm
	P (PDIP, 8)	9.81mm × 6.35mm
	PS (SOP, 8)	6.20mm × 5.30mm

(1) For more information, see Section 10.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Schematic

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4 Pin Configuration and Functions

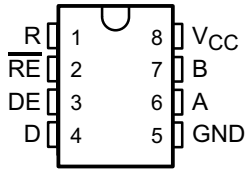


Figure 4-1. Top View

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Logic data output from RS-485 Receiver
$\overline{RE}$	2	I	Receive enable (active low)
DE	3	I	Driver enable (active high)
D	4	I	Logic data input to RS-485 driver
GND	5	—	Device ground pin
A	6	I/O	RS-422 or RS-485 data line
B	7	I/O	RS-422 or RS-485 data line
V_{CC}	8	—	Power input, connect to 5V power source

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_I	Enable input voltage		5.5	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1.6mm (1/16 inch) from case for 10 seconds		260	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

5.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		-7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65176B	–40		105	°C
		SN75176B	0		70	

(1) Differential input/output bus voltage is measured at the non-inverting terminal A, with respect to the inverting terminal B.

5.3 Thermal Information

THERMAL METRIC(1)		SNx5176			UNIT
		D (SOIC)	PS (SO)	P (PDIP)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.4	113.2	88.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	57.9	65.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.6	69.0	69.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	14.6	35.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	68.1	64.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application note.

5.4 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP[2]	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18mA				–1.5	V
V_O	Output voltage	I_O = 0		0		Vcc	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	Vcc	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100Ω, see Figure 6-1		½ V_{OD1} or 2 [3]			V
		R_L = 54Ω, see Figure 6-1		1.5	2.5	5	
V_{OD3}	Differential output voltage	See [4]		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage[5]	R_L = 54Ω or 100Ω, see Figure 6-1				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54Ω or 100Ω, see Figure 6-1		-1		+3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage[5]	R_L = 54Ω or 100Ω, see Figure 6-1				±0.2	V
I_O	Output current	Output disabled[6]	V_O = 12V			1	mA
			V_O = –7V			–0.8	
I_{IH}	High-level input current	V_I = 2.4V				20	µA
I_{IL}	Low-level input current	V_I = 0.4V				–400	µA
I_{OS}	Short-circuit output current	V_O = –7V				–250	mA
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 12V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

(1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5V and T_A = 25°C.
(3) The minimum V_{OD2} with a 100Ω load is either ½ V_{OD1} or 2V, whichever is greater.
(4) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
(5) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A the for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

5.5 Electrical Characteristics – Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7V, I_O = –0.4mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5V, I_O = 8mA		–0.2(2)			V
V_{hys}	Input hysteresis voltage (V_{IT+} – $V_{IT–}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = –18mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200mV, I_{OH} = –400µA, see Figure 6-2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200mV, I_{OL} = 8mA, see Figure 6-2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4V to 2.4V				±20	µA
I_I	Line input current	Other input = 0V(3)	V_I = 12V			1	mA
			V_I = –7V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7V				20	µA
I_{IL}	Low-level enable input current	V_{IL} = 0.4V				–100	µA
r_I	Input resistance	V_I = 12V		12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

(1) All typical values are at V_{CC} = 5V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

5.6 Switching Characteristics – Driver

V_{CC} = 5V, R_L = 110Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54Ω, see Figure 6-3		15	22	ns
$t_{t(OD)}$	Differential-output transition time	R_L = 54Ω, see Figure 6-3		20	30	ns
t_{PZH}	Output enable time to high level	See Figure 6-4		85	120	ns
t_{PZL}	Output enable time to low level	See Figure 6-5		40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 6-4		150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 6-5		20	30	ns

5.7 Switching Characteristics – Receiver

V_{CC} = 5V, C_L = 15pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3V, see Figure 6-6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	
t_{PZH}	Output enable time to high level	See Figure 6-7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	
t_{PHZ}	Output disable time from high level	See Figure 6-7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	

5.8 Typical Characteristics

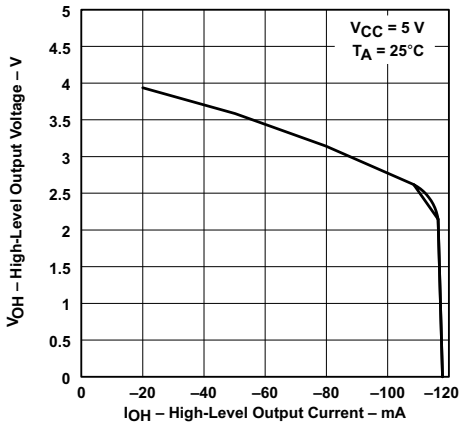


Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current

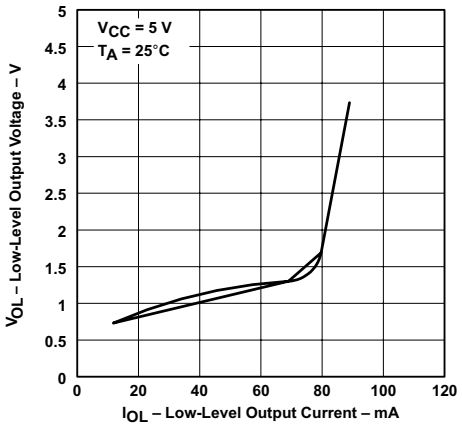


Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

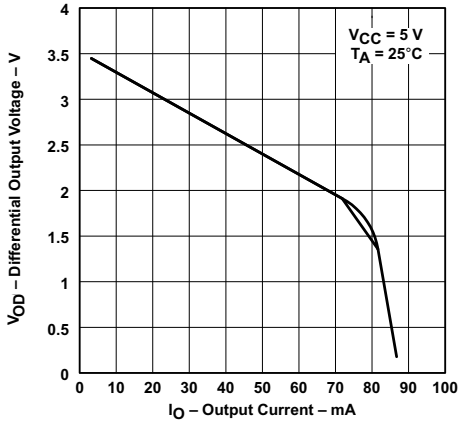


Figure 5-3. Driver Differential Output Voltage vs Output Current

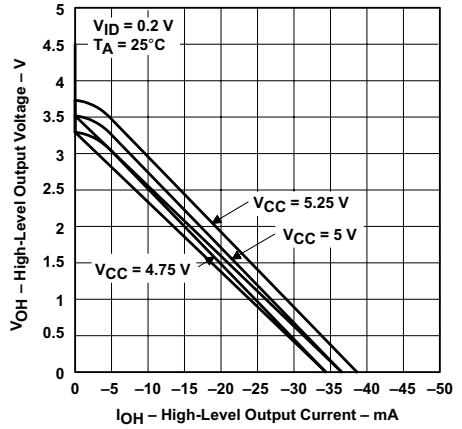
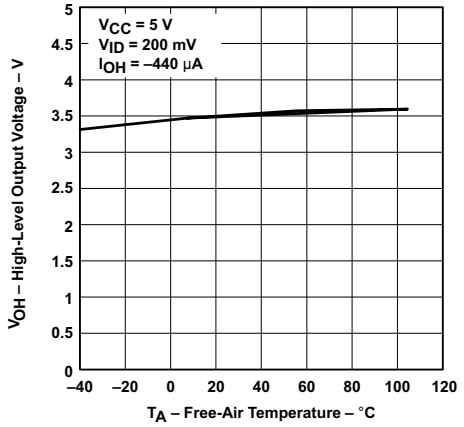


Figure 5-4. Receiver High-Level Output Voltage vs High-Level Output Current



Only the 0°C to 70°C portion of the curve applies to the SN75176B device.

Figure 5-5. Receiver High-Level Output Voltage vs Free-Air Temperature

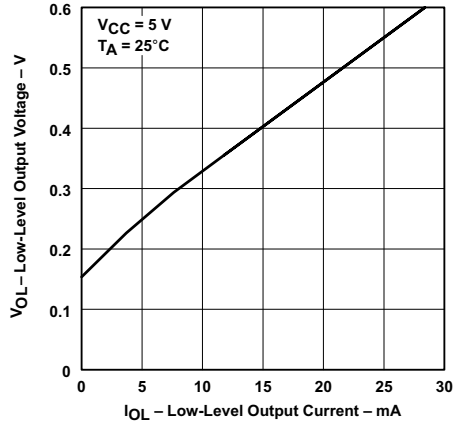


Figure 5-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

5.8 Typical Characteristics (continued)

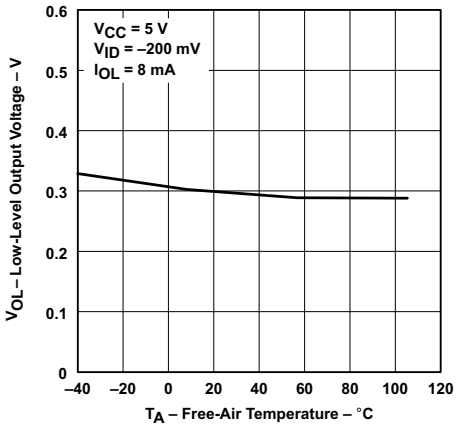


Figure 5-7. Receiver Low-Level Output Voltage vs Free-Air Temperature

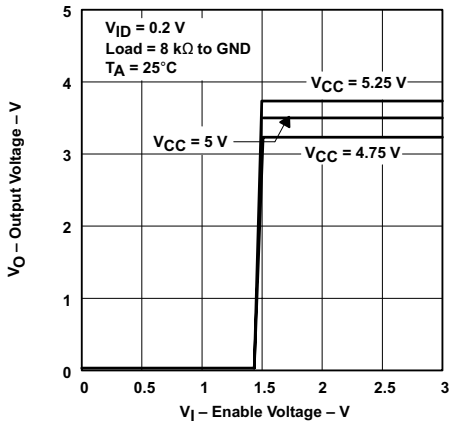


Figure 5-8. Receiver Output Voltage vs Enable Voltage

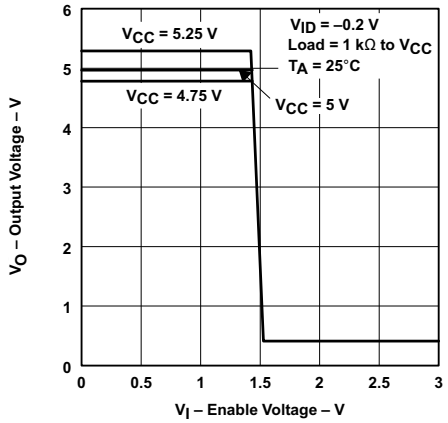


Figure 5-9. Receiver Output Voltage vs Enable Voltage

Parameter Measurement Information

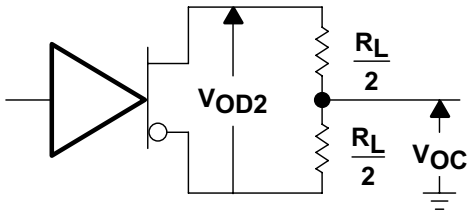


Figure 6-1. Driver V_{OD} and V_{OC}

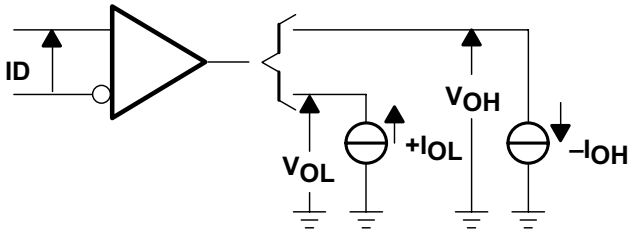
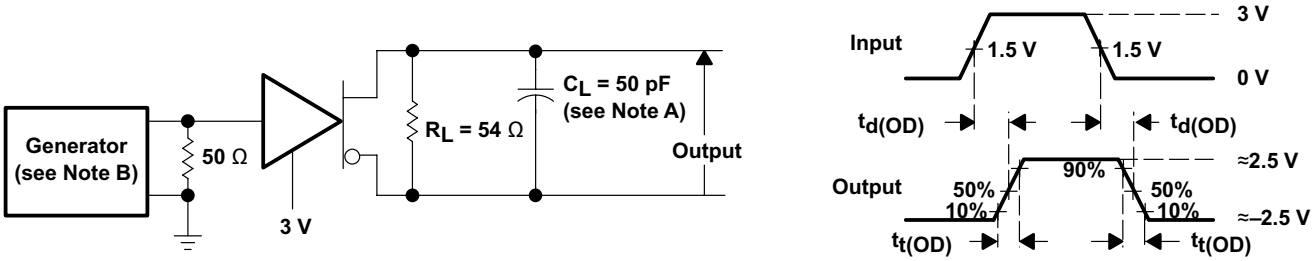


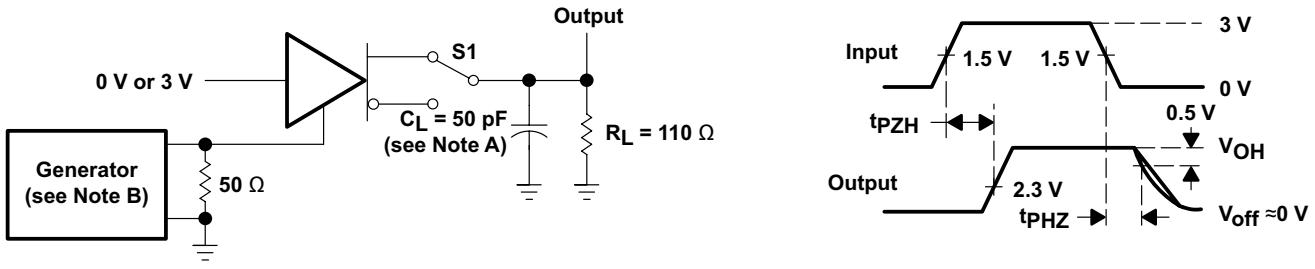
Figure 6-2. Receiver V_{OH} and V_{OL}



TEST CIRCUIT **VOLTAGE WAVEFORMS**

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1MHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT **VOLTAGE WAVEFORMS**

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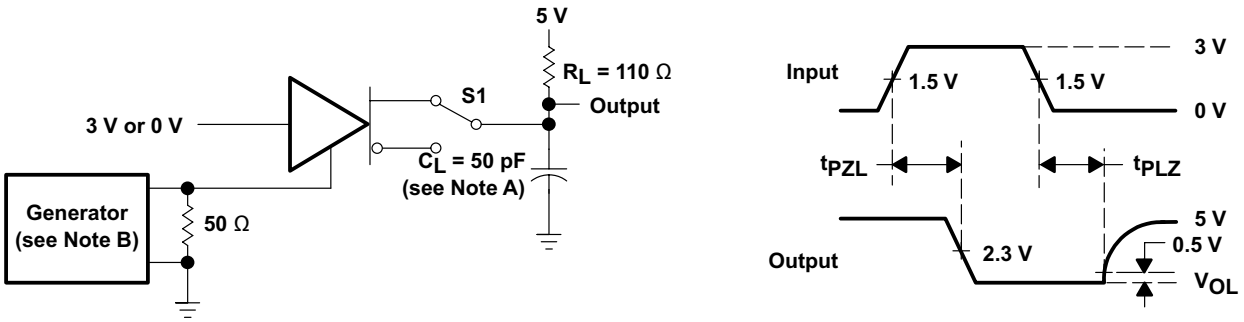
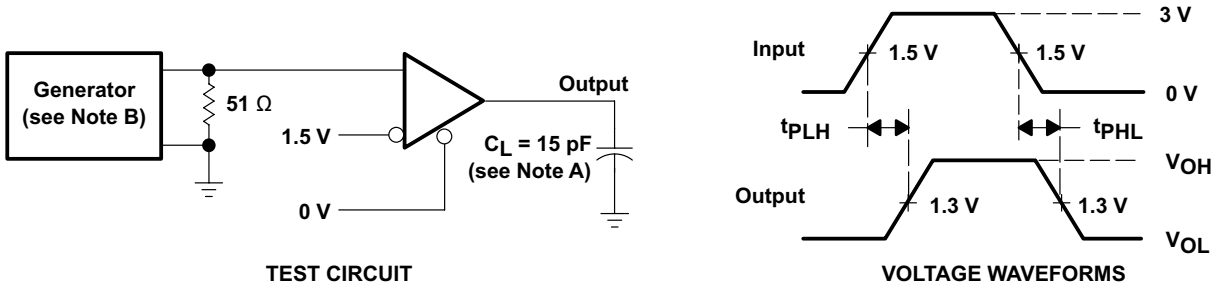
Figure 6-4. Driver Test Circuit and Voltage Waveforms



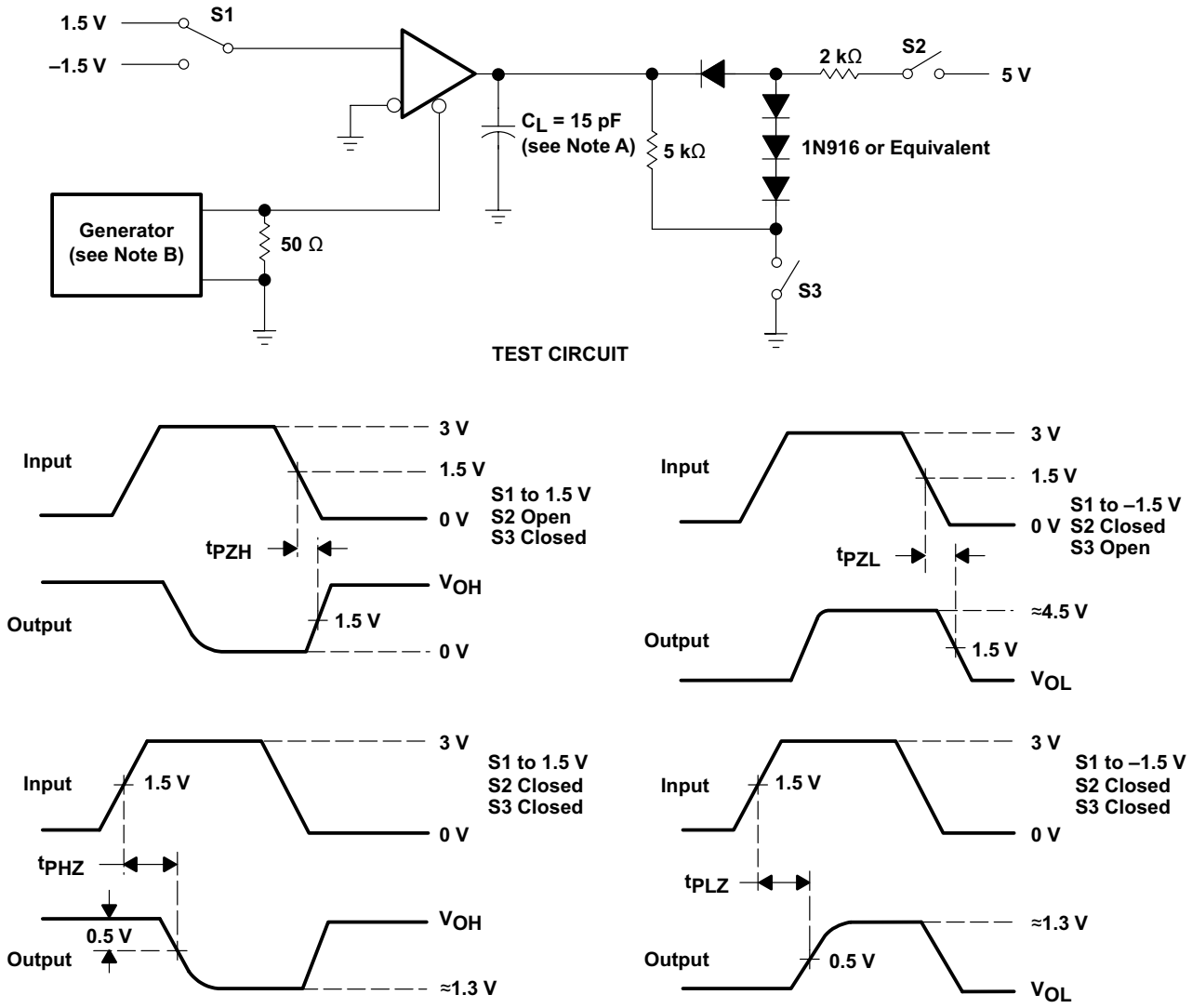
A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1MHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-5. Driver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1MHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-6. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1MHz, 50% duty cycle, t_r ≤ 6ns, t_f ≤ 6ns, Z_O = 50Ω.

Figure 6-7. Receiver Test Circuit and Voltage Waveforms

6 Detailed Description

6.1 Overview

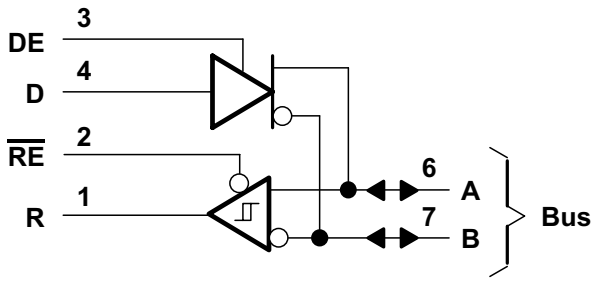
The SN65176B and SN75176B differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B devices can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. Use the TTL logic input, the DE pin, to turn the driver on and off.

Table 6-1. Driver Function (1)

INPUT D	ENABLE DE	DIFFERENTIAL OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level, = low level, X = irrelevant, Z = high impedance (off)

6.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. Use the TTL logic input, the $\overline{RE}$ pin, to turn the receiver logic output on and off.

Table 6-2. Receiver Function Table (1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2V$	L	H
$-0.2V < V_{ID} < 0.2V$	L	U
$V_{ID} \leq -0.2V$	L	L
X	H	Z
Open	L	U

(1) H = high level, L = low level, U = unknown, Z = high impedance (off)

6.4 Device Functional Modes

6.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and $\overline{RE}$ can be connected together for a single port direction control bit.

6.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports. The bus ports are designed to offer minimum loading to the bus when the driver is disabled or $V_{CC} = 0$.

6.4.3 Symbol Cross Reference

Table 6-3. Symbol Equivalents

DATA SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\|V_{OD1}\|$	V_o	V_o
$\|V_{OD2}\|$	V_t ®$_L$ = 100Ω)	V_t ®$_L$ = 54Ω)
$\|V_{OD3}\|$		V_t (test termination measurement 2)
$\Delta\|V_{OD}\|$	$\| \|V_t\| - \|\overline{V}_t\| \|$	$\| \|V_t - \|\overline{V}_t\| \|$
V_{OC}	$\|V_{os}\|$	$\|V_{os}\|$
$\Delta\|V_{OC}\|$	$\|V_{os} - \overline{V}_{os}\|$	$\|V_{os} - \overline{V}_{os}\|$
I_{OS}	$\|I_{sa}\|$, $\|I_{sb}\|$	
I_O	$\|I_{xa}\|$, $\|I_{xb}\|$	I_{ia}, I_{ib}

7 Application and Implementation

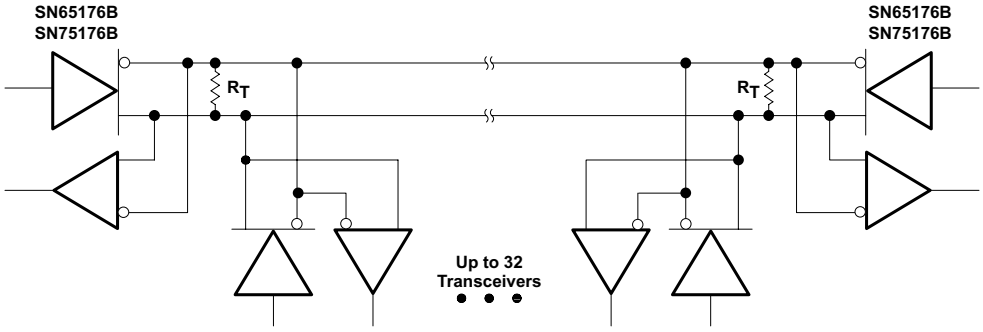
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

Use SN65176B and SN75176B in RS-485 and RS-422 physical layer communications.

7.2 Typical Application



Termiante the line at both ends in its characteristic impedance ®$_T$ = Z_O). Keep the stub lengths off of the main line as short as possible.

Figure 7-1. Typical RS-485 Application Circuit

7.2.1 Design Requirements

- 5V power source
- RS-485 bus operating at 10Mbps or less
- Connector that establishes the correct polarity for port pins
- External fail safe implementation

7.2.2 Detailed Design Procedure

Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line. If desired, add external fail-safe biasing to establish +200mV on the A-B port.

7.2.3 Application Curves

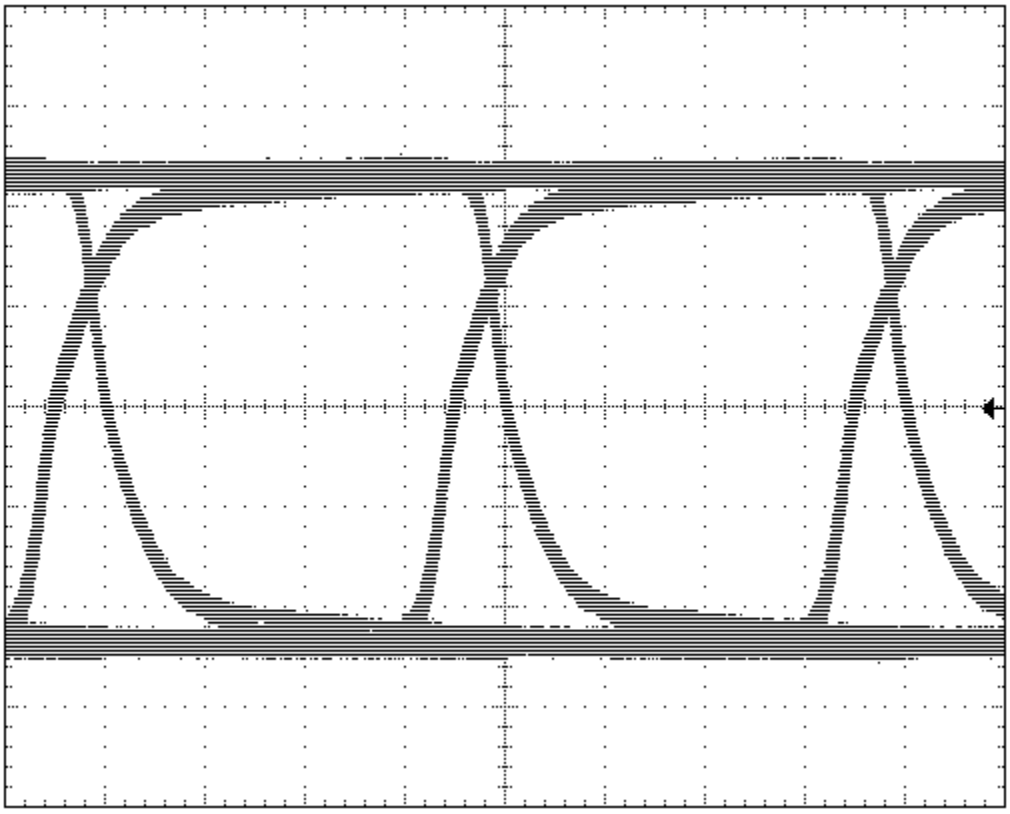


Figure 7-2. Eye Diagram for 10Mbits/s Over 100 feet of Standard CAT-5E Cable 120Ω Termination at Both Ends

In Figure 7-2, the scale is 1V per division and 25nS per division.

7.3 System Examples

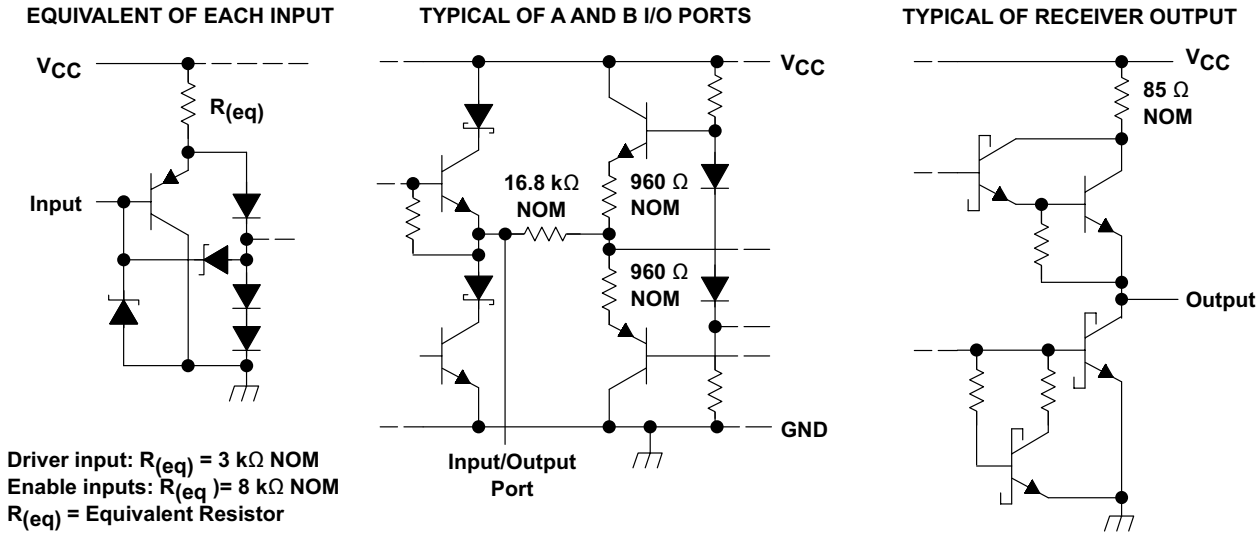


Figure 7-3. Schematics of Inputs and Outputs

7.4 Power Supply Recommendations

Establish a power supply of 5V with a tolerance less than 10%.

7.5 Layout

7.5.1 Layout Guidelines

Traces from device pins A and B to connector must be short and capable of 250 mA maximum current.

7.5.2 Layout Example

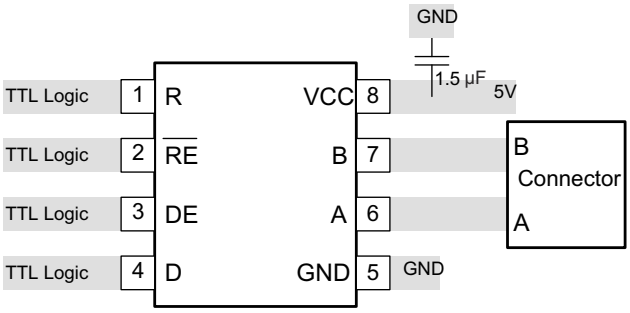


Figure 7-4. Layout Diagram

8 Device and Documentation Support

8.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (December 2021) to Revision I (August 2025)	Page
• Added a 3-row tape and reel option for the SN65176BDE orderable	18

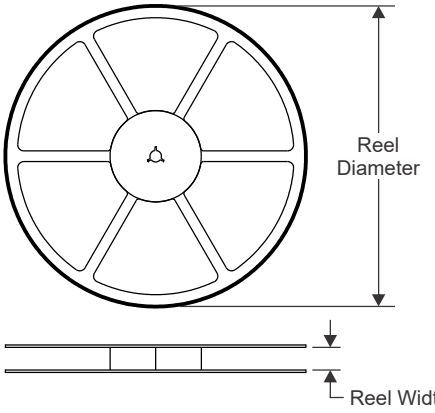
Changes from Revision G (July 2021) to Revision H (December 2021)	Page
• Changed ψ_{JT} From 78.8 to 8.8 for the D package in the *Thermal Information* table	4

10 Mechanical, Packaging, and Orderable Information

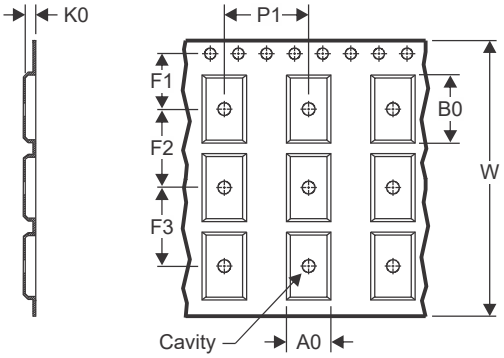
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

10.1 Tape and Reel Information

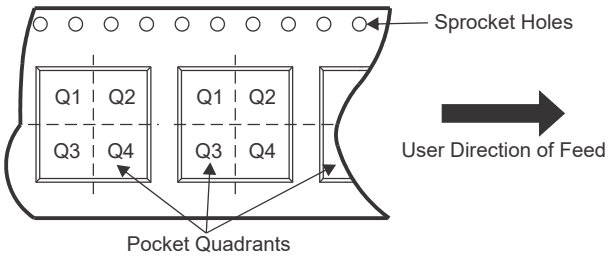
REEL DIMENSIONS



TAPE DIMENSIONS



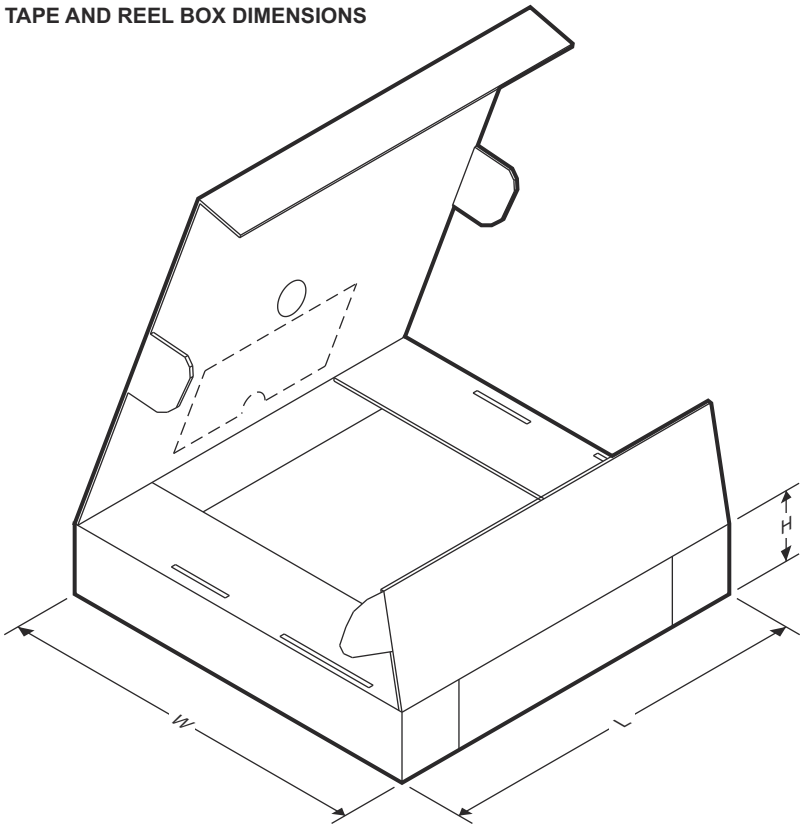
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers
F1	Distance between centers of sprocket hole and first cavity row
F2	Distance between centers of first and second cavity rows
F3	Distance between centers of second and third cavity rows

Device	Package Type	Package Drawing	Pins	SPQ	Carrier	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant	F1 (mm)	F2 (mm)	F3 (mm)
SN65176BDR	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN65176BDR	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN65176BDR	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN65176BDRG4	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN65176BDRG4	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN75176BDR	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN75176BDR	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN75176BDR	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN75176BDRG4	SOIC	D	8	2500	Single row	330	12.4	6.4	5.2	2.1	8	12	Q1	—	—	—
SN75176BPSR	SO	PS	8	2000	Single row	330	16.4	8.35	6.6	2.4	12	16	Q1	—	—	—
SN65176BDE	SOIC	D	8	7500	Multi-row (3)	330	24.4	6.45	5.25	2.1	8	24	Q1	5.25	6.25	6.25

TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65176BDR	SOIC	D	8	2500	353	353	32
SN65176BDR	SOIC	D	8	2500	353	353	32
SN65176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65176BDRG4	SOIC	D	8	2500	340.5	336.1	25
SN65176BDRG4	SOIC	D	8	2500	353	353	32
SN75176BDR	SOIC	D	8	2500	353	353	32
SN75176BDR	SOIC	D	8	2500	353	353	32
SN75176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75176BDRG4	SOIC	D	8	2500	340.5	336.1	25
SN75176BPSR	SO	PS	8	2000	353	353	32
SN65176BDE	SOIC	D	8	7500	356.0	356.0	45.0

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65176BD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 105	65176B
SN65176BDE	Active	Production	SOIC (D) | 8	7500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B
SN65176BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B
SN65176BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B
SN65176BDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B
SN65176BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B
SN65176BDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B
SN65176BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	SN65176BP
SN65176BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 105	SN65176BP
SN75176BD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	75176B
SN75176BDG4	NRND	Production	null (null) |	75 | TUBE	-	Call TI	Call TI	0 to 70	
SN75176BDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B
SN75176BDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B
SN75176BDRE4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B
SN75176BDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B
SN75176BDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B
SN75176BP	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75176BP
SN75176BP.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75176BP
SN75176BPE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	SN75176BP
SN75176BPSR	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B
SN75176BPSR.A	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B
SN75176BPSRG4	Active	Production	SO (PS) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

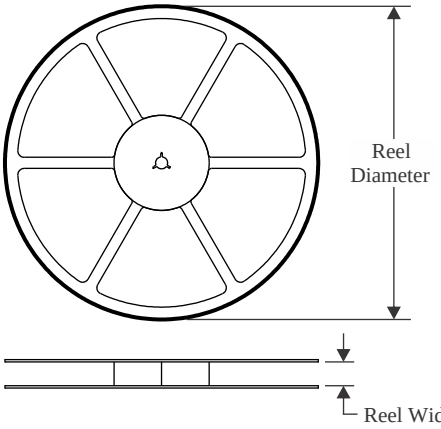
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

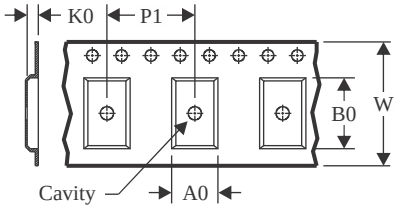
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

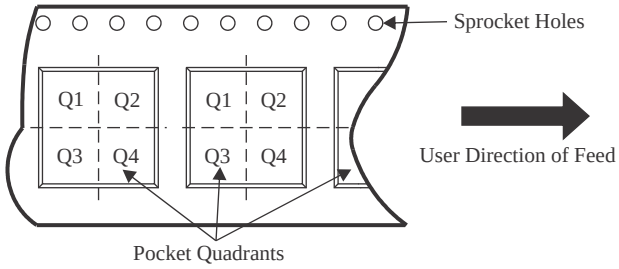


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

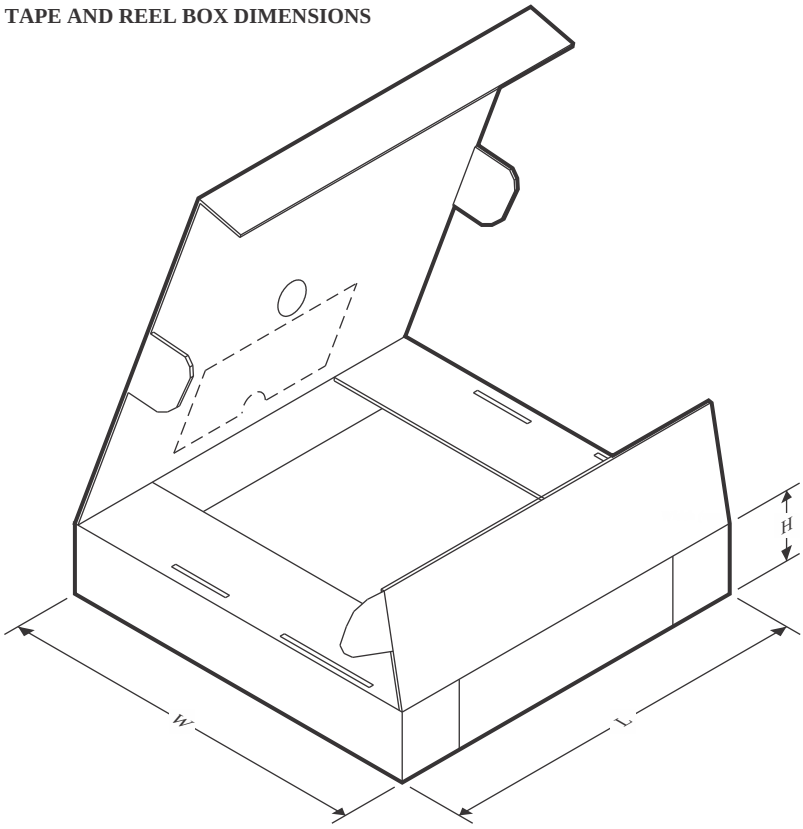
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

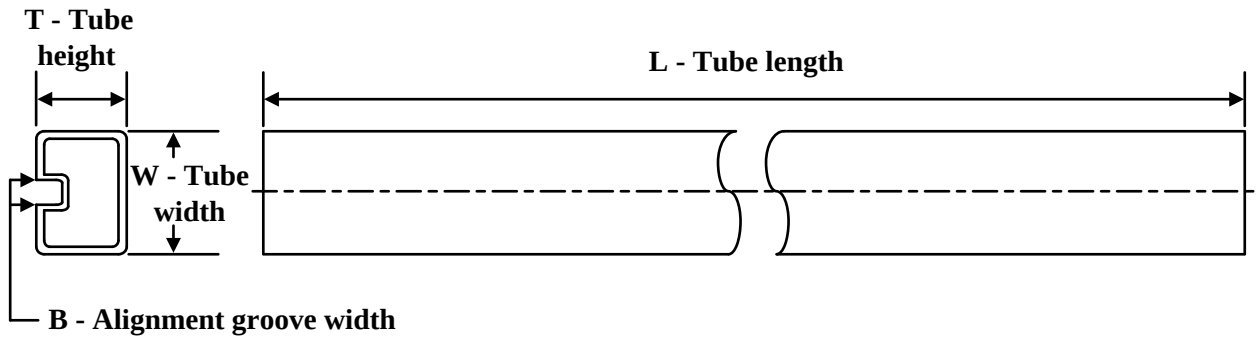
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

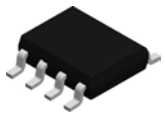
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65176BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN65176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65176BDRG4	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75176BDR	SOIC	D	8	2500	353.0	353.0	32.0
SN75176BDRG4	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BPSR	SO	PS	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN65176BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BP.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BPE4	P	PDIP	8	50	506	13.97	11230	4.32

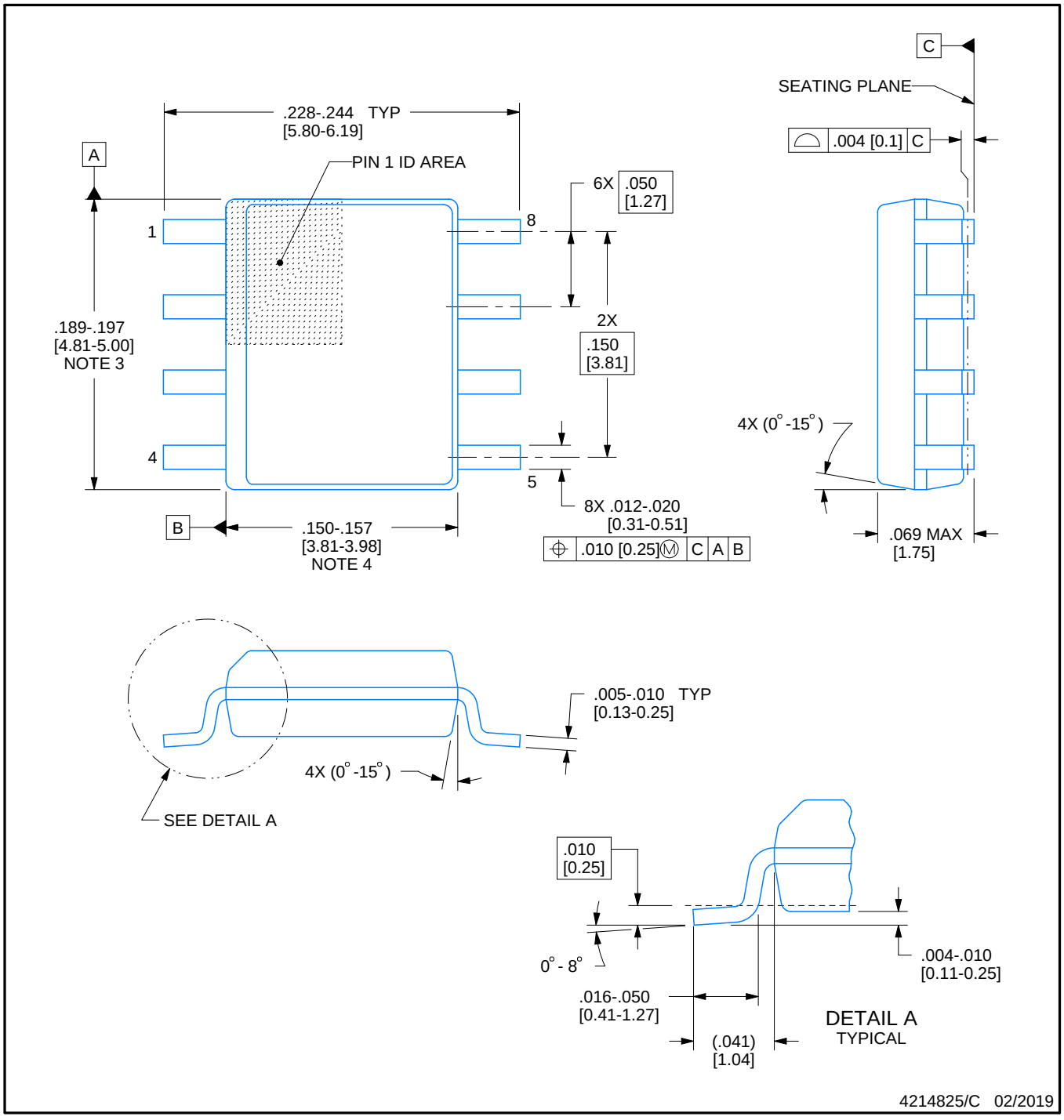


PACKAGE OUTLINE

D0008A

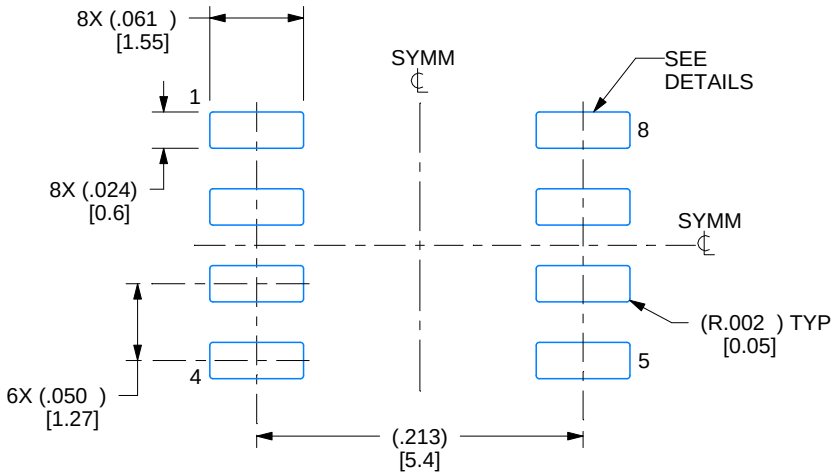
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

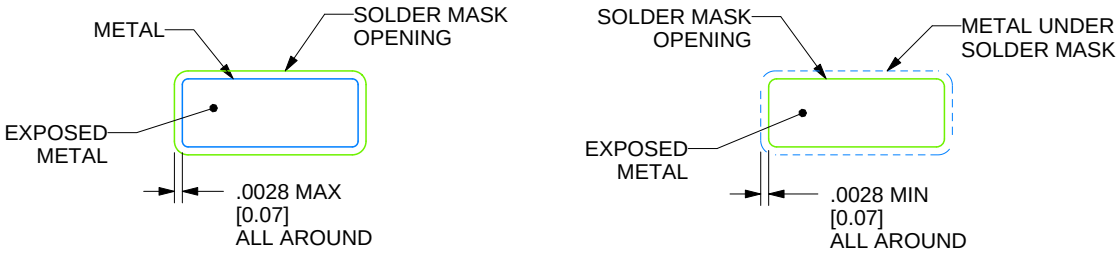


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

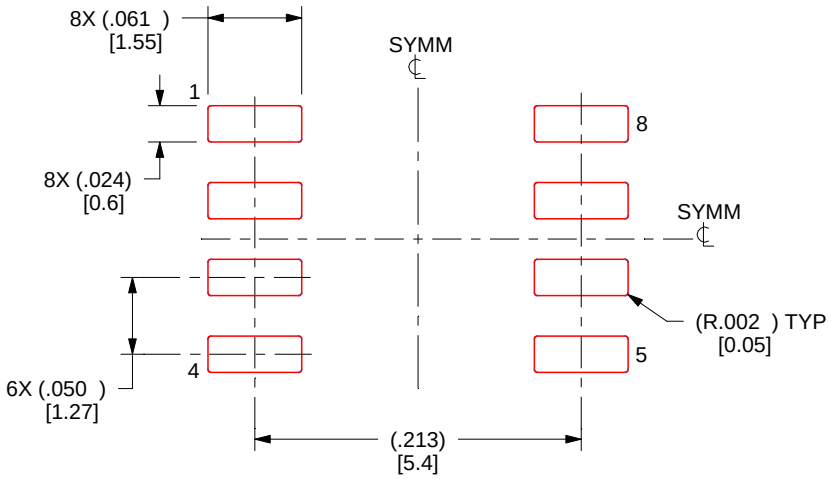
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

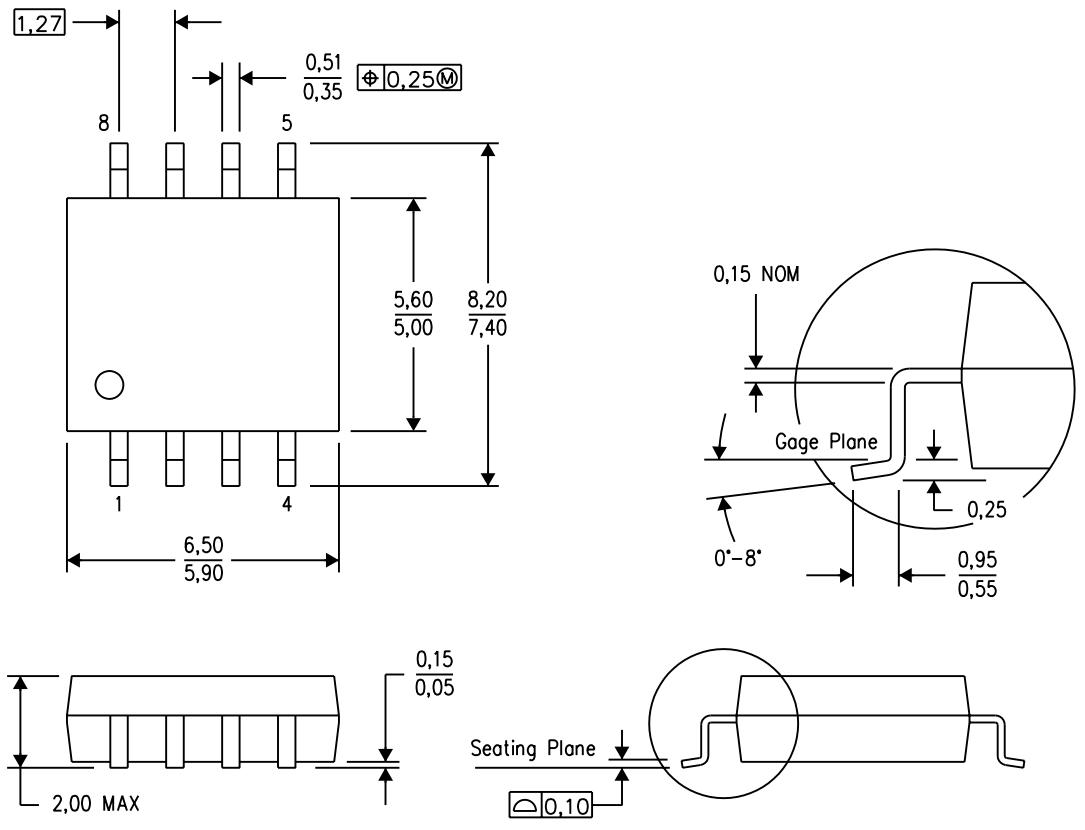
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

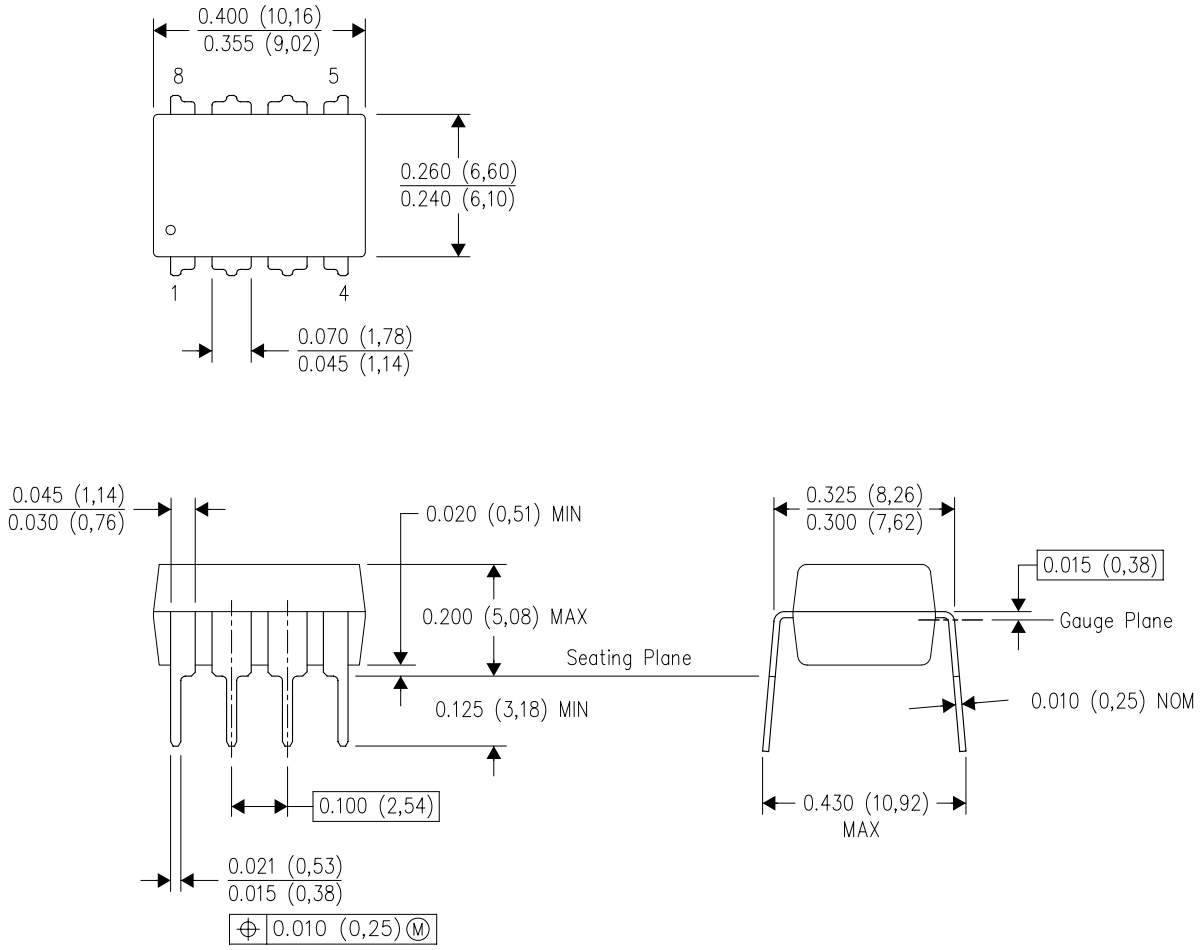
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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Last updated 10/2025