SN65HVD7x 3.3-V Supply RS-485 With IEC ESD protection

1 Features

- Small-size VSSOP Packages Save Board Space, or SOIC for Drop-in Compatibility
- Bus I/O Protection
  - >±15 kV HBM Protection
  - >±12 kV IEC 61000-4-2 Contact Discharge
  - >±4 kV IEC 61000-4-4 Fast Transient Burst
- Extended Industrial Temperature Range –40°C to 125°C
- Large Receiver Hysteresis (80 mV) for Noise Rejection
- Low Unit-Loading Allows Over 200 Connected Nodes
- Low Power Consumption
  - Low Standby Supply Current: < 2 µA
  - I_{CC} < 1 mA Quiescent During Operation
- 5-V Tolerant Logic Inputs Compatible With 3.3-V or 5-V Controllers
- Signaling Rate Options Optimized for: 250 kbps, 20 Mbps, 50 Mbps
- Glitch Free Power-Up and Power-Down Bus Inputs and Outputs

2 Applications

- Factory Automation
- Telecommunications Infrastructure
- Motion Control

3 Description

These devices have robust 3.3-V drivers and receivers in a small package for demanding industrial applications. The bus pins are robust to ESD events with high levels of protection to Human-Body Model and IEC Contact Discharge specifications.

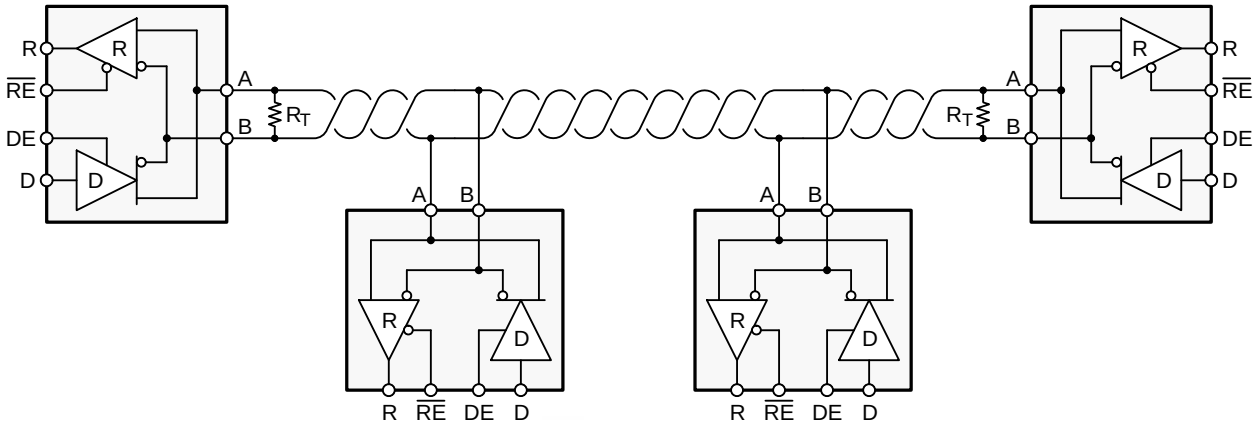
Each of these devices combines a differential driver and a differential receiver which operate from a single 3.3-V power supply. The driver differential outputs and the receiver differential inputs are connected internally to form a bus port suitable for half-duplex (two-wire bus) communication. These devices feature a wide common-mode voltage range making the devices suitable for multi-point applications over long cable runs. These devices are characterized from –40°C to 125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN65HVD72, SN65HVD75, SN65HVD78	SOIC (8)	4.91 mm × 3.90 mm
	VSSOP (8)	3.00 mm × 3.00 mm
	VSON (8)	

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (Januarly 2019) to Revision H — **Page**

- Changed the Pin Configuration images ... 4
- Changed Supply voltage, V_{CC} MAX value From = 3.6 V To: 5 V in the *Absolute Maximum Ratings* table ... 5
- Deleted "or R pin" for V_{CC} in the *Absolute Maximum Ratings* ... 5
- Added reliability note to V_{CC} in the *Recommended Operating Conditions* table ... 5

Changes from Revision F (December 2016) to Revision G — **Page**

- Changed From: Supply voltage, V_{CC} MAX value = 5.5 V To: Supply voltage, V_{CC} or R pin MAX value = 3.6 V in the *Absolute Maximum Ratings* table ... 5
- Changed From: Input voltage at any logic pin To: Voltage at D, DE, or $\overline{RE}$ in the *Absolute Maximum Ratings* table ... 5

Changes from Revision E (September 2016) to Revision F — **Page**

- Changed pin A From: 7 To: 6, and pin B From: 6 To: 7 in Figure 26 ... 22

Changes from Revision D (July 2015) to Revision E — **Page**

- Added new Feature: Glitch Free Power-Up and Power-Down Bus Inputs and Outputs ... 1

Changes from Revision C (September 2013) to Revision D **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1

Changes from Revision B (June 2012) to Revision C **Page**

- Deleted Feature: > ±12kV IEC61000-4-2 Air-Gap Discharge 1
- Added Footnote 2 to the *Absolute Maximum Ratings* table 5
- Changed the Switching Characteristics conditions statement From: 250 kbps devices (SN65HVD70, 71, 72) bit time > 4 µs To: 250 kbps device (SN65HVD72) bit time ≥ 4 µs 7
- Changed the Switching Characteristics conditions statement From: 250 kbps devices (SN65HVD73, 74, 75) bit time > 50 ns To: 250 kbps device (SN65HVD75) bit time ≥ 50 ns 8
- Changed the Switching Characteristics conditions statement From: 250 kbps devices (SN65HVD76, 77, 78)bit time > 20 ns To: 250 kbps device (SN65HVD78) bit time ≥ 20 ns 8
- Added note : R_L = 54 Ω to Figure 6, Figure 7, and Figure 8 9
- Added the DGK package to the SN65HVD72, 75, 78 Logic Diagram 15
- Replaced the LOW-POWER STANDBY MODE section 19
- Added text to the Transient Protection section 20

Changes from Revision A (May 2012) to Revision B **Page**

- Added the SON-8 package and Nodes column to *Device Comparison Table*, ... 4
- Changed the Voltage range at A or B Inputs MIN value From: –8 V To: –13 V in the *Absolute Maximum Ratings* table 5
- Added footnote for free-air temperature to the Recommended Operating Conditions table 5
- Changed the Bus input current (disabled driver) TYP values for HVD78 V_I = 12 V From: 150 To: 240 and V_I = –7 V From: –120 To: –180 7
- Changed, Thermal Information 7
- Changed, Thermal Characteristics 7
- Added TYP values to the Switching Characteristics table 8
- Added TYP values to the Switching Characteristics table 8
- Changed the SN65HVD72, 75, 78 Logic Diagram 15
- Added section: LOW-POWER STANDBY MODE 19

Changes from Original (March 2012) to Revision A **Page**

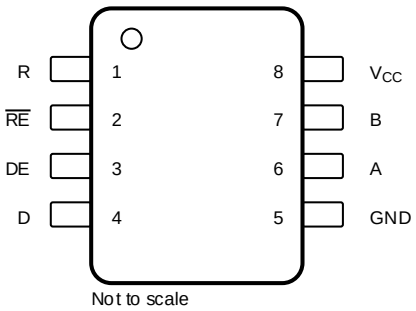
- Added VALUEs to the Thermal Characteristics table in the DEVICE INFORMATION section. 7
- Changed the Switching Characteristics condition statement From: 15 kbps devices (SN65HVD73, 74, 75) bit time > 65 ns To: 20 Mbps devices (SN65HVD73, 74, 75) bit time > 50 ns 8
- Changed the Switching Characteristics condition statement From: 50 kbps devices (SN65HVD76, 77, 78) bit time > 20 ns To: 50 Mbps devices (SN65HVD76, 77, 78) bit time > 20 ns 8
- Added Figure 4 to *Typical Characteristics*. 9
- Added Figure 5 to *Typical Characteristics*. 9
- Added Figure 6 to *Typical Characteristics*. 9
- Added Figure 7 to *Typical Characteristics*. 9
- Added Figure 8 to *Typical Characteristics*. 9
- Added Figure 9 to *Typical Characteristics*. 9
- Added *Application Information* section to data sheet. 17

5 Device Comparison Table

PART NUMBER	SIGNALING RATE	NODES	DUPLEX	ENABLES
SN65HVD72	Up to 250 kbps	213	Half	DE, $\overline{RE}$
SN65HVD75	Up to 20 Mbps			
SN65HVD78	Up to 50 Mbps	96		

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



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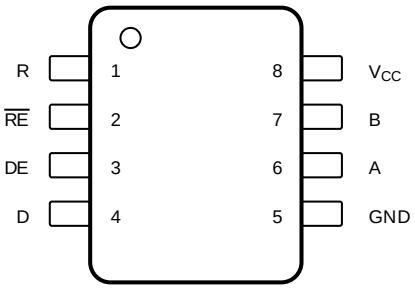
DGK Package
8-Pin VSSOP
Top View



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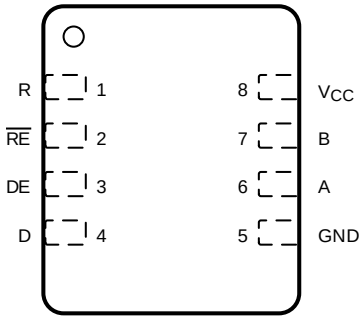
DRB Package
8-Pin VSON
Top View



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Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NUMBER		
A	6	Bus I/O	Driver output or receiver input (complementary to B)
B	7	Bus I/O	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-high driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Active-low receiver enable
V_{CC}	8	Supply	3-V to 3.6-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over recommended operating range (unless otherwise specified) (1)

	MIN	MAX	UNIT
Supply voltage, V_{CC}	–0.5	5	V
Voltage at A or B inputs	–13	16.5	
Voltage at D, DE, or $\overline{RE}$	–0.3	5.7	
Voltage input, transient pulse, A and B, through 100 Ω	–100	100	
Receiver output current	–24	24	mA
Junction temperature, T_J		170	°C
Continuous total power dissipation	See *Power Dissipation*		
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 or ANSI/ESDA/JEDEC JS-002, all pins(2)	±1500	
		JEDEC Standard 22, Test Method A115 (Machine Model), all pins	±300	
		IEC 61000-4-2 ESD (Air-Gap Discharge), bus pins and GND (3)	±12000	
		IEC 61000-4-2 ESD (Contact Discharge), bus pins and GND	±12000	
		IEC 61000-4-4 EFT (Fast transient or burst) bus pins and GND	±4000	
		IEC 60749-26 ESD (Human Body Model), bus pins and GND	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) By inference from contact discharge results, see *Application and Implementation*.

7.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}(1)	Supply voltage		3	3.3	3.6	V
V_I	Input voltage at any bus terminal (separately or common mode)(2)		–7		12	V
V_{IH}	High-level input voltage (driver, driver enable, and receiver enable inputs)		2		V_{CC}	V
V_{IL}	Low-level input voltage (driver, driver enable, and receiver enable inputs)		0		0.8	V
V_{ID}	Differential input voltage		–12		12	V
I_O	Output current, driver		–60		60	mA
I_O	Output current, receiver		–8		8	mA
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
$1/t_{UI}$	Signaling rate	SN65HVD72			250	kbps
		SN65HVD75			20	Mbps
		SN65HVD78			50	Mbps
T_A(3)	Operating free-air temperature (See *Thermal Information*)		–40		125	°C
T_J	Junction temperature		–40		150	°C

(1) Exposure to conditions beyond the recommended operation maximum for extended periods may affect device reliability.
(2) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet.
(3) Operation is specified for internal (junction) temperatures up to 150°C. Self-heating due to internal power dissipation should be considered for each application. Maximum junction temperature is internally limited by the thermal shutdown (TSD) circuit which disables the driver outputs when the junction temperature reaches 170°C.

7.4 Thermal Information

THERMAL METRIC[1]		SN65HVD72, SN65HVD75, SN65HVD78			UNIT
		D (SOIC)	DGK (VSSOP)	DRB (VSON)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	110.7	168.7	40	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.7	62.2	49.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	—	3.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	51.3	89.5	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	9.2	7.4	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	50.7	87.9	15.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
$\lvert V_{OD}\rvert$	Driver differential output voltage magnitude	R_L = 60 Ω, 375 Ω on each output to –7 V to 12 V	See Figure 10	1.5	2		V
		R_L = 54 Ω (RS-485)	See Figure 11	1.5	2		
		R_L = 100 Ω (RS-422), $T_J \geq 0°C$ $V_{CC} \geq 3.2$ V		2	2.5		
$\Delta\lvert V_{OD}\rvert$	Change in magnitude of driver differential output voltage	R_L = 54 Ω, C_L = 50 pF		–50	0	50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	Center of two 27-Ω load resistors		1	$V_{CC}/2$	3	V
ΔV_{OC}	Change in differential driver output common-mode voltage	Center of two 27-Ω load resistors		–50	0	50	mV
$V_{OC(PP)}$	Peak-to-peak driver common-mode output voltage	Center of two 27-Ω load resistors			200		mV
C_{OD}	Differential output capacitance				15		pF
V_{IT+}	Positive-going receiver differential input voltage threshold			See (1)	–70	–20	mV
V_{IT-}	Negative-going receiver differential input voltage threshold			–200	–150	See (1)	mV
V_{HYS}	Receiver differential input voltage threshold hysteresis ($V_{IT+} - V_{IT-}$)			50	80		mV
V_{OH}	Receiver high-level output voltage	I_{OH} = –8 mA		2.4	V_{CC} – 0.3		V
V_{OL}	Receiver low-level output voltage	I_{OL} = 8 mA			0.2	0.4	V
I_I	Driver input, driver enable, and receiver enable input current			–2		2	µA
I_{OZ}	Receiver output high-impedance current	V_O = 0 V or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	µA
I_{OS}	Driver short-circuit output current			–160		160	mA

(1) Under any specific conditions, V_{IT+} is assured to be at least V_{HYS} higher than V_{IT-}.

Electrical Characteristics (continued)

over recommended operating range (unless otherwise specified)

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
I_I	Bus input current (disabled driver)	V_{CC} = 3 to 3.6 V or V_{CC} = 0 V DE at 0 V	SN65HVD72 SN65HVD75	V_I = 12 V		75	150	µA
				V_I = –7 V	–100	–40		
			SN65HVD78	V_I = 12 V		240	333	
				V_I = –7 V	–267	–180		
I_{CC}	Supply current (quiescent)	Driver and receiver enabled	DE = V_{CC}, $\overline{RE}$ = GND No load			750	950	µA
		Driver enabled, receiver disabled	DE = V_{CC}, $\overline{RE}$ = V_{CC} No load			300	500	
		Driver disabled, receiver enabled	DE = GND, $\overline{RE}$ = GND No load			600	800	
		Driver and receiver disabled	$\overline{DE}$ = GND, D = open $\overline{RE}$ = V_{CC}, No load			0.1	2	
	Supply current (dynamic)	See *Typical Characteristics*						
T_{TSD}	Thermal shutdown junction temperature					170		°C

7.6 Power Dissipation

PARAMETER			TEST CONDITIONS		VALUE	UNIT
PD	Power Dissipation driver and receiver enabled, V_{CC} = 3.6 V, T_J = 150°C 50% duty cycle square-wave signal at signaling rate: • SN65HVD72 at 250 kbps • SN65HVD75 at 20 Mbps • SN65HVD78 at 50 Mbps	Unterminated	R_L = 300 Ω C_L = 50 pF (driver)	SN65HVD72	120	mW
				SN65HVD75	160	
				SN65HVD78	200	
		RS-422 load	R_L = 100 Ω C_L = 50 pF (driver)	SN65HVD72	155	mW
				SN65HVD75	195	
				SN65HVD78	230	
		RS-485 load	R_L = 54 Ω C_L = 50 pF (driver)	SN65HVD72	190	mW
				SN65HVD75	230	
				SN65HVD78	260	

7.7 Switching Characteristics: 250 kbps Device (SN65HVD72) Bit Time ≥ 4 µs

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω C_L = 50 pF	See Figure 12	0.3	0.7	1.2	µs
t_{PHL}, t_{PLH}	Driver propagation delay				0.7	1	µs
$t_{SK(P)}$	Driver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$					0.2	µs
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		0.1	0.4	µs
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			0.5	1	µs
		Receiver disabled			3	9	
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 15		12	30	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				75	100	ns
$t_{SK(P)}$	Receiver pulse skew, $\lvert t_{PHL} - t_{PLH} \rvert$				3	15	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				40	100	ns
$t_{PZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		20	50	ns
		Driver disabled	See Figure 17		3	8	µs

7.8 Switching Characteristics: 20 Mbps Device (SN65HVD75) Bit Time ≥50 ns

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 12	2	7	14	ns
t_{PHL}, t_{PLH}	Driver propagation delay			7	11	17	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				0	2	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		12	50	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	20	ns
		Receiver disabled			3	7	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 15		5	10	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time				60	70	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$				0	6	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				15	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		10	50	ns
		Driver disabled	See Figure 17		3	8	µs

7.9 Switching Characteristics: 50 Mbps Device (SN65HVD78) Bit Time ≥20 ns

over recommended operating conditions

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
DRIVER							
t_r, t_f	Driver differential output rise or fall time	R_L = 54 Ω, C_L = 50 pF	See Figure 12	1	3	6	ns
t_{PHL}, t_{PLH}	Driver propagation delay				9	15	ns
$t_{SK(P)}$	Driver pulse skew, $\|t_{PHL} - t_{PLH}\|$				0	1	ns
t_{PHZ}, t_{PLZ}	Driver disable time		See Figure 13 and Figure 14		10	30	ns
t_{PZH}, t_{PZL}	Driver enable time	Receiver enabled			10	30	ns
		Receiver disabled				8	µs
RECEIVER							
t_r, t_f	Receiver output rise or fall time	C_L = 15 pF	See Figure 15	1	3	6	ns
t_{PHL}, t_{PLH}	Receiver propagation delay time					35	ns
$t_{SK(P)}$	Receiver pulse skew, $\|t_{PHL} - t_{PLH}\|$					2.5	ns
t_{PLZ}, t_{PHZ}	Receiver disable time				8	30	ns
$t_{pZL(1)}$, $t_{PZH(1)}$, $t_{PZL(2)}$, $t_{PZH(2)}$	Receiver enable time	Driver enabled	See Figure 16		10	30	ns
		Driver disabled	See Figure 17		3	8	µs

7.10 Typical Characteristics

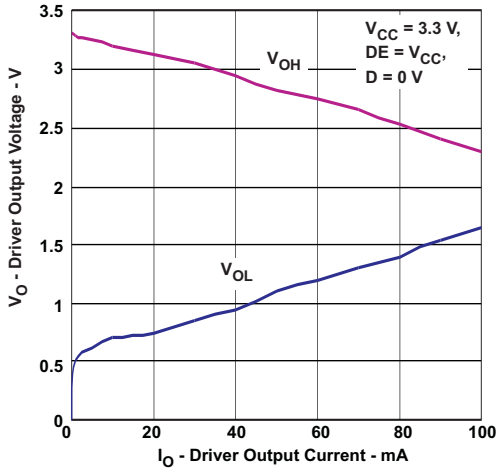


Figure 1. Driver Output Voltage vs Driver Output Current

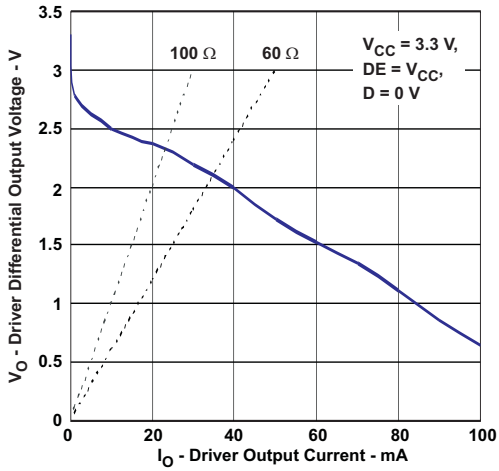


Figure 2. Driver Differential Output Voltage vs Driver Output Current

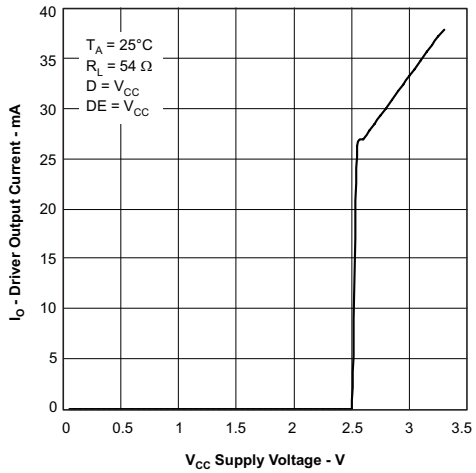


Figure 3. Driver Output Current vs Supply Voltage

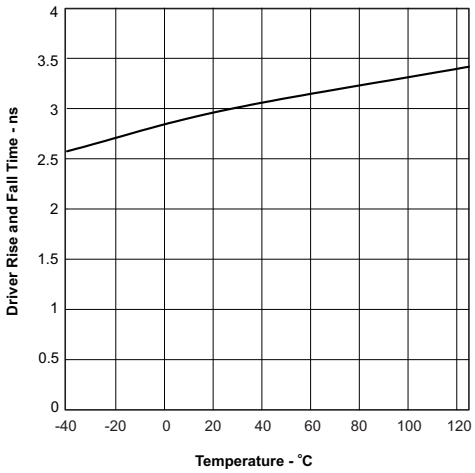


Figure 4. SN65HVD78 Driver Rise or Fall Time vs Temperature

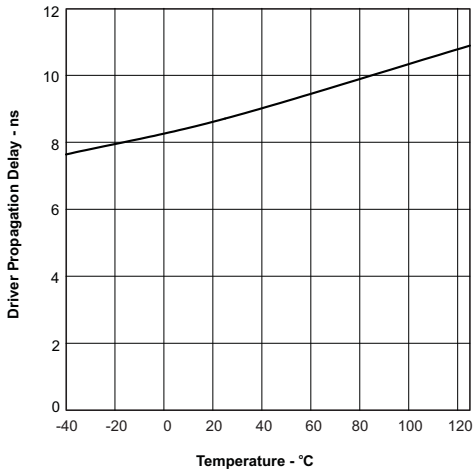


Figure 5. SN65HVD78 Driver Propagation Delay vs Temperature

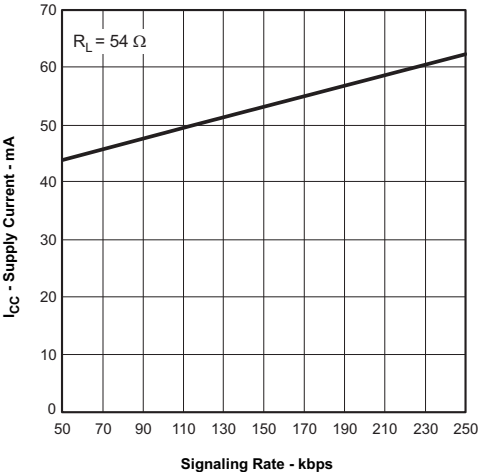


Figure 6. SN65HVD72 Supply Current vs Signal Rate

Typical Characteristics (continued)

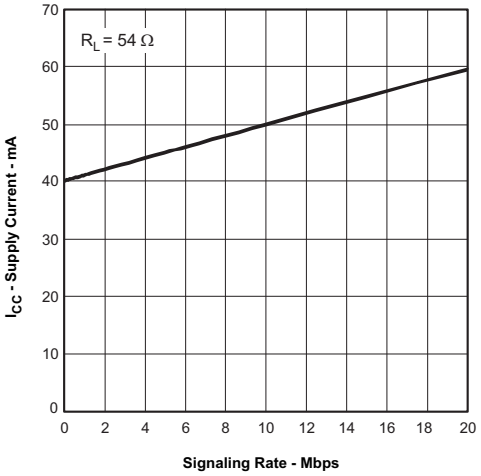


Figure 7. SN65HVD75 Supply Current vs Signal Rate

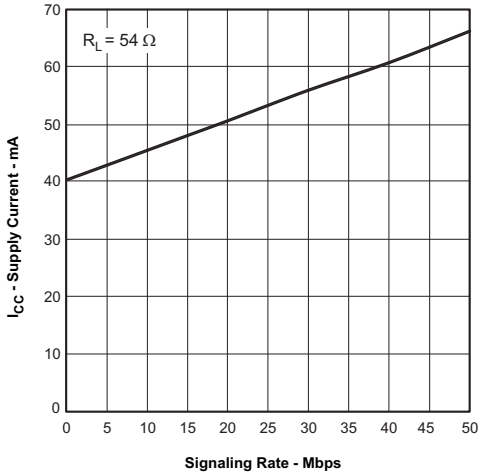


Figure 8. SN65HVD78 Supply Current vs Signal Rate

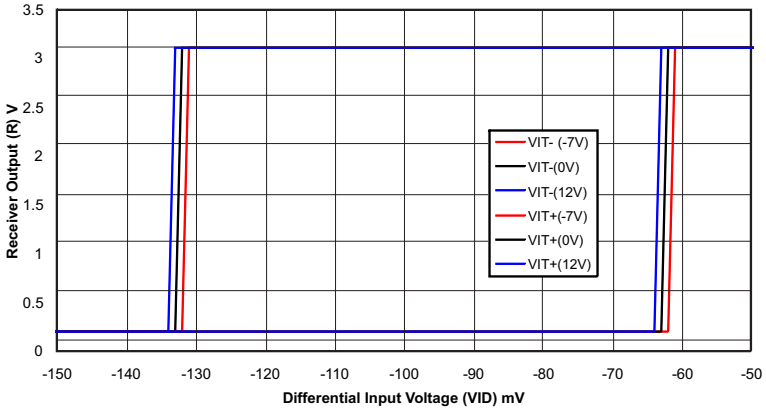


Figure 9. Receiver Output vs Input

8 Parameter Measurement Information

Input generator rate is 100 kbps, 50% duty cycle, rise or fall time is less than 6 ns, output impedance is 50 Ω.

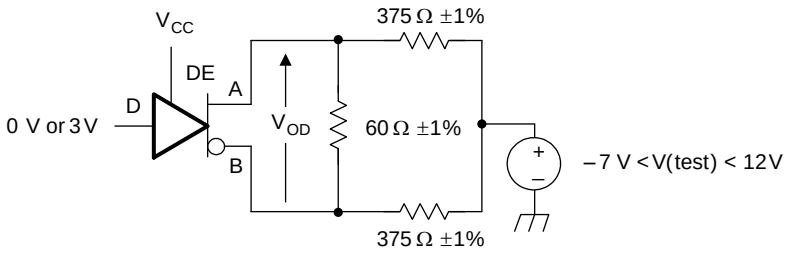


Figure 10. Measurement of Driver Differential Output Voltage With Common-Mode Load

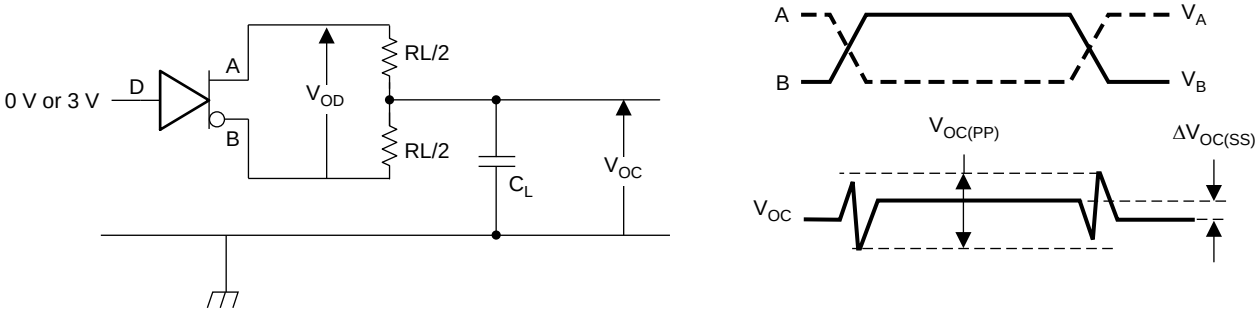


Figure 11. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

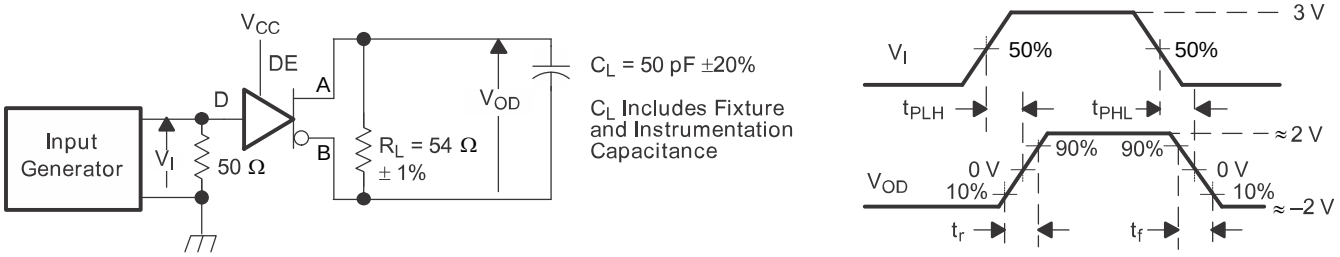
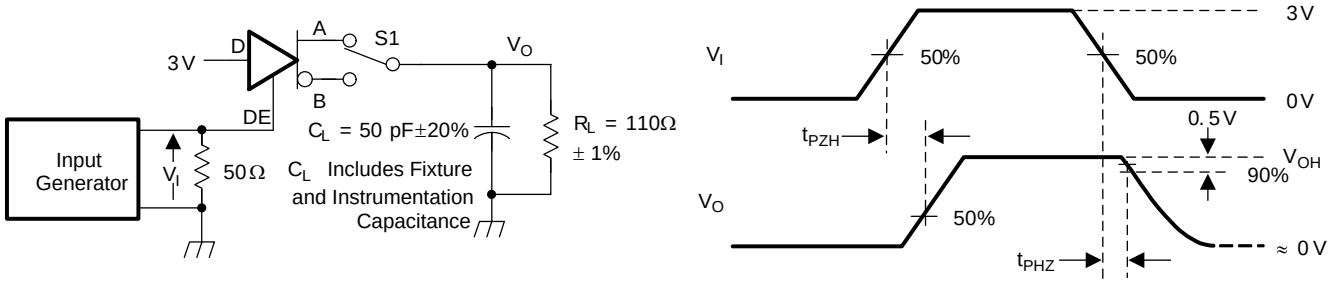


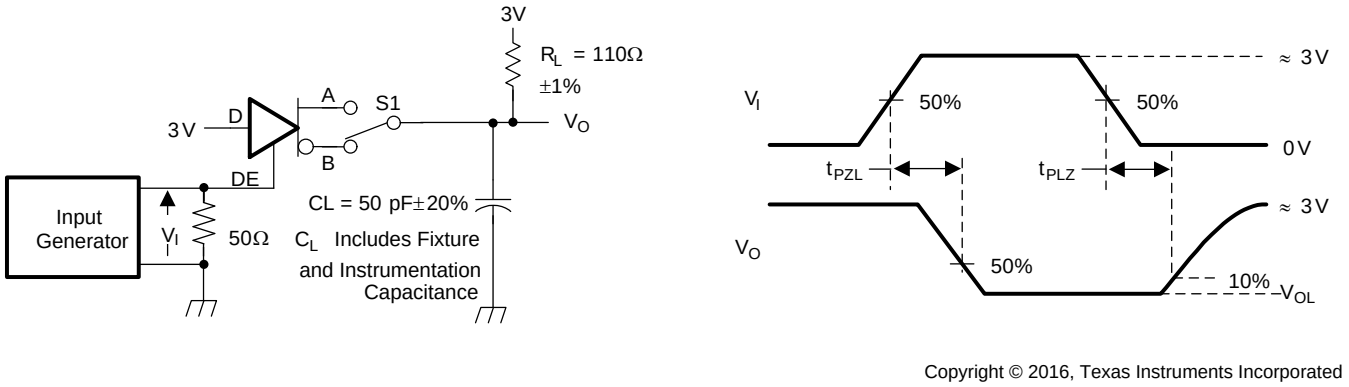
Figure 12. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays



D at 3 V to test non-inverting output, D at 0 V to test inverting output.

Figure 13. Measurement of Driver Enable and Disable Times With Active High Output and Pulldown Load

Parameter Measurement Information (continued)



D at 0 V to test non-inverting output, D at 3 V to test inverting output.

Figure 14. Measurement of Driver Enable and Disable Times With Active Low Output and Pullup Load

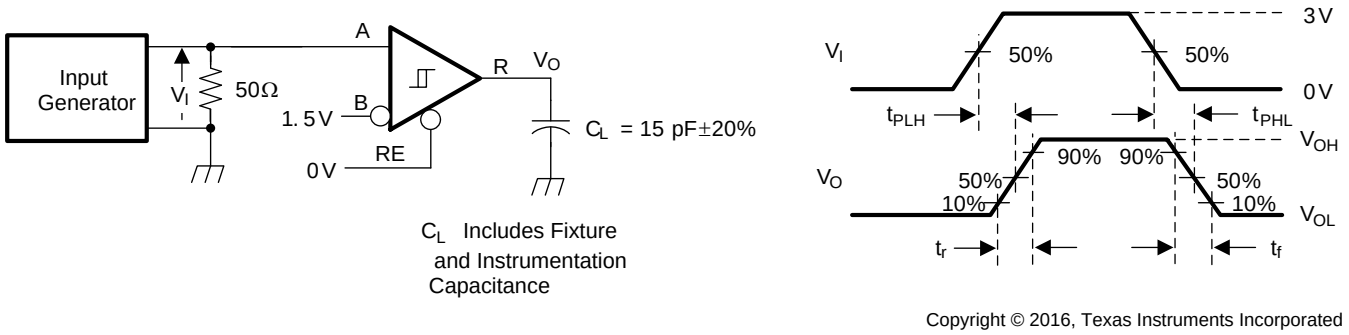


Figure 15. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

Parameter Measurement Information (continued)

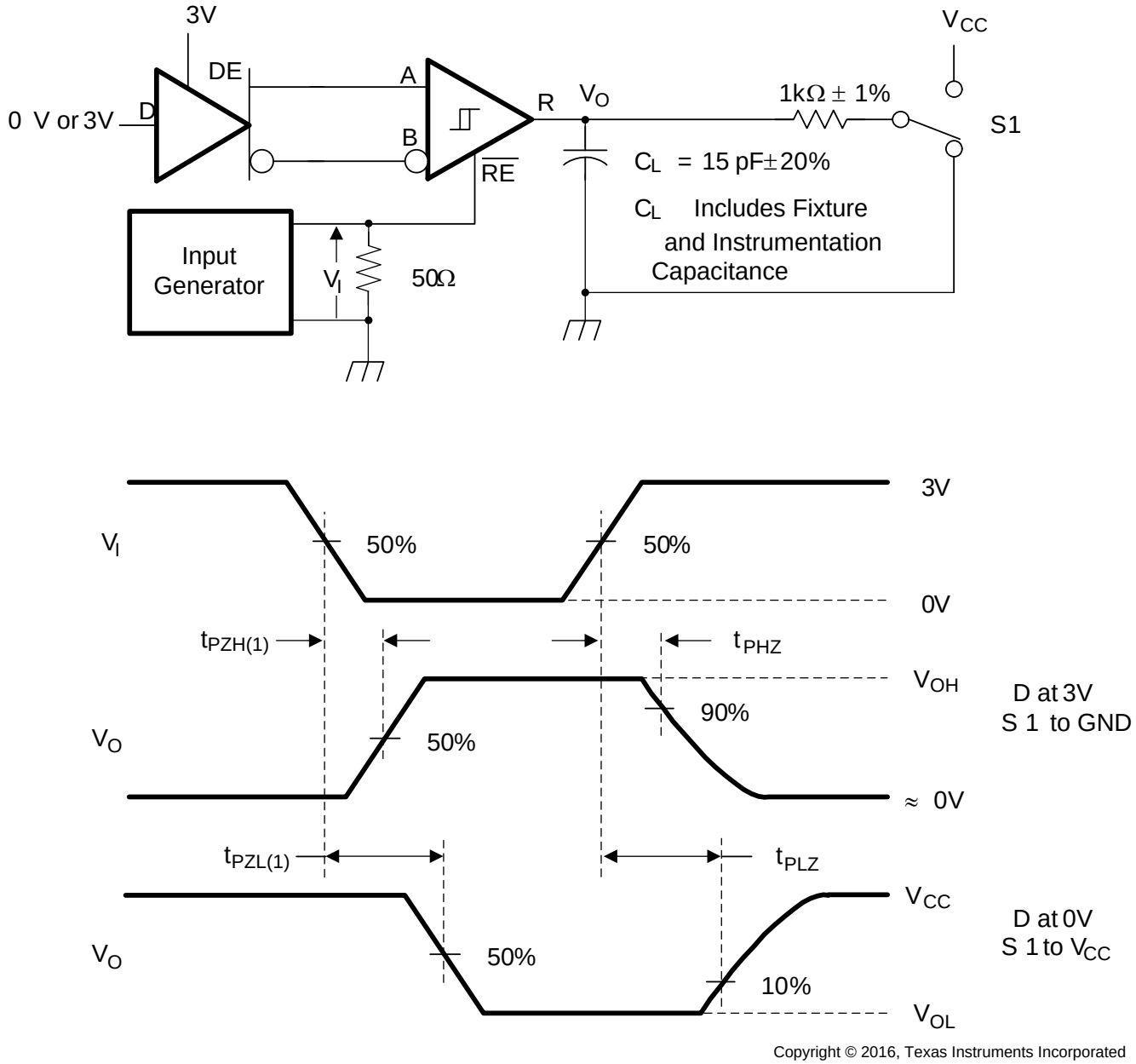


Figure 16. Measurement of Receiver Enable and Disable Times With Driver Enabled

Parameter Measurement Information (continued)

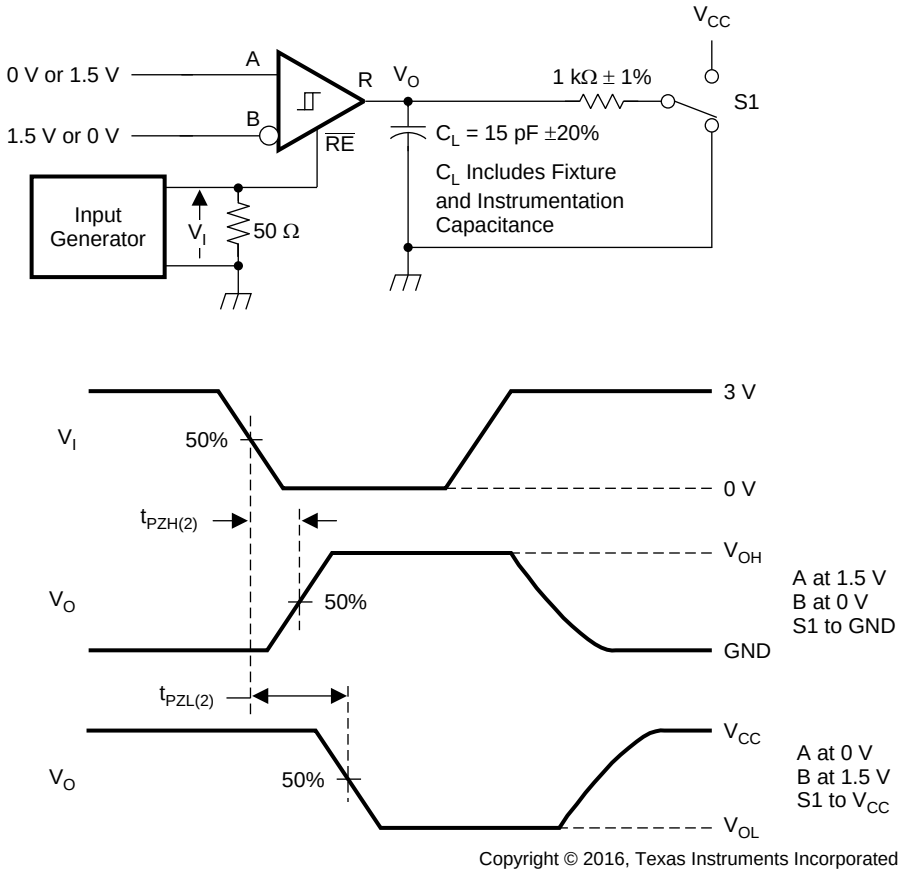


Figure 17. Measurement of Receiver Enable Times With Driver Disabled

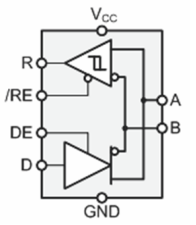
9 Detailed Description

9.1 Overview

The SN65HVD72, SN65HVD75, and SN65HVD78 are low-power, half-duplex RS-485 transceivers available in 3 speed grades suitable for data transmission up to 250 kbps, 20 Mbps, and 50 Mbps.

These devices have active-high driver enables and active-low receiver enables. A standby current of less than 2 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



9.3 Feature Description

Internal ESD protection circuits protect the transceiver against electrostatic discharges (ESD) according to IEC 61000-4-2 of up to ±12 kV, and against electrical fast transients (EFT) according to IEC 61000-4-4 of up to ±4 kV.

The SN65HVD7x half-duplex family provides internal biasing of the receiver input thresholds in combination with large input threshold hysteresis. At a positive input threshold of V_{IT+} = –20 mV and an input hysteresis of V_{HYS} = 50 mV, the receiver output remains logic high under a bus-idle or bus-short condition even in the presence of 140-mV_{PP} differential noise without the need for external failsafe biasing resistors.

Device operation is specified over a wide ambient temperature range from –40°C to 125°C.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case the differential output voltage defined as $V_{OD} = V_A – V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; thus, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}; thus, when left open while the driver is enabled, output A turns high and B turns low.

Table 1. Driver Function Table

INPUT	ENABLE	OUTPUTS		DESCRIPTION
D	DE	A	B	
H	H	H	L	Actively drive bus high
L	H	L	H	Actively drive bus low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus high by default

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or the bus is not actively driven (idle bus).

Table 2. Receiver Function Table

DIFFERENTIAL INPUT	ENABLE	OUTPUT	DESCRIPTION
$V_{ID} = V_A - V_B$	$\overline{RE}$	R	
$V_{IT+} < V_{ID}$	L	H	Receive valid bus high
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Failsafe high output
Short-circuit bus	L	H	Failsafe high output
Idle (terminated) bus	L	H	Failsafe high output

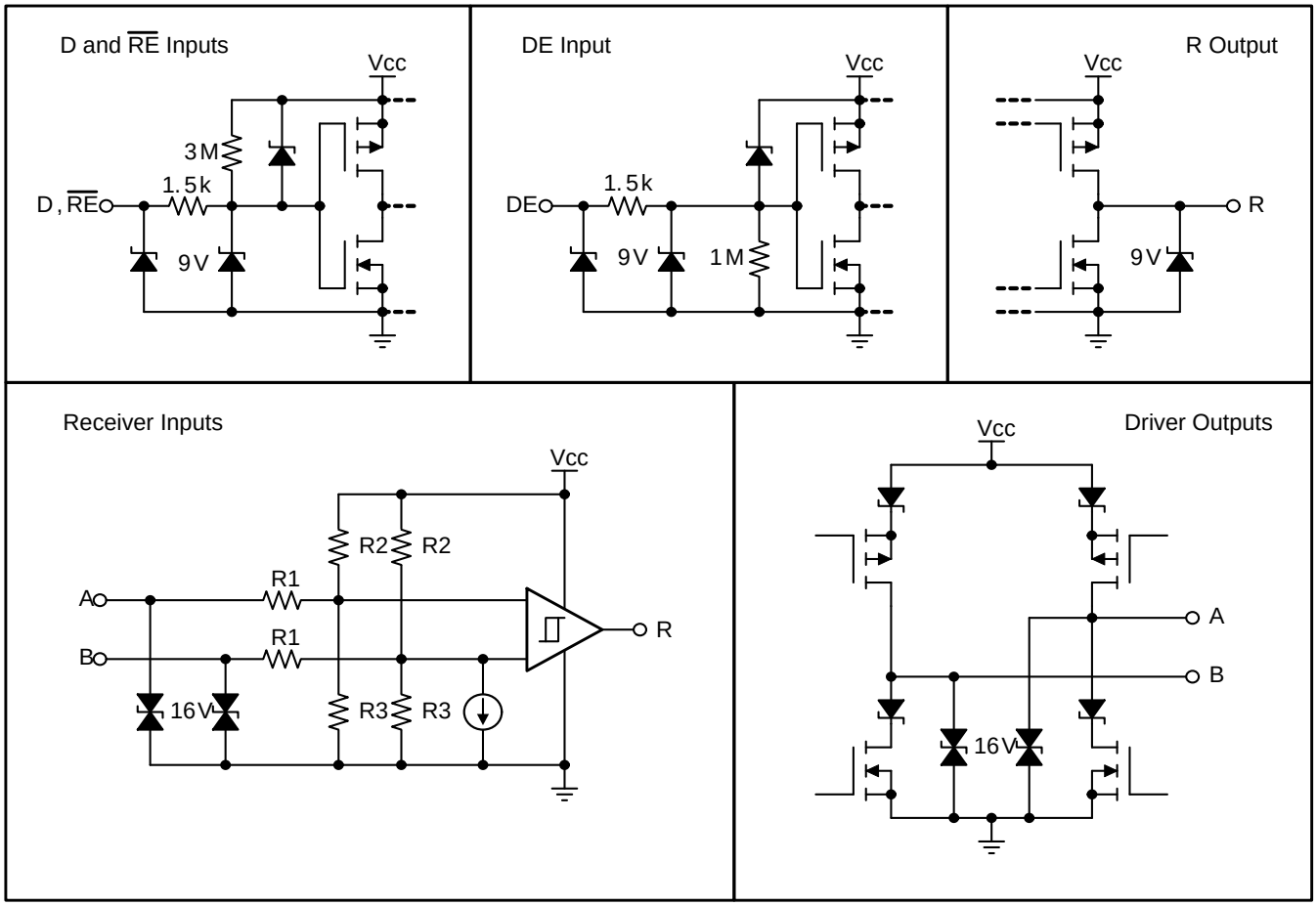


Figure 18. Equivalent Input and Output Circuit Diagrams

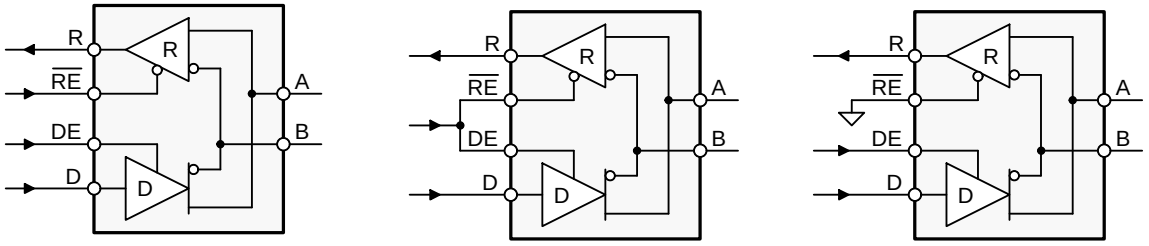
10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The SN65HVD72, SN65HVD75, and SN65HVD78 are half-duplex RS-485 transceivers commonly used for asynchronous data transmission. The driver and receiver enable pins allow for the configuration of different operating modes.



a) Independent driver and receiver enable signals

b) Combined enable signals for use as directional control pin

c) Receiver always on

Figure 19. Transceiver Configurations

Using independent enable lines provides the most flexible control as it allows for the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows for relatively high data rates over long cable lengths.

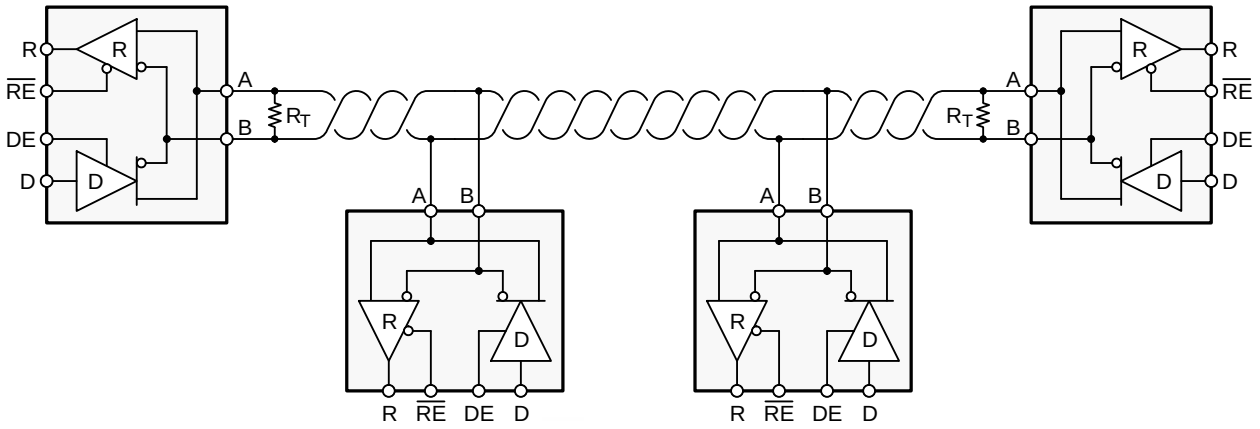


Figure 20. Typical RS-485 Network With SN65HVD7x Transceivers

Common cables used are unshielded twisted pair (UTP), such as low-cost CAT-5 cable with Z_0 = 100 Ω, and RS-485 cable with Z_0 = 120 Ω. Typical cable sizes are AWG 22 and AWG 24.

The maximum bus length is typically given as 4000 ft or 1200 m, and represents the length of an AWG 24 cable whose cable resistance approaches the value of the termination resistance, thus reducing the bus signal by half or 6 dB. Actual maximum usable cable length depends on the signaling rate, cable characteristics, and environmental conditions.

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

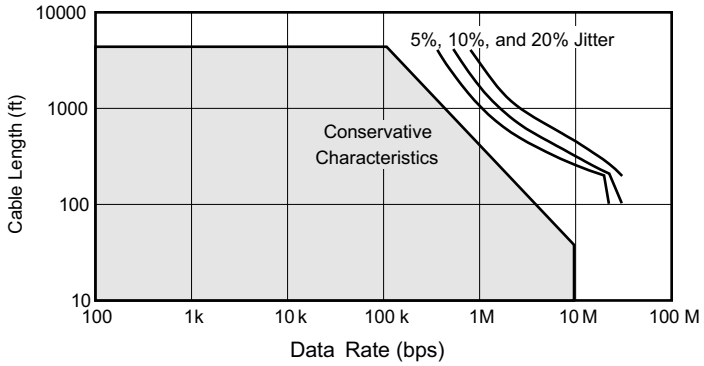


Figure 21. Cable Length vs Data Rate Characteristic

Typical Application (continued)

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a non-terminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in Equation 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

- t_r is the 10/90 rise time of the driver
- c is the speed of light (3×10^8 m/s)
- v is the signal velocity of the cable or trace as a factor of c

Per Equation 1, Table 3 shows the maximum cable-stub lengths for the minimum driver output rise times of the SN65HVD7x half-duplex family of transceivers for a signal velocity of 78%.

Table 3. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD72	300	7	23
SN65HVD75	2	0.05	0.16
SN65HVD78	1	0.025	0.08

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to drive 32 unit loads (UL), where 1 unit load represents a receiver input current of 1 mA at 12 V, or a load impedance of approximately 12 kΩ. Because the SN65HVD72 and SN65HVD75 have a receiver input current of 150 µA at 12 V, they are 3/20 UL transceivers, and no more than 213 transceivers should be connected to the bus. Similarly, the SN65HVD78 has a receiver input current of 333 µA at 12 V and is a 1/3 UL transceiver, meaning no more than 96 transceivers should be connected to the bus.

10.2.1.4 Receiver Failsafe

The differential receiver is failsafe to invalid bus states caused by:

- Open bus conditions such as a disconnected connector
- Shorted bus conditions such as cable damage shorting the twisted-pair together, or
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic high so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input-indeterminate range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input V_{ID} is more positive than 200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the failsafe performance are V_{IT+}, V_{IT-}, and V_{HYS} (the separation between V_{IT+} and V_{IT-}). As shown in *Electrical Characteristics*, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than 200 mV will always cause a high receiver output.

When the differential input signal is close to zero, it is still above the maximum V_{IT+} threshold of –20 mV, and the receiver output will be high. Only when the differential input is more than V_{HYS} below V_{IT+} will the receiver output transition to a low state. Therefore, the noise immunity of the receiver inputs during a bus fault condition includes the receiver hysteresis value, V_{HYS}, as well as the value of V_{IT+}.

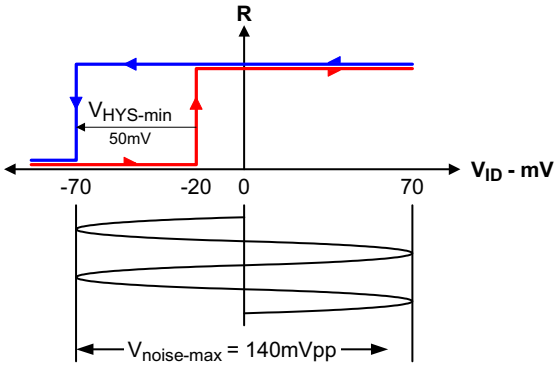


Figure 22. SN65HVD7x Noise Immunity

10.2.1.5 Transient Protection

The bus pins of the SN65HVD7x transceiver family possess on-chip ESD protection against ±15-kV human body model (HBM) and ±12-kV IEC 61000-4-2 contact discharge. The IEC-ESD test is far more severe than the HBM-ESD test. The 50% higher charge capacitance, C_S, and 78% lower discharge resistance, R_D, of the IEC-model produce significantly higher discharge currents than the HBM-model.

As stated in the IEC 61000-4-2 standard, contact discharge is the preferred test method; although IEC air-gap testing is less repeatable than contact testing, air discharge protection levels are inferred from the contact discharge test results.

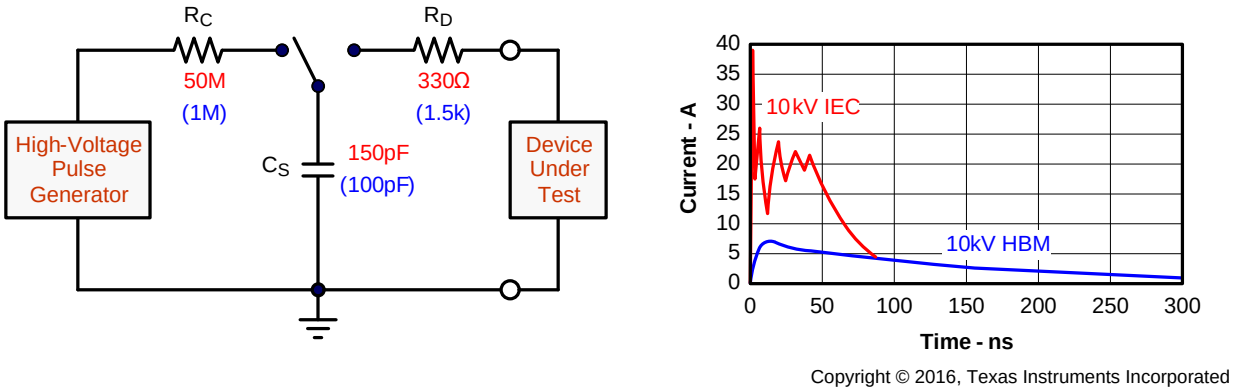


Figure 23. HBM and IEC-ESD Models and Currents in Comparison (HBM Values in Parenthesis)

The on-chip implementation of IEC ESD protection significantly increases the robustness of equipment. Common discharge events occur due to human contact with connectors and cables. Designers may choose to implement protection against longer duration transients, typically referred to as surge transients.

EFTs are generally caused by relay-contact bounce or the interruption of inductive loads. Surge transients often result from lightning strikes (direct strike or an indirect strike which induce voltages and currents), or the switching of power systems, including load changes and short circuit switching. These transients are often encountered in industrial environments, such as factory automation and power-grid systems.

Figure 24 compares the pulse-power of the EFT and surge transients with the power caused by an IEC ESD transient. The left-hand diagram shows the relative pulse-power for a 0.5-kV surge transient and 4-kV EFT transient, both of which dwarf the 10-kV ESD transient visible in the lower-left corner. 500-V surge transients are representative of events that may occur in factory environments in industrial and process automation.

The right-hand diagram shows the pulse-power of a 6-kV surge transient, relative to the same 0.5-kV surge transient. 6-kV surge transients are most likely to occur in power generation and power-grid systems.

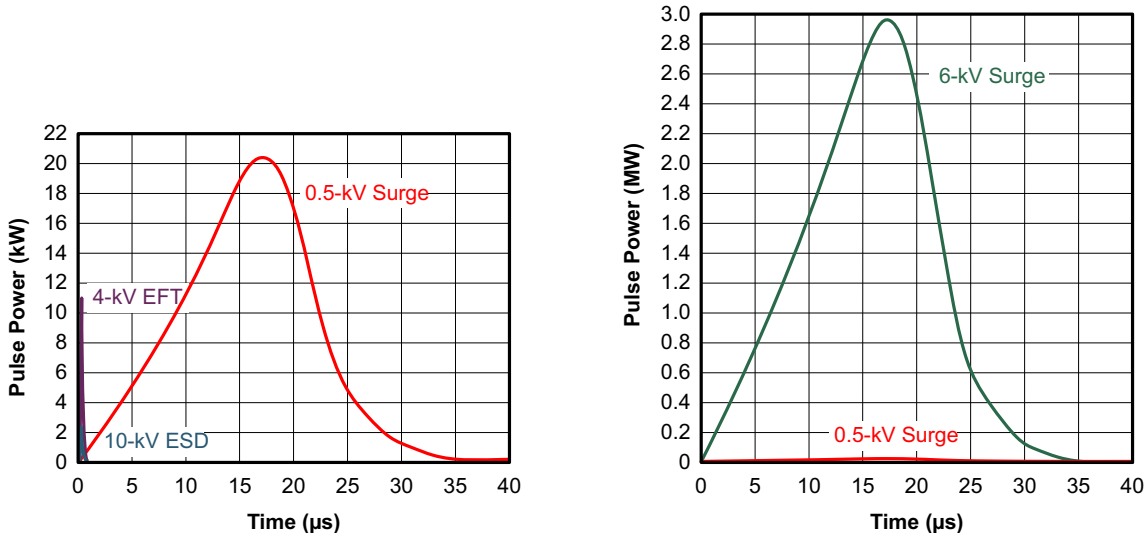


Figure 24. Power Comparison of ESD, EFT, and Surge Transients

In the case of surge transients, high-energy content is characterized by long pulse duration and slow decaying pulse power. The electrical energy of a transient that is dumped into the internal protection cells of a transceiver is converted into thermal energy which heats and destroys the protection cells, thus destroying the transceiver. Figure 25 shows the large differences in transient energies for single ESD, EFT, and surge transients, as well as for an EFT pulse train, commonly applied during compliance testing.

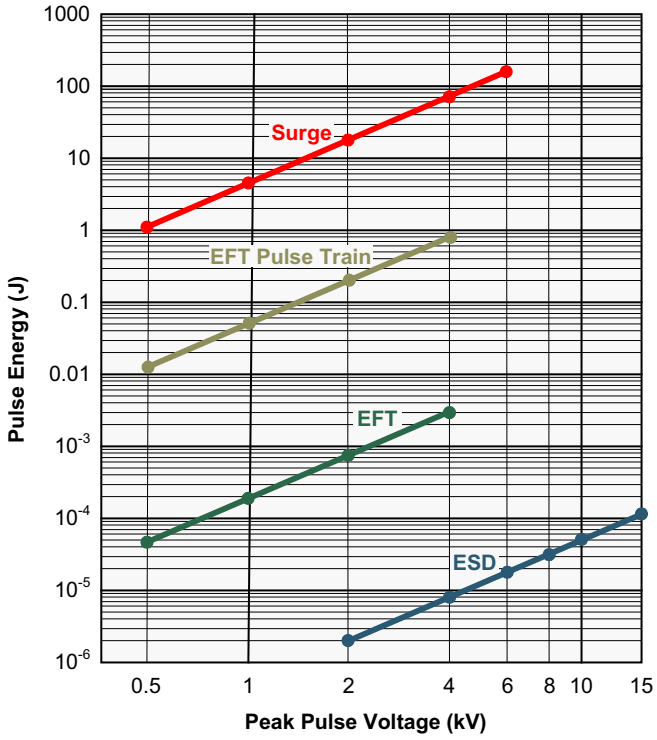


Figure 25. Comparison of Transient Energies

10.2.2 Detailed Design Procedure

10.2.2.1 External Transient Protection

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary. Figure 26 suggests two circuits that provide protection against light and heavy surge transients, in addition to ESD and EFT transients. Table 4 presents the associated bill of materials.

Table 4. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V, 250-kbps RS-485 Transceiver	SN65HVD72D	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW060310RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns
TBU1, TBU2	Bidirectional Surge Suppressor	TBU-CA-065-200-WH	Bourns
MOV1, MOV2	200-mA Transient Blocking Unit, 200-V, Metal-Oxide Varistor	MOV-10D201K	Bourns

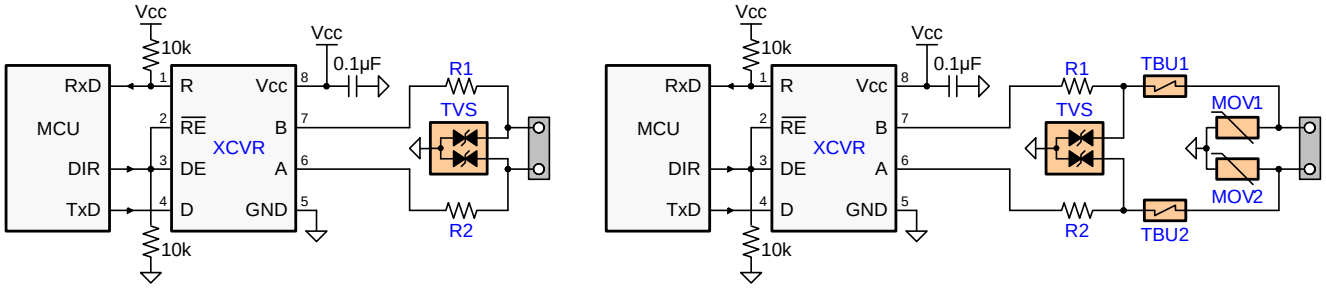


Figure 26. Transient Protections Against ESD, EFT, and Surge Transients

The left-hand circuit provides surge protection of ≥500-V surge transients, while the right-hand circuit can withstand surge transients of up to 5 kV.

10.2.2.2 Isolated Bus Node Design

Many RS-485 networks use isolated bus nodes to prevent the creation of unintended ground loops and their disruptive impact on signal integrity. An isolated bus node typically includes a microcontroller that connects to the bus transceiver via a multi-channel, digital isolator (Figure 27).

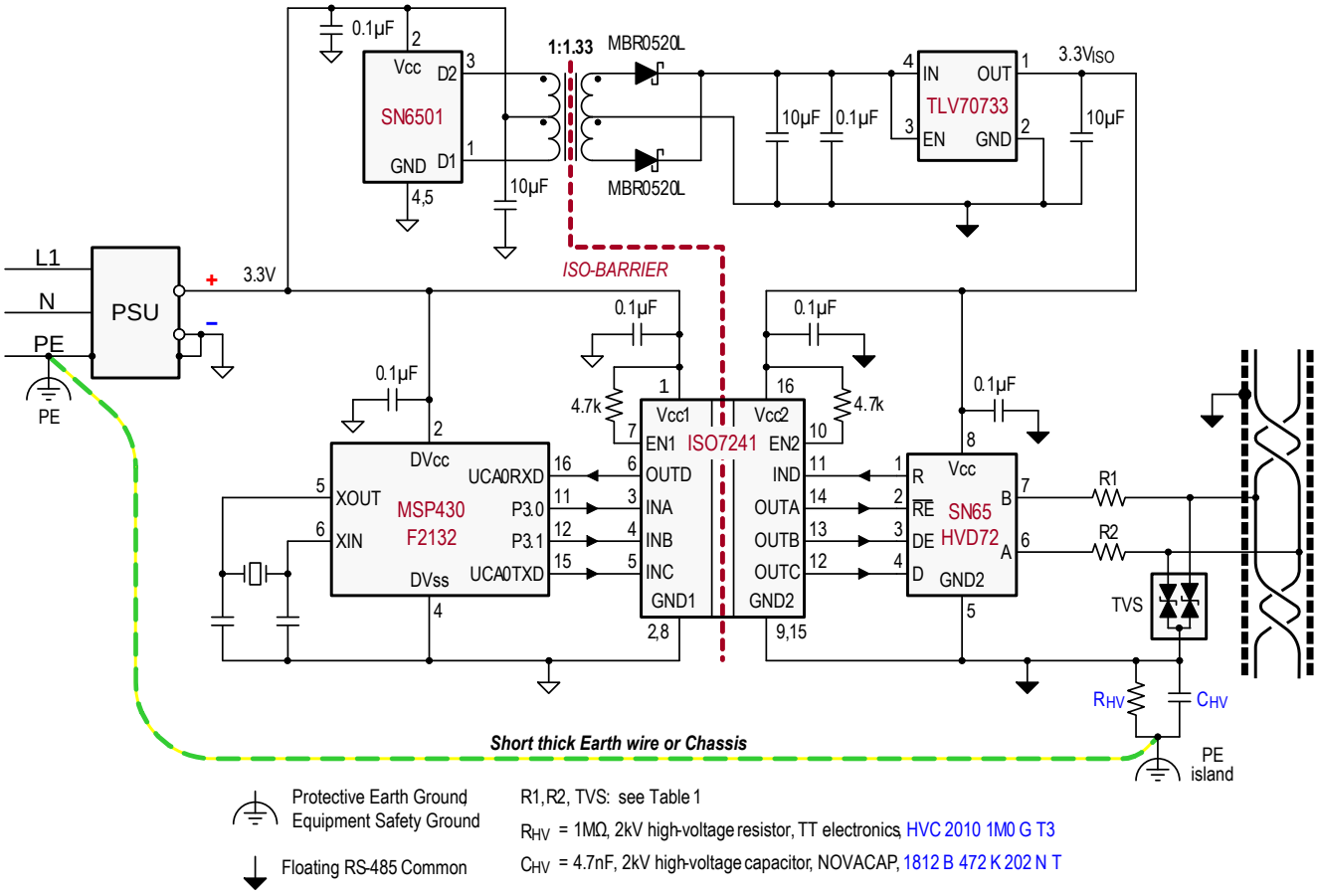


Figure 27. Isolated Bus Node with Transient Protection

Power isolation is accomplished using the push-pull transformer driver SN6501 and a low-cost LDO, TLV70733.

Signal isolation uses the quadruple digital isolator ISO7241. Notice that both enable inputs, EN_1 and EN_2, are pulled up via 4.7 kΩ resistors to limit their input currents during transient events.

While the transient protection is similar to the one in Figure 26 (left circuit), an additional high-voltage capacitor is used to divert transient energy from the floating RS-485 common further towards Protective Earth (PE) ground. This is necessary as noise transients on the bus are usually referred to Earth potential.

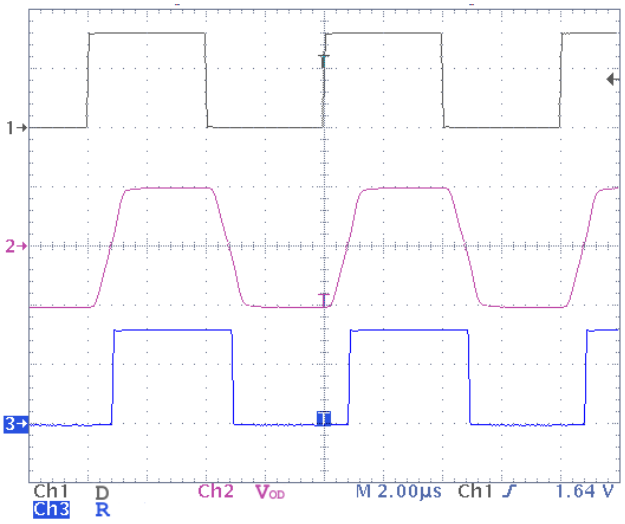
R_{HV} refers to a high voltage resistor, and in some applications even a varistor. This resistance is applied to prevent charging of the floating ground to dangerous potentials during normal operation.

Occasionally varistors are used instead of resistors to rapidly discharge C_{HV}, if it is expected that fast transients might charge C_{HV} to high-potentials.

Note that the PE island represents a copper island on the PCB for the provision of a short, thick Earth wire connecting this island to PE ground at the entrance of the power supply unit (PSU).

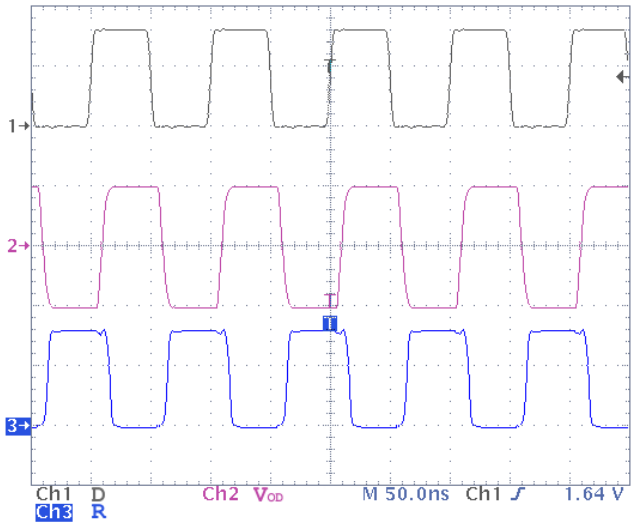
In equipment designs using a chassis, the PE connection is usually provided through the chassis itself. Typically the PE conductor is tied to the chassis at one end while the high-voltage components, C_{HV} and R_{HV}, are connecting to the chassis at the other end.

10.2.3 Application Curves



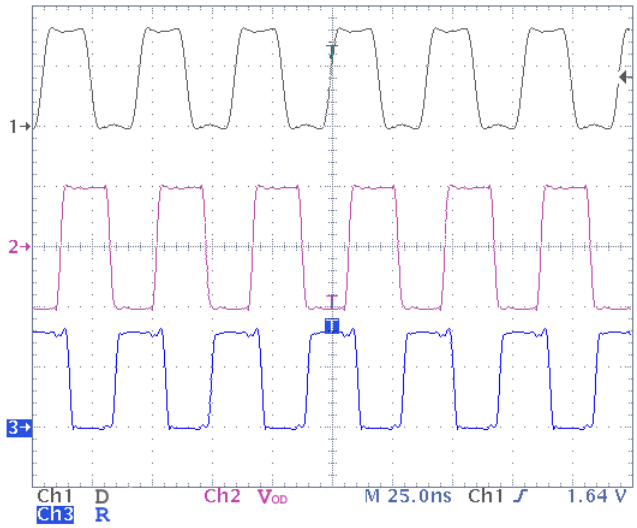
R_L = 60 Ω

Figure 28. SN65HVD72, 250 kbps



R_L = 60 Ω

Figure 29. SN65HVD75, 20 Mbps



R_L = 60 Ω

Figure 30. SN65HVD78, 50 Mbps

11 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply should be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 is a linear voltage regulator suitable for the 3.3 V supply.

See the SN6501 data sheet for isolated power supply designs.

12 Layout

12.1 Layout Guidelines

On-chip IEC ESD protection is sufficient for laboratory and portable equipment but often insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high-frequency layout techniques must be applied during PCB design.

For a successful PCB design, start with the design of the protection circuit in mind.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transients currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pullup or pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof series resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus pins. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to 200 mA.

12.2 Layout Example

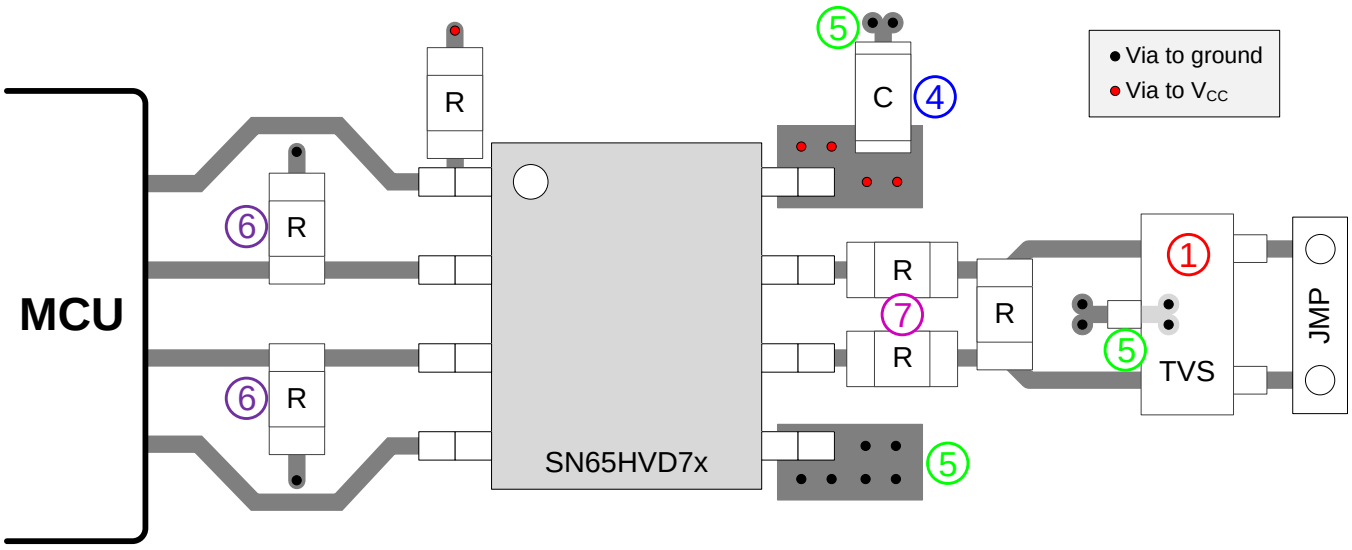


Figure 31. SN65HVD7x Half-Duplex Layout Example

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

SN6501 Transformer Driver for Isolated Power Supplies, SLLSEA0

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 5. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD72	Click here	Click here	Click here	Click here	Click here
SN65HVD75	Click here	Click here	Click here	Click here	Click here
SN65HVD78	Click here	Click here	Click here	Click here	Click here

13.4 Community Resources

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD72D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD72	Samples
SN65HVD72DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD72	Samples
SN65HVD72DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD72	Samples
SN65HVD75D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG | SN	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD75	Samples
SN65HVD75DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD75	Samples
SN65HVD75DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD75	Samples
SN65HVD78D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DGK	ACTIVE	VSSOP	DGK	8	80	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HVD78	Samples
SN65HVD78DRBR	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD78	Samples
SN65HVD78DRBT	ACTIVE	SON	DRB	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	HVD78	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

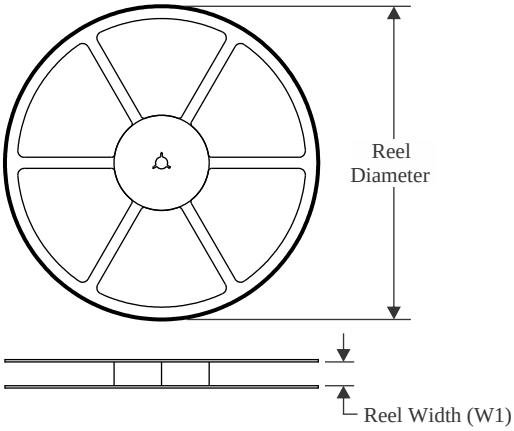
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

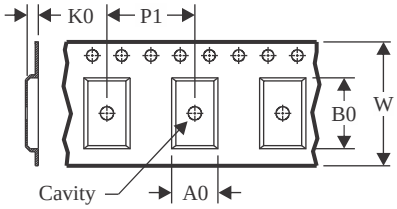
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

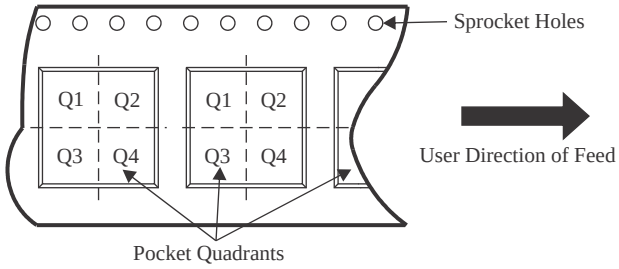


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

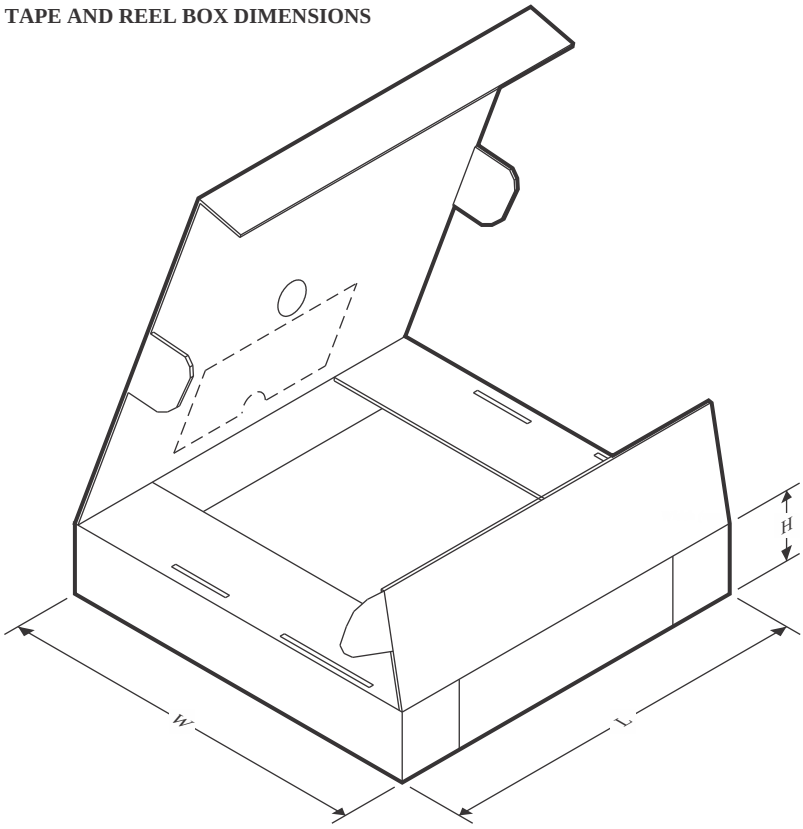
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD72DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD72DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD72DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD72DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD72DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD75DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD75DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD75DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD75DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD75DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD78DGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD78DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD78DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
SN65HVD78DRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

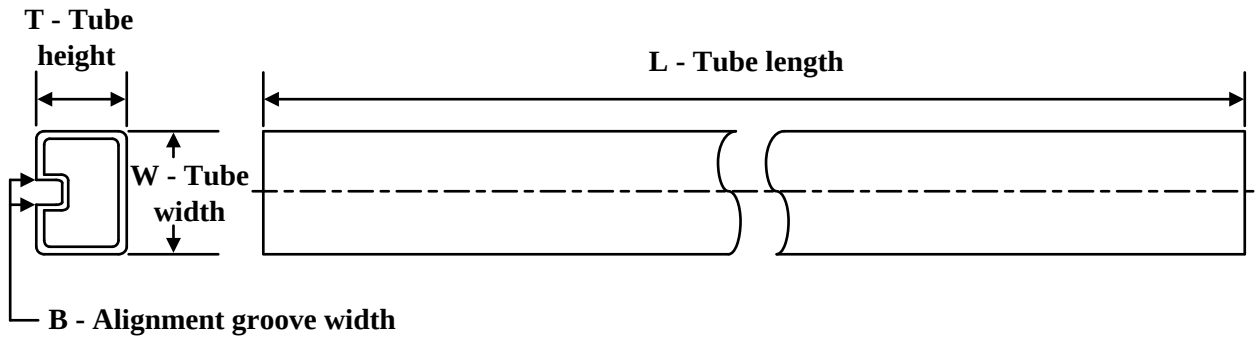
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD72DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD72DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
SN65HVD72DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD72DRBR	SON	DRB	8	3000	346.0	346.0	33.0
SN65HVD72DRBT	SON	DRB	8	250	210.0	185.0	35.0
SN65HVD75DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD75DGKR	VSSOP	DGK	8	2500	366.0	364.0	50.0
SN65HVD75DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD75DRBR	SON	DRB	8	3000	346.0	346.0	33.0
SN65HVD75DRBT	SON	DRB	8	250	210.0	185.0	35.0
SN65HVD78DGKR	VSSOP	DGK	8	2500	364.0	364.0	27.0
SN65HVD78DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD78DRBR	SON	DRB	8	3000	346.0	346.0	33.0
SN65HVD78DRBT	SON	DRB	8	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD72D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD72DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
SN65HVD75D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD75DGK	DGK	VSSOP	8	80	330	6.55	500	2.88
SN65HVD78D	D	SOIC	8	75	506.6	8	3940	4.32
SN65HVD78DGK	DGK	VSSOP	8	80	330	6.55	500	2.88

GENERIC PACKAGE VIEW

DRB 8

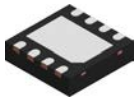
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203482/L

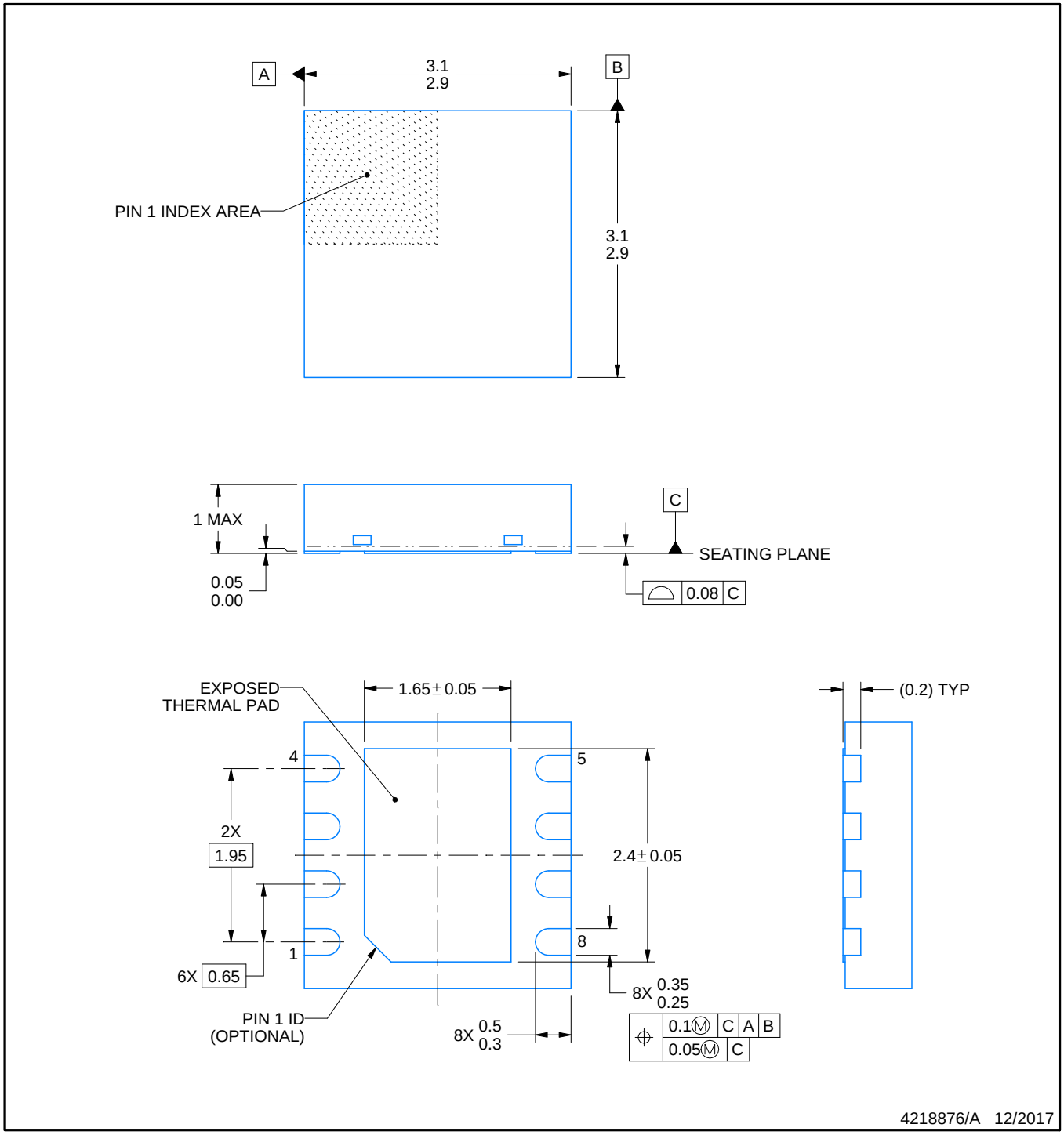
DRB0008B



PACKAGE OUTLINE

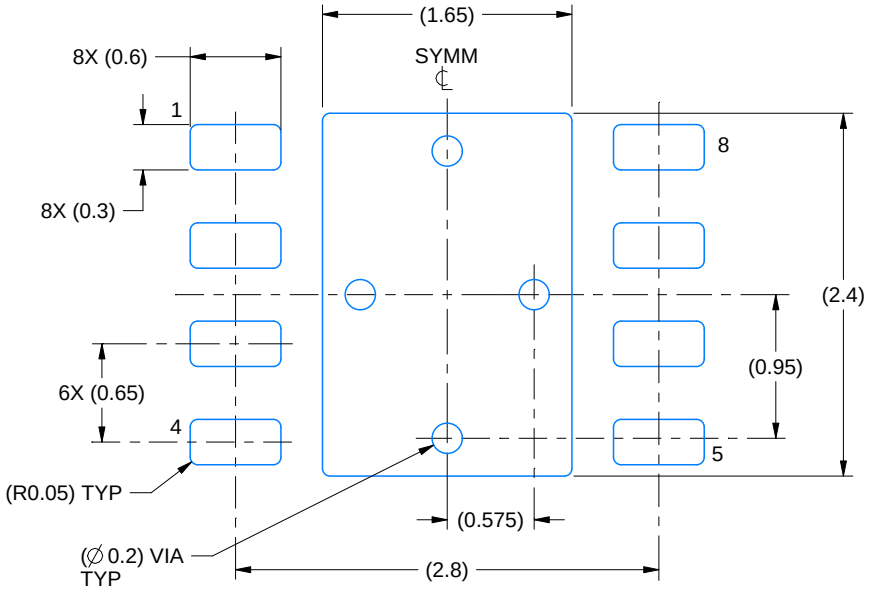
VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

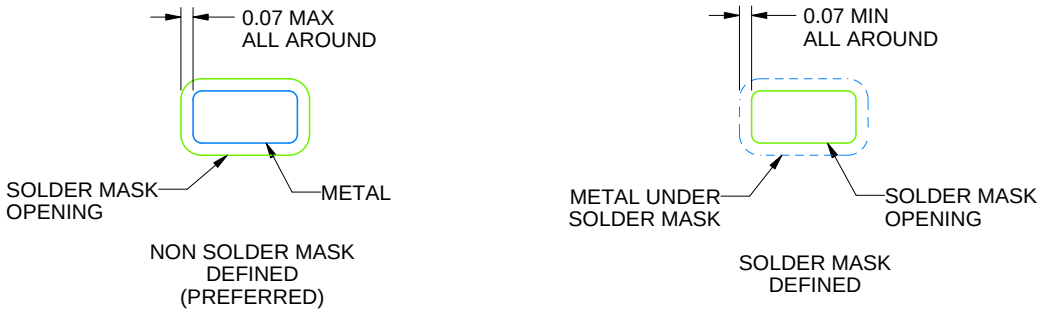


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

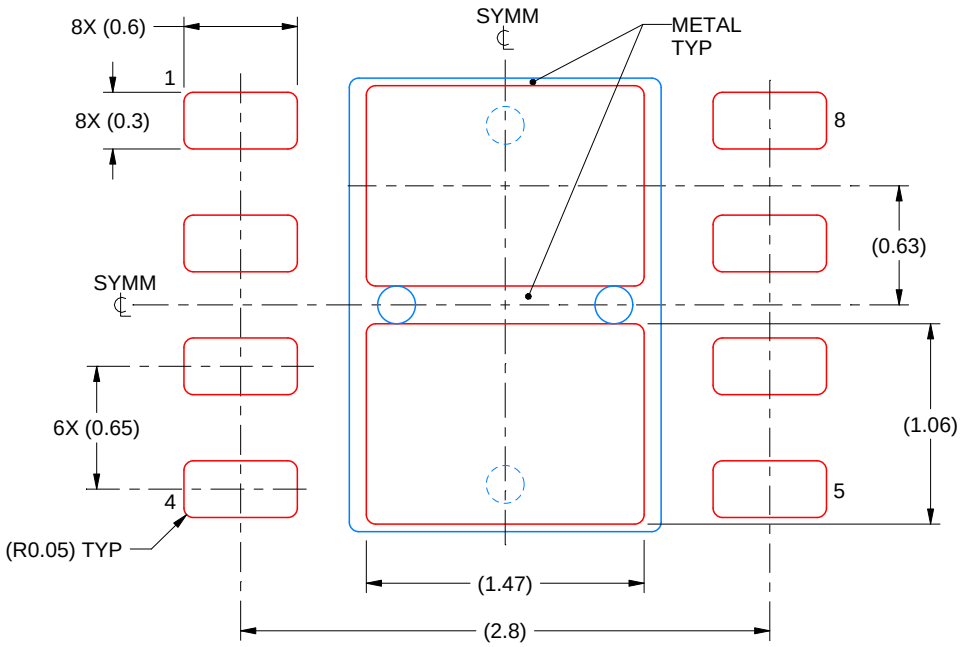


SOLDER MASK DETAILS

4218876/A 12/2017

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



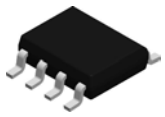
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
81% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218876/A 12/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

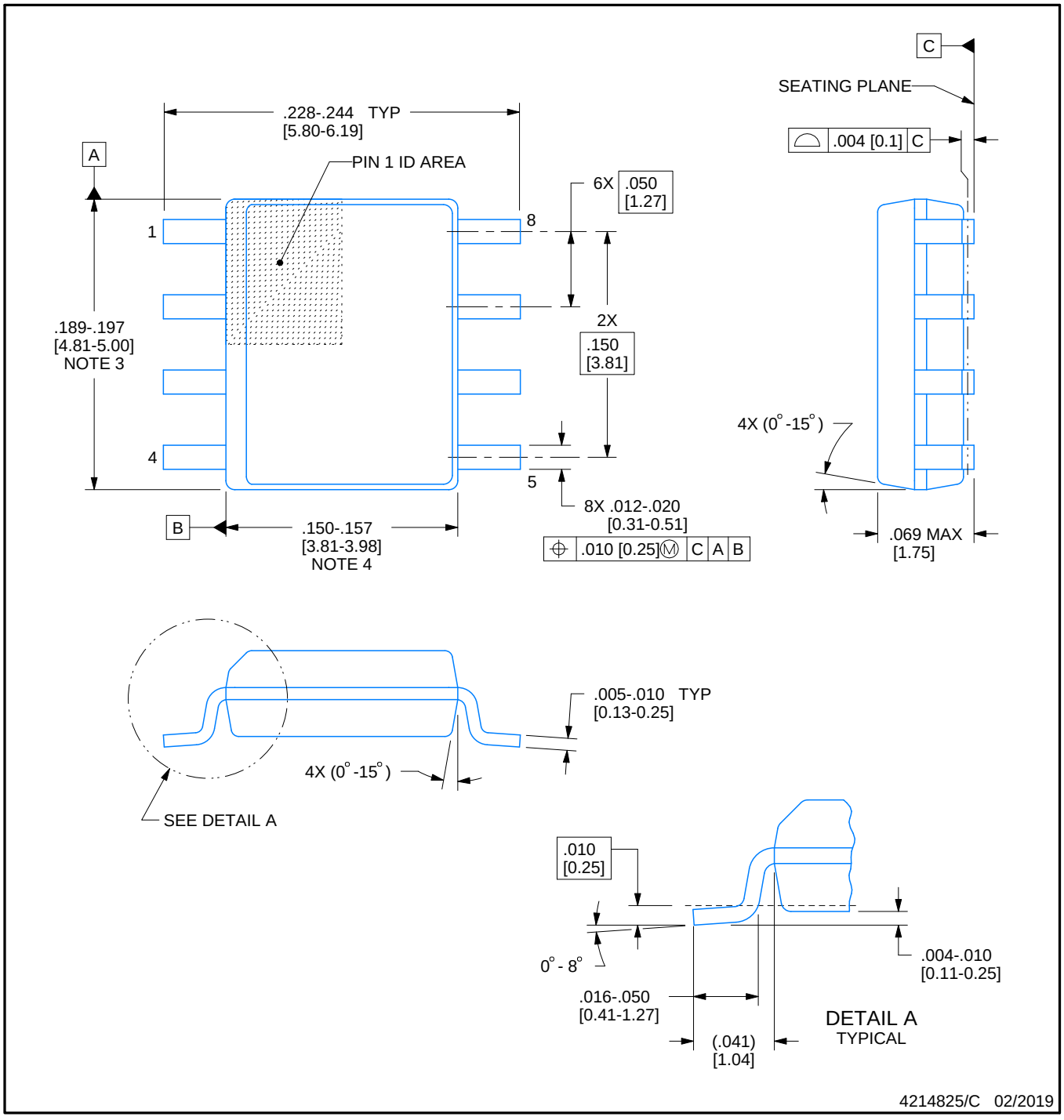


PACKAGE OUTLINE

D0008A

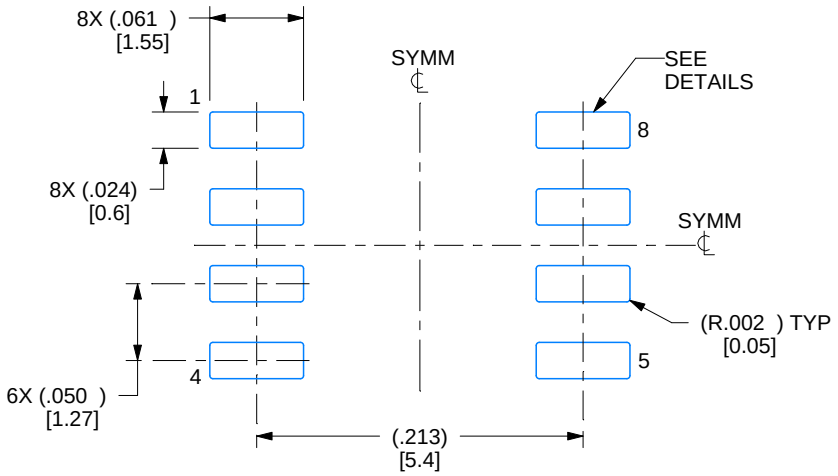
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

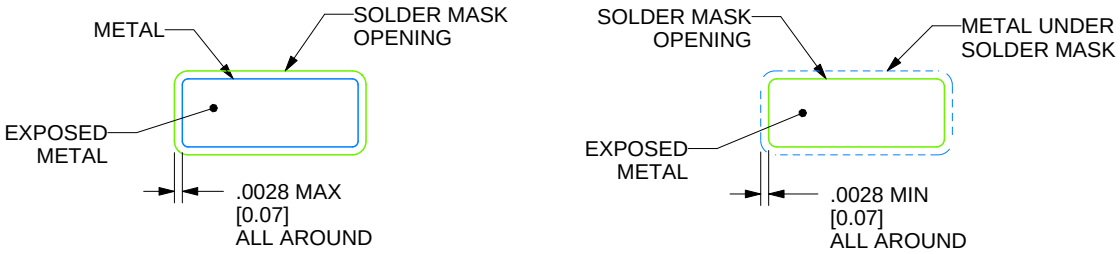


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

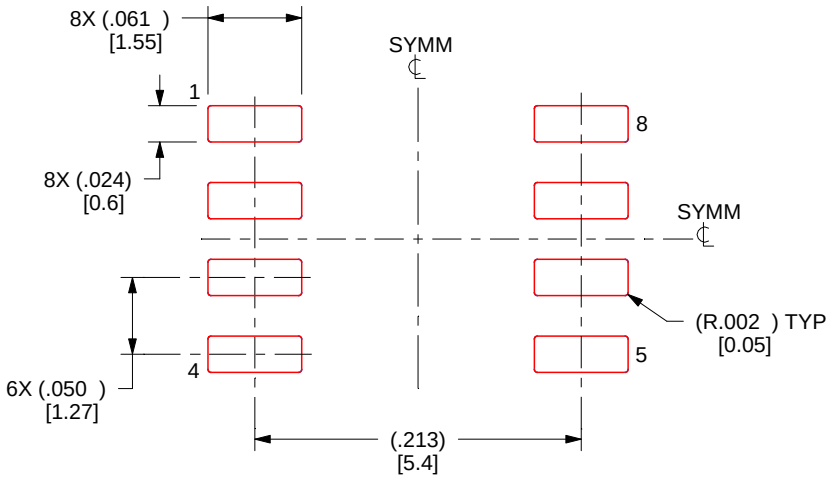
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



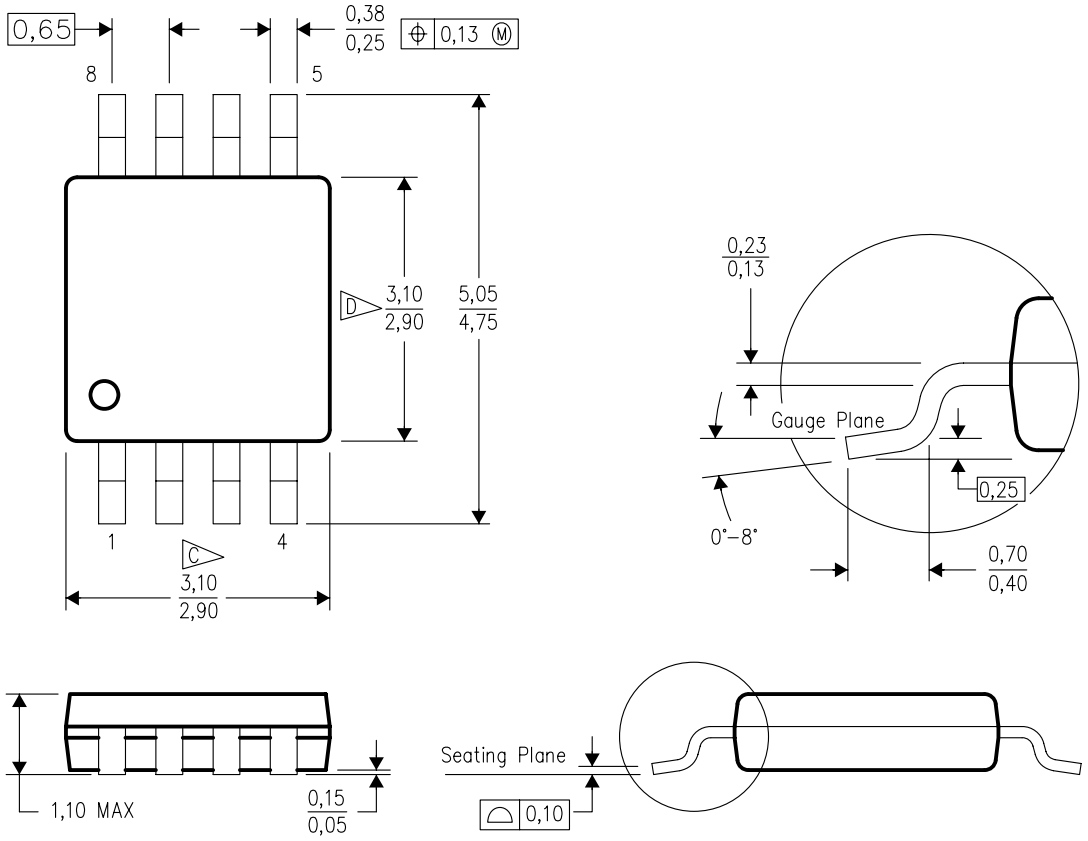
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

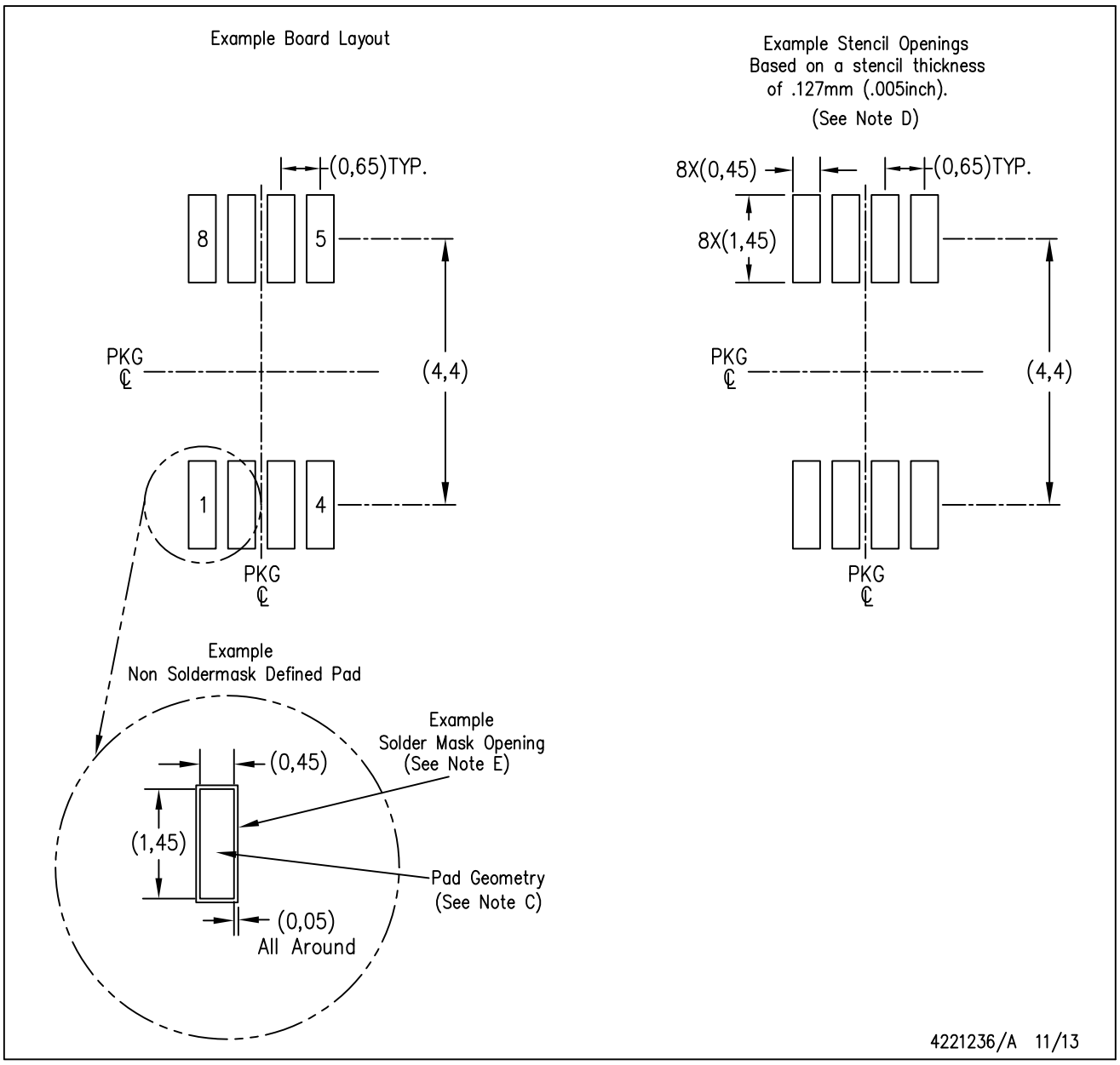
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265