

74CBTLV3253

Dual 1-of-4 multiplexer/demultiplexer

Rev. 7 — 23 April 2024

Product data sheet

1. General description

The 74CBTLV3253 provides a dual 1-of-4 high-speed multiplexer/demultiplexer with two common select inputs (S0, S1) and two output enable inputs (1 $\overline{\text{OE}}$, 2 $\overline{\text{OE}}$). The low ON resistance of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise. When pin n $\overline{\text{OE}}$ = LOW, one of the four switches is selected (low-impedance ON-state) with pins S0 and S1. When pin n $\overline{\text{OE}}$ = HIGH, all switches are in the high-impedance OFF-state, independent of pins S0 and S1.

To ensure the high-impedance OFF-state during power-up or power-down, n $\overline{\text{OE}}$ should be tied to the V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Schmitt trigger action at control input makes the circuit tolerant to slower input rise and fall times across the entire V_{CC} range from 2.3 V to 3.6 V.

This device is fully specified for partial power-down applications using I_{OFF}. The I_{OFF} circuitry disables the output, preventing the damaging backflow current through the device when it is powered down.

2. Features and benefits

- Supply voltage range from 2.3 V to 3.6 V
- High noise immunity
- Complies with JEDEC standard:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8-B/JESD36 (2.7 V to 3.6 V)
- 5 Ω switch connection between two ports
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- I_{OFF} circuitry provides partial Power-down mode operation
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74CBTLV3253D	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74CBTLV3253DS	-40 °C to +85 °C	SSOP16 [1]	plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm	SOT519-1
74CBTLV3253PW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74CBTLV3253BQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1

[1] Also known as QSOP16.

4. Functional diagram

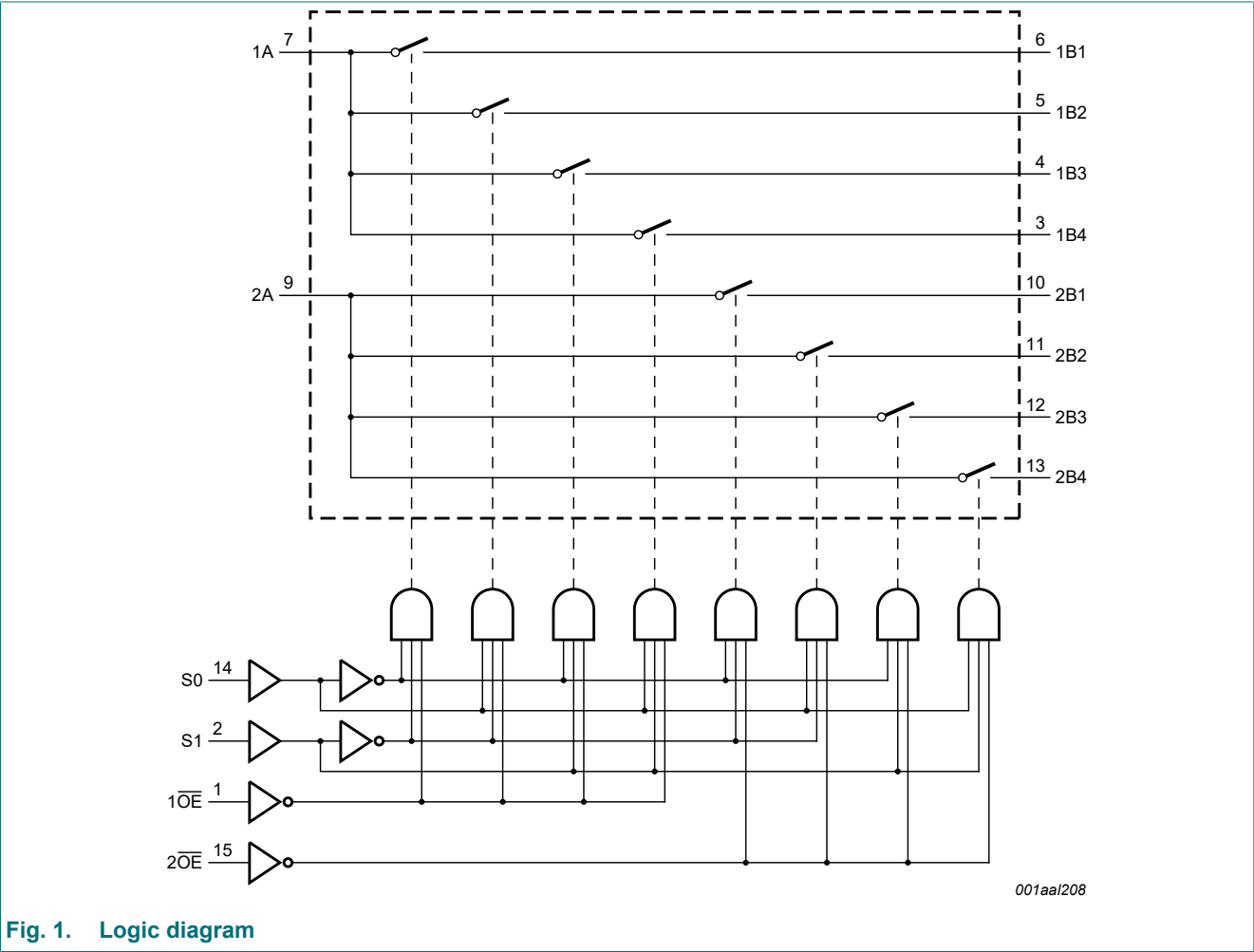
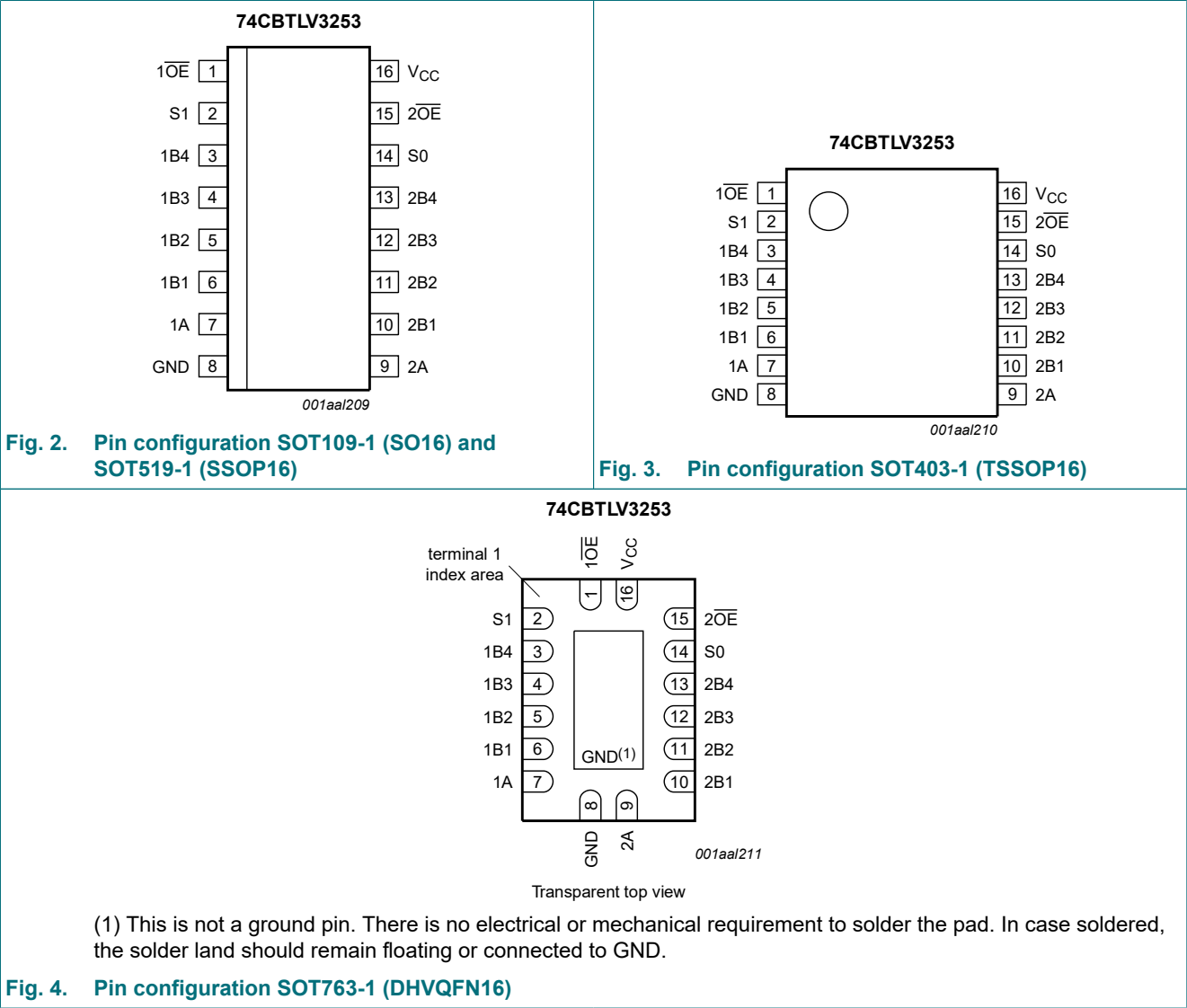


Fig. 1. Logic diagram

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 15	output enable input (active LOW)
S0, S1	14, 2	select input
1B1 to 1B4	6, 5, 4, 3	B input/output
2B1 to 2B4	10, 11, 12, 13	B input/output
GND	8	ground (0 V)
1A, 2A	7, 9	A input/output
VCC	16	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level.

Inputs				Function switch
1OE	2OE	S1	S0	
X	H	X	X	disconnect 2A and 2Bn
H	X	X	X	disconnect 1A and 1Bn
L	L	L	L	1A to 1B1 and 2A to 2B1
L	L	L	H	1A to 1B2 and 2A to 2B2
L	L	H	L	1A to 1B3 and 2A to 2B3
L	L	H	H	1A to 1B4 and 2A to 2B4

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	control inputs [1]	-0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode [2]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V	-50	-	mA
I _{SW}	switch current	V _{SW} = 0 V to V _{CC}	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [3]	-	500	mW

- [1] The minimum input voltage rating may be exceeded if the input clamping current ratings are observed.
- [2] The switch voltage ratings may be exceeded if switch clamping current ratings are observed
- [3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT519-1 (SSOP16) packages: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		2.3	3.6	V
V _I	input voltage		0	3.6	V
V _{SW}	switch voltage	enable and disable mode	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.6 V [1]	0	200	ns/V

- [1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	-	-	1.7	-	V
		V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 V to 2.7 V	-	-	0.7	-	0.7	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I _I	input leakage current	pin n $\overline{\text{OE}}$; V _I = GND to V _{CC} ; V _{CC} = 3.6 V	-	-	±1	-	±20	μA
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Fig. 5	-	-	±1	-	±20	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Fig. 6	-	-	±1	-	±20	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	μA
I _{CC}	supply current	V _I = GND or V _{CC} ; I _O = 0 A; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V	-	-	10	-	50	μA
ΔI _{CC}	additional supply current	pin n $\overline{\text{OE}}$; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V; One input at 3 V, other inputs at V _{CC} or GND.	-	-	300	-	2000	μA
C _I	input capacitance	pin n $\overline{\text{OE}}$; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	5.2	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	20.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

9.1. Test circuits

V_I = V_{CC} or GND and V_O = GND or V_{CC}.

Fig. 5. Test circuit for measuring OFF-state leakage current (one switch)

V_I = V_{CC} or GND and V_O = open circuit.

Fig. 6. Test circuit for measuring ON-state leakage current (one switch)

9.2. ON resistance

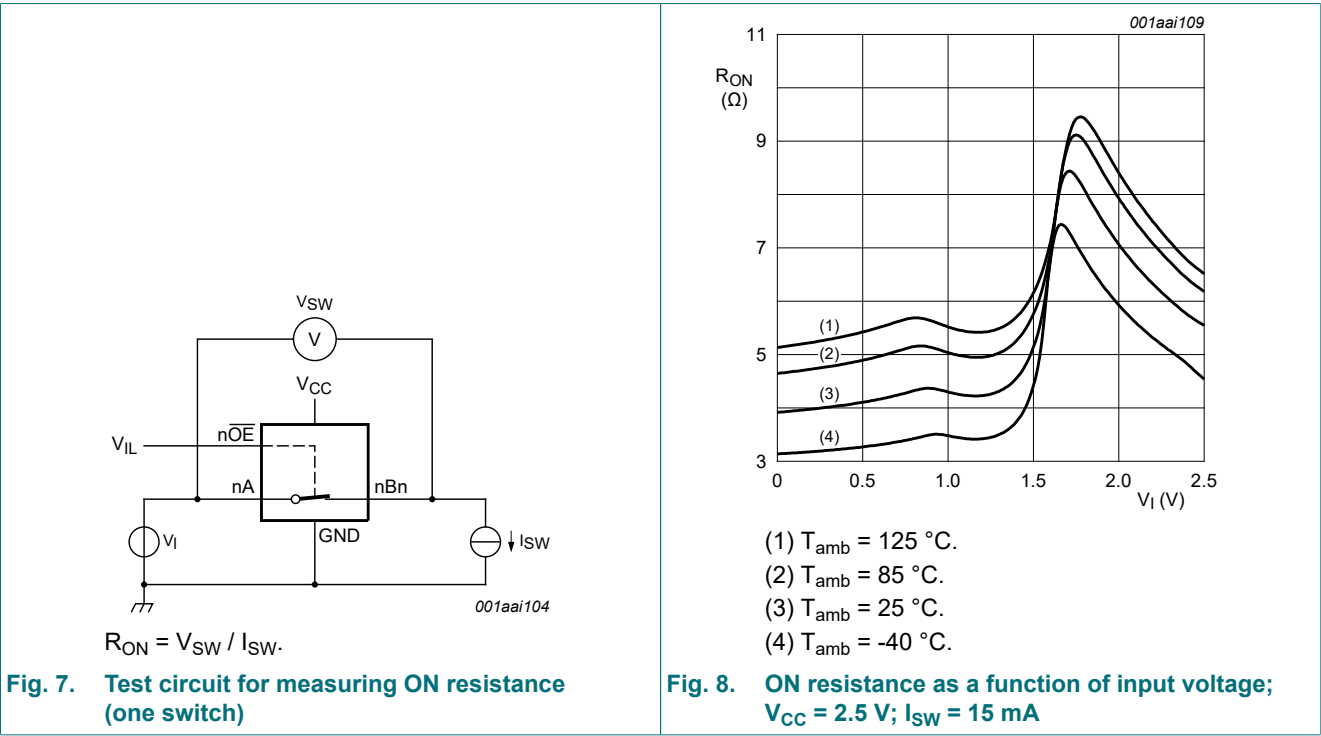
Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R _{ON}	ON resistance	V _{CC} = 2.3 V to 2.7 V; see Fig. 8 to Fig. 10 [2]						
		I _{SW} = 64 mA; V _I = 0 V	-	4.2	8.0	-	15.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	4.2	8.0	-	15.0	Ω
		I _{SW} = 15 mA; V _I = 1.7 V	-	8.4	40.0	-	60.0	Ω
		V _{CC} = 3.0 V to 3.6 V; see Fig. 11 to Fig. 13						
		I _{SW} = 64 mA; V _I = 0 V	-	4.0	7.0	-	11.0	Ω
		I _{SW} = 24 mA; V _I = 0 V	-	4.0	7.0	-	11.0	Ω
		I _{SW} = 15 mA; V _I = 2.4 V	-	6.2	15.0	-	25.5	Ω

- [1] Typical values are measured at T_{amb} = 25 °C and nominal V_{CC}.
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

9.3. ON resistance test circuit and graphs



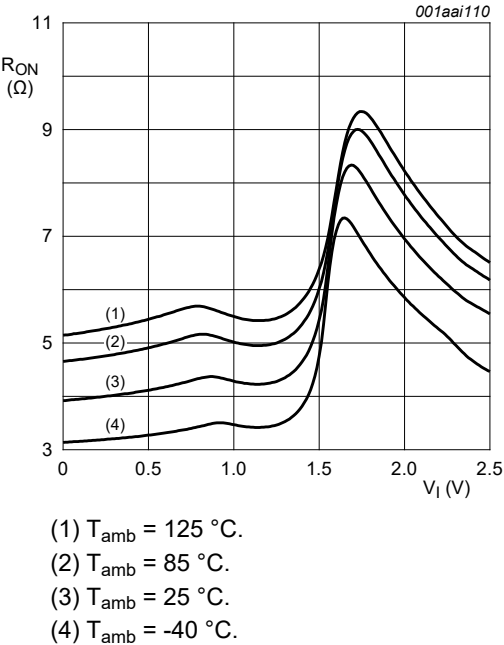


Fig. 9. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}; I_{SW} = 24\text{ mA}$

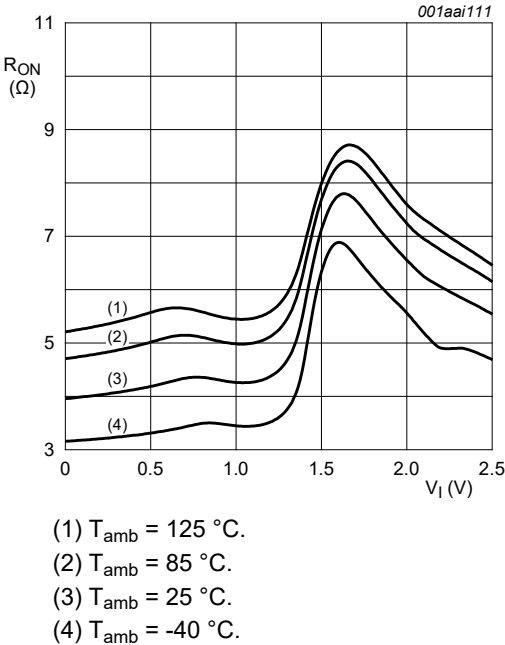


Fig. 10. ON resistance as a function of input voltage;
 $V_{CC} = 2.5\text{ V}; I_{SW} = 64\text{ mA}$

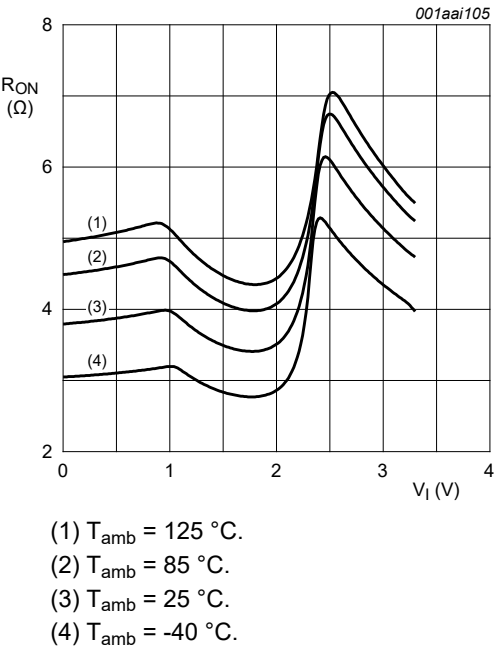


Fig. 11. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}; I_{SW} = 15\text{ mA}$

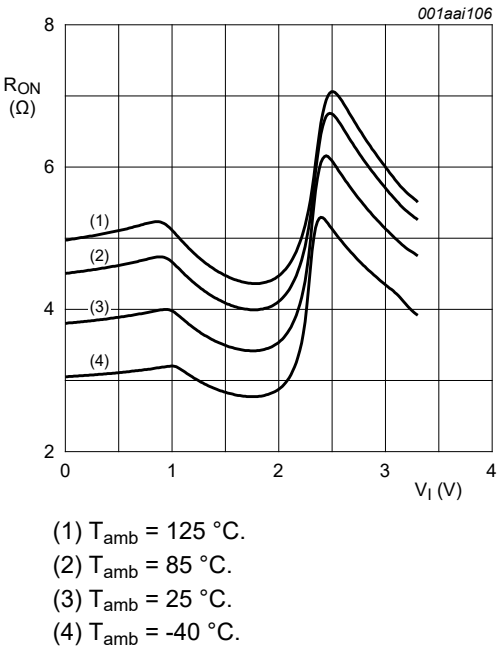
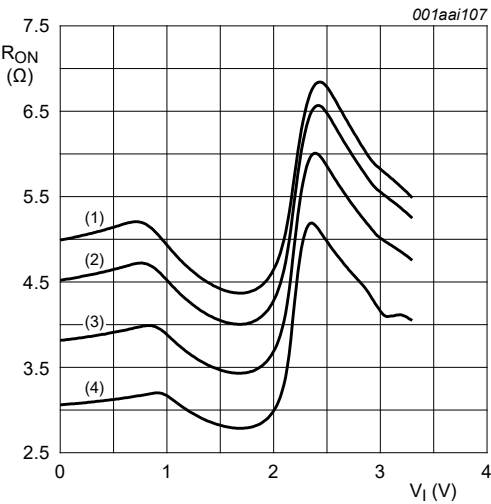


Fig. 12. ON resistance as a function of input voltage;
 $V_{CC} = 3.3\text{ V}; I_{SW} = 24\text{ mA}$



- (1) $T_{amb} = 125\text{ }^{\circ}\text{C}$.
- (2) $T_{amb} = 85\text{ }^{\circ}\text{C}$.
- (3) $T_{amb} = 25\text{ }^{\circ}\text{C}$.
- (4) $T_{amb} = -40\text{ }^{\circ}\text{C}$.

Fig. 13. ON resistance as a function of input voltage; $V_{CC} = 3.3\text{ V}$; $I_{SW} = 64\text{ mA}$

10. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0\text{ V}$; for test circuit see Fig. 16

Symbol	Parameter	Conditions	$T_{amb} = -40\text{ }^{\circ}\text{C to } +85\text{ }^{\circ}\text{C}$			$T_{amb} = -40\text{ }^{\circ}\text{C to } +125\text{ }^{\circ}\text{C}$		Unit
			Min	Typ [1]	Max	Min	Max	
t_{pd}	propagation delay	nA to nBn or nBn to nA; see Fig. 14 [2] [3]						
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	-	-	0.15	-	0.25	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	-	-	0.15	-	0.25	ns
		Sn to nA; see Fig. 14 [3]						
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.0	2.2	6.8	1.0	7.5	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	2.0	5.5	1.0	6.1	ns
t_{en}	enable time	nOE to nA or nBn; see Fig. 15 [4]						
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.0	2.1	5.0	1.0	5.5	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	1.9	4.8	1.0	5.3	ns
		Sn to nBn; see Fig. 15 [4]						
		$V_{CC} = 2.3\text{ V to } 2.7\text{ V}$	1.0	2.1	4.3	1.0	4.7	ns
		$V_{CC} = 3.0\text{ V to } 3.6\text{ V}$	1.0	1.9	4.0	1.0	4.4	ns

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			T _{amb} = -40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{dis}	disable time	n $\overline{\text{OE}}$ to nA or nBn; see Fig. 15 [5]						
		V _{CC} = 2.3 V to 2.7 V	1.0	2.6	5.5	1.0	6.1	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.2	5.4	1.0	5.9	ns
		Sn to nBn; see Fig. 15 [5]						
		V _{CC} = 2.3 V to 2.7 V	0.8	2.0	4.8	0.8	5.3	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.0	4.5	1.0	5.0	ns

- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1. Waveforms and test circuit

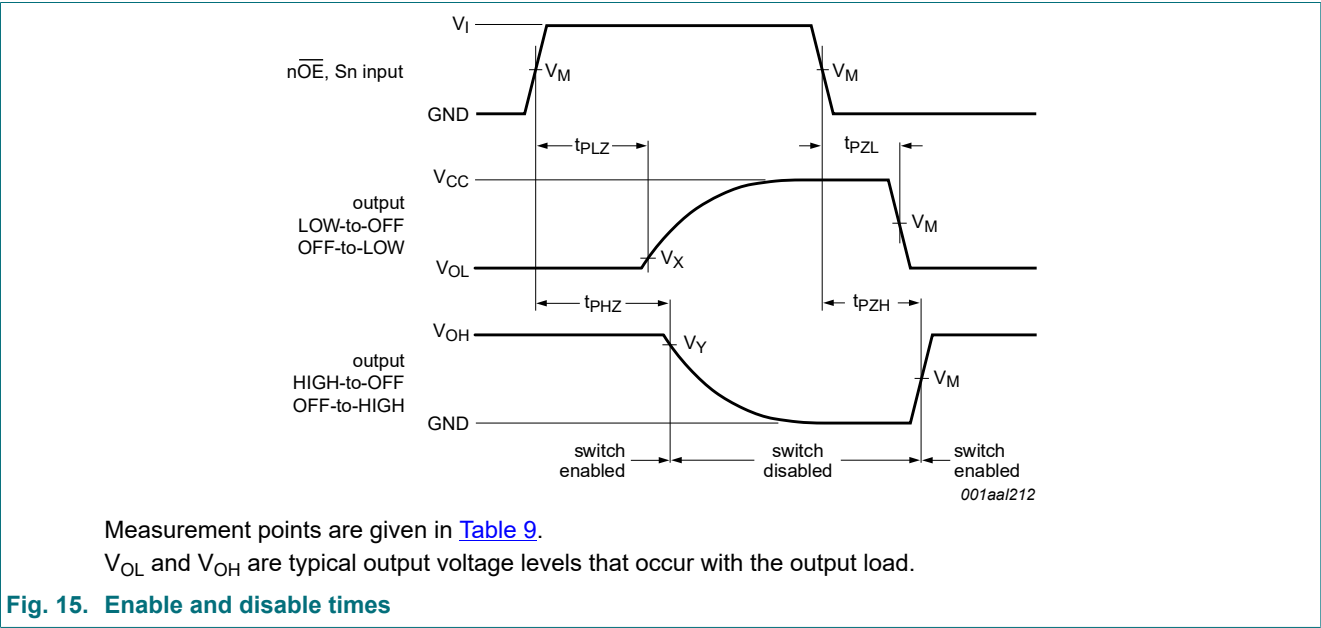
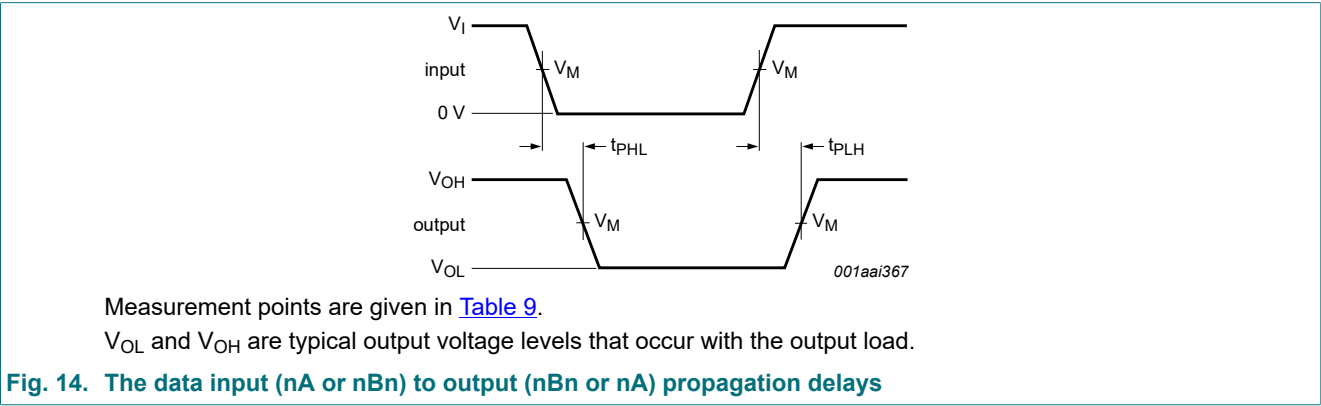


Table 9. Measurement points

Supply voltage	Input			Output		
V _{CC}	V _M	V _I	t _r = t _f	V _M	V _X	V _Y
2.3 V to 2.7 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.5V _{CC}	V _{OL} + 0.15 V	V _{OH} - 0.15 V
3.0 V to 3.6 V	0.5V _{CC}	V _{CC}	≤ 2.0 ns	0.5V _{CC}	V _{OL} + 0.3 V	V _{OH} - 0.3 V

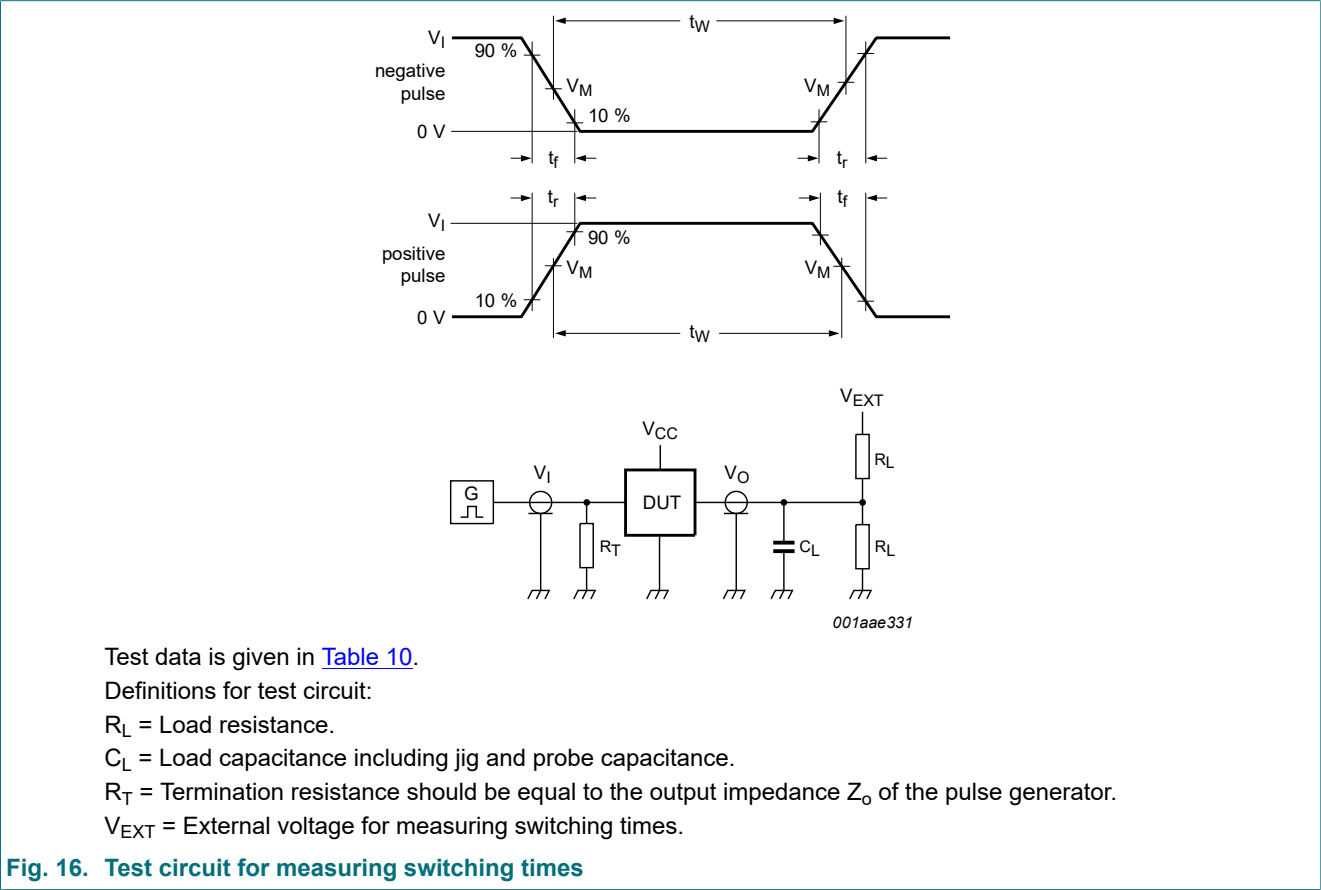


Fig. 16. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V _{EXT}		
V _{CC}	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
2.3 V to 2.7 V	30 pF	500 Ω	open	GND	2V _{CC}
3.0 V to 3.6 V	50 pF	500 Ω	open	GND	2V _{CC}

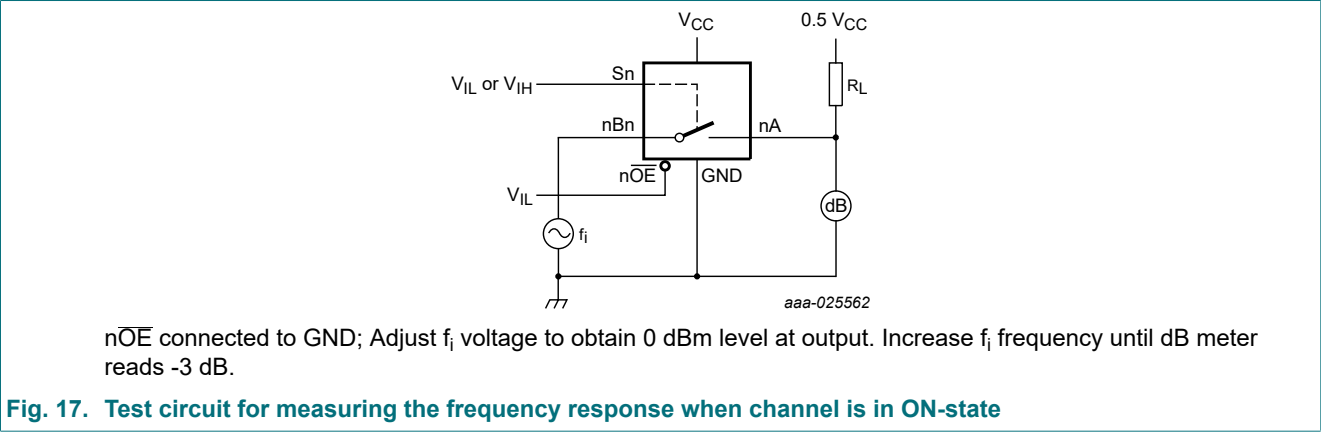
10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND}$ or V_{CC} (unless otherwise specified); $t_r = t_f \leq 2.5 \text{ ns}$.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ	Max	
f _(-3dB)	-3 dB frequency response	V _{CC} = 3.3 V; R _L = 50 Ω; see Fig. 17 [1]	-	302	-	MHz

[1] f_i is biased at 0.5V_{CC}.



11. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1

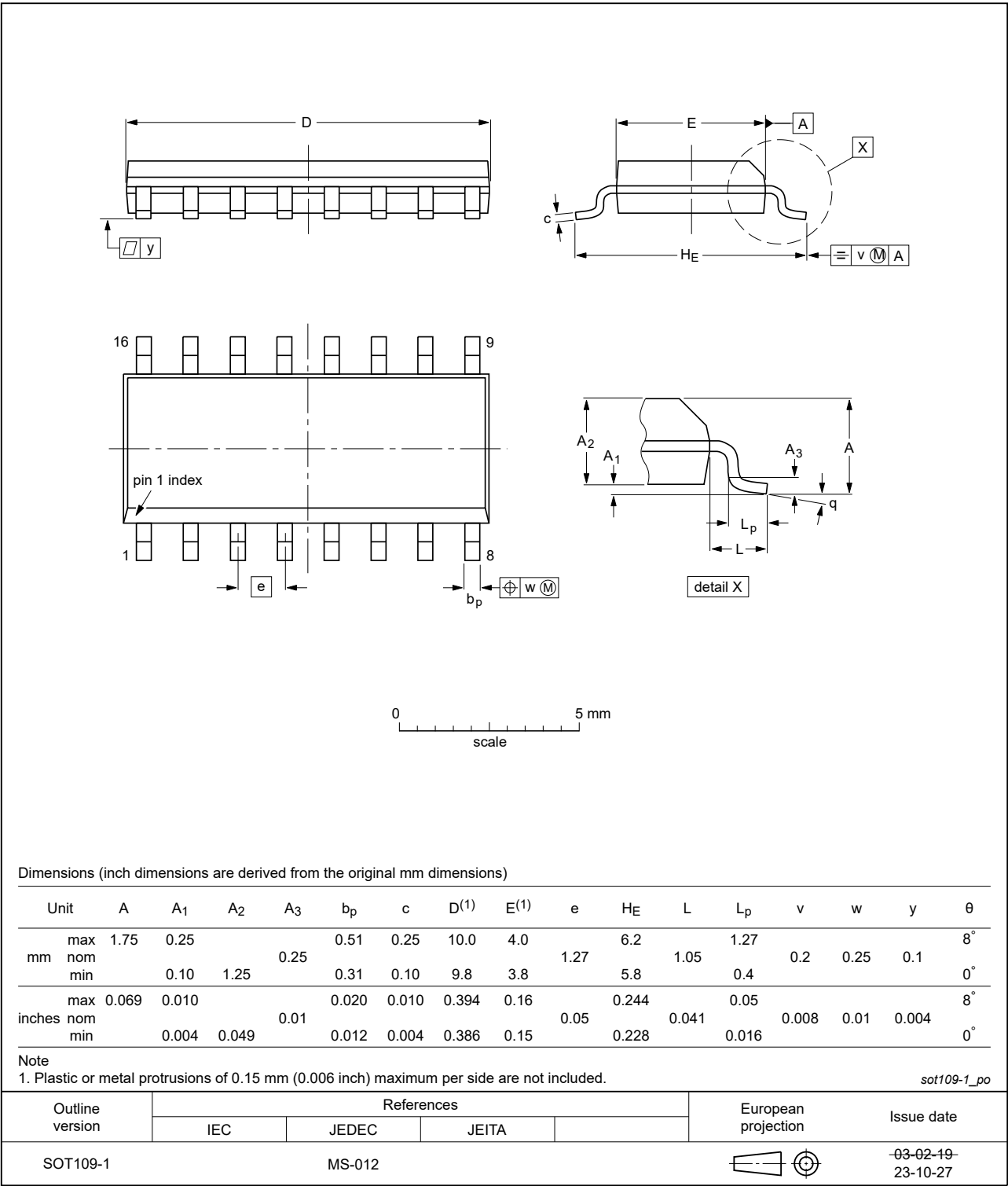


Fig. 18. Package outline SOT109-1 (SO16)

SSOP16: plastic shrink small outline package; 16 leads; body width 3.9 mm; lead pitch 0.635 mm SOT519-1

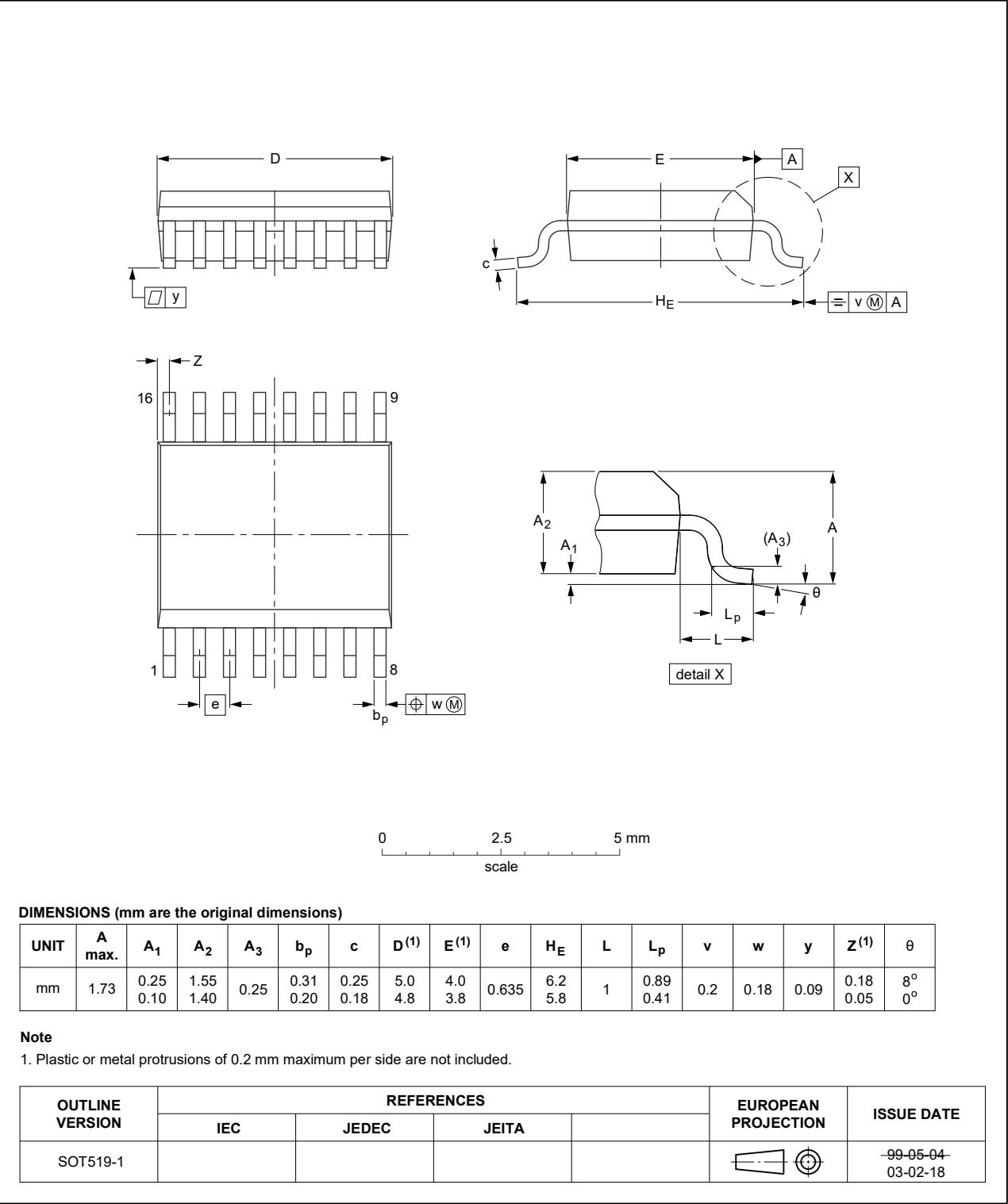


Fig. 19. Package outline SOT519-1 (SSOP16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

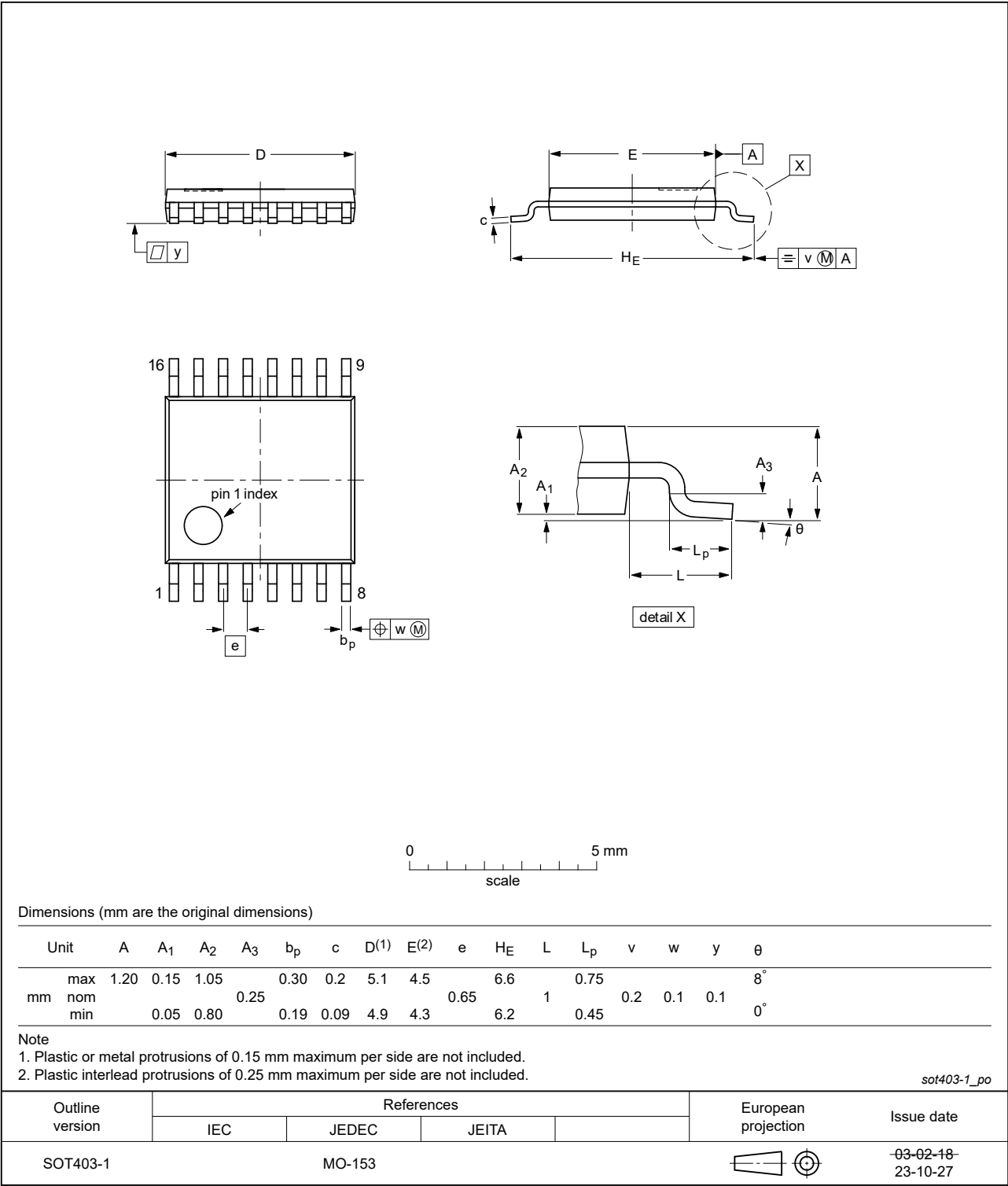


Fig. 20. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm

SOT763-1

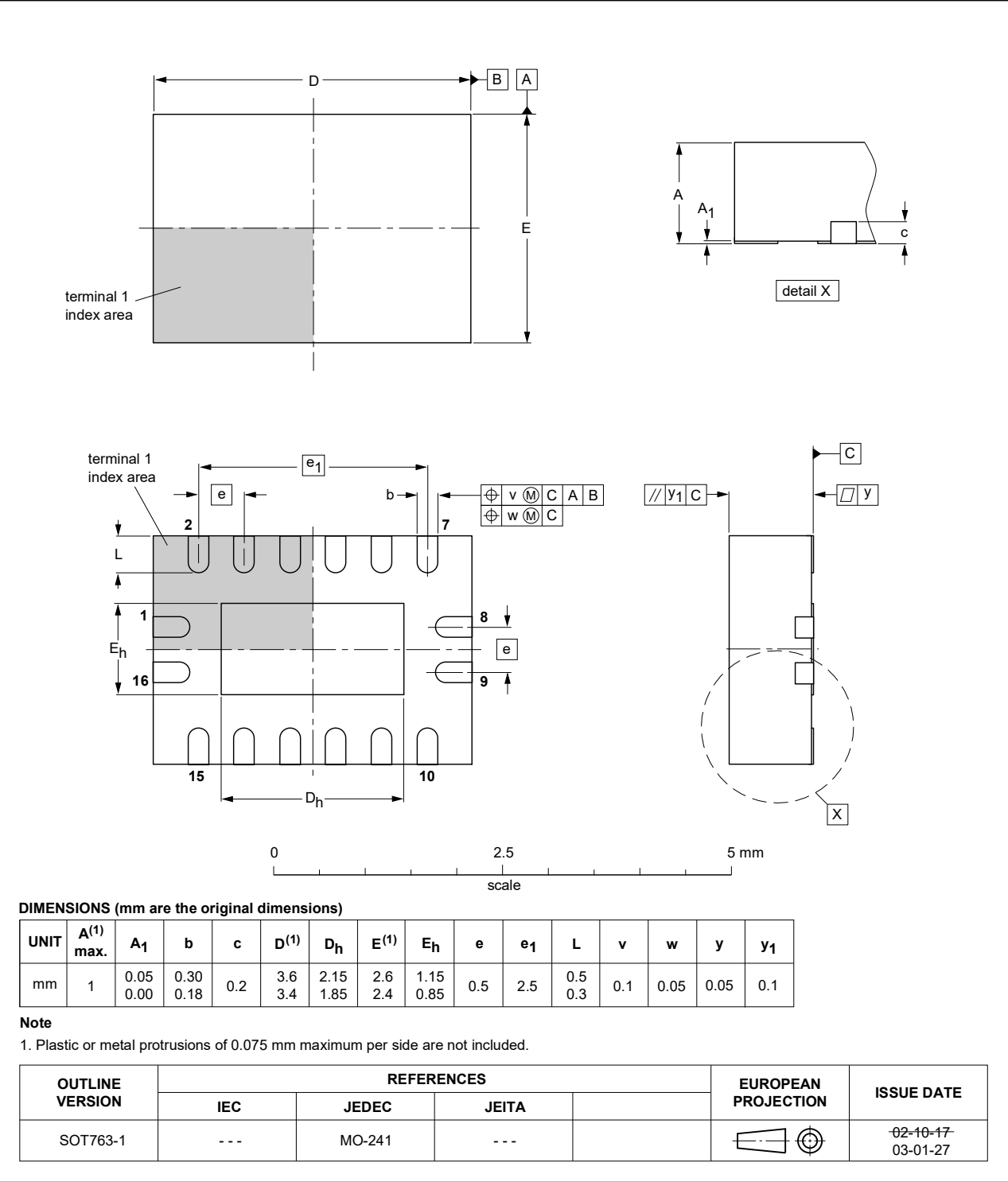


Fig. 21. Package outline SOT763-1 (DHVQFN16)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLV3253 v.7	20240423	Product data sheet	-	74CBTLV3253 v.6
Modifications:	<ul style="list-style-type: none">Fig. 18, Fig. 20: Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.Section 2: ESD specification updated according to the latest JEDEC standard.			
74CBTLV3253 v.6	20200924	Product data sheet	-	74CBTLV3253 v.5
Modifications:	<ul style="list-style-type: none">The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia.Legal texts have been adapted to the new company name where appropriate.Table 4: Derating values for P_{tot} total power dissipation updated.			
74CBTLV3253 v.5	20161111	Product data sheet	-	74CBTLV3253 v.4
Modifications:	<ul style="list-style-type: none">Section 10.2 added.			
74CBTLV3253 v.4	20111215	Product data sheet	-	74CBTLV3253 v.3
Modifications:	<ul style="list-style-type: none">Legal pages updated.			
74CBTLV3253 v.3	20110107	Product data sheet	-	74CBTLV3253 v.2
74CBTLV3253 v.2	20101125	Product data sheet	-	74CBTLV3253 v.1
74CBTLV3253 v.1	20100108	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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