

# SNx4HC245 Octal Bus Transceivers With 3-State Outputs

## 1 Features

- Wide Operating Voltage Range of 2 V to 6 V
- High-Current 3-State Outputs Drive Bus Lines Directly or Up to 15 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 12$  ns
- $\pm 6$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- On Products Compliant to MIL-PRF-38535, All Parameters Are Tested Unless Otherwise Noted. On All Other Products, Production Processing Does Not Necessarily Include Testing of All Parameters.

## 2 Applications

- Servers
- PCs and Notebooks
- Network Switches
- Wearable Health and Fitness Devices
- Telecom Infrastructures
- Electronic Points of Sale

## 3 Description

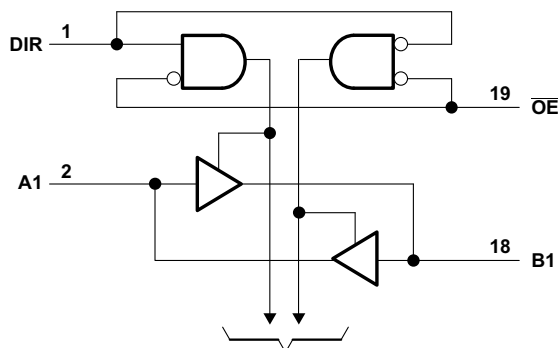
These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements.

The devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ( $\overline{OE}$ ) input can be used to disable the device so that the buses are effectively isolated.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SNx4HC245	DB (SSOP, 20)	7.20 mm $\times$ 5.30 mm
	DW (SOIC, 20)	12.80 mm $\times$ 7.50 mm
	N (PDIP, 20)	24.33 mm $\times$ 6.35 mm
	NS (SO, 20)	12.60 mm $\times$ 5.30 mm
	PW (TSSOP, 20)	6.50 mm $\times$ 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



To Seven Other Channels  
**Logic Diagram (Positive Logic)**



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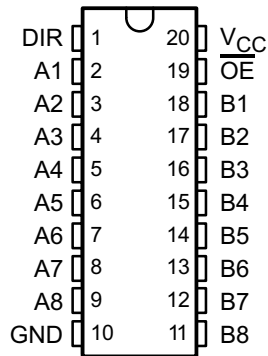
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## 4 Revision History

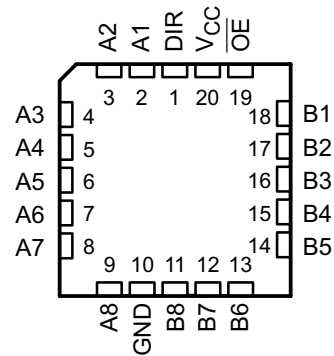
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision E (September 2015) to Revision F (August 2022)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Updated the numbering, formatting, tables, figures and cross-references throughout the document to reflect modern datasheet standards.....</li> </ul>	<b>1</b>
<b>Changes from Revision D (August 2003) to Revision E (July 2015)</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>Added <i>Device Comparison</i> section, <i>Thermal Information</i> section, <i>ESD Ratings</i> section, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, and <i>Layout</i> section.....</li> <li>Added Military Disclaimer to Features list.....</li> <li>Updated FK package pinout drawing.....</li> </ul>	<b>1</b> <b>1</b> <b>3</b>

## 5 Pin Configuration and Functions



**Figure 5-1. DB, DGV, DW, N, J, W, or PW Package  
20-Pin SSOP, TVSOP, SOIC, PDIP CDIP, CFP, or  
TSSOP Top View**



**Figure 5-2. FK Package 20-Pin LCCC Top View**

PIN		TYPE <sup>(1)</sup>	DESCRIPTION
NO.	NAME		
1	DIR	I/O	Direction Pin
2	A1	I/O	A1 Input/Output
3	A2	I/O	A2 Input/Output
4	A3	I/O	A3 Input/Output
5	A4	I/O	A4 Input/Output
6	A5	I/O	A5 Input/Output
7	A6	I/O	A6 Input/Output
8	A7	I/O	A7 Input/Output
9	A8	I/O	A8 Input/Output
10	GND	—	Ground Pin
11	B8	I/O	B8 Input/Output
12	B7	I/O	B7 Input/Output
13	B6	I/O	B6 Input/Output
14	B5	I/O	B5 Input/Output
15	B4	I/O	B4 Input/Output
16	B3	I/O	B3 Input/Output
17	B2	I/O	B2 Input/Output
18	B1	I/O	B1 Input/Output
19	OE	I/O	Output Enable
20	VCC	—	Power Pin

(1) Signal Types: I = Input, O = Output, I/O = Input or Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
$I_{IK}$	Input clamp current <sup>(2)</sup>	$V_I < 0$ or $V_I > V_{CC}$		±20 mA
$I_{OK}$	Output clamp current <sup>(2)</sup>	$V_O < 0$ or $V_O > V_{CC}$		±20 mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$		±35 mA
	Continuous current through $V_{CC}$ or GND			±70 mA
$T_{stg}$	Storage temperature	-65	150	°C
$T_J$	Junction Temperature		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

### 6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±3000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		SN54HC245			SN74HC245			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$	Supply voltage	2	5	6	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5			V
		$V_{CC} = 4.5$ V		3.15	3.15			
		$V_{CC} = 6$ V		4.2	4.2			
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	0.5			V
		$V_{CC} = 4.5$ V		1.35	1.35			
		$V_{CC} = 6$ V		1.8	1.8			
$V_I$	Input voltage	0		$V_{CC}$	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	0		$V_{CC}$	V
$\Delta t/\Delta v$	Input transition rise and fall time	$V_{CC} = 2$ V		1000	1000			ns
		$V_{CC} = 4.5$ V		500	500			
		$V_{CC} = 6$ V		400	400			
$T_A$	Operating free-air temperature	-55		125	-40		85	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

## 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		SNx4HC245					UNIT
		DB (SSOP)	DW (SOIC)	N (PDIP)	NS (SOP)	PW (TSSOP)	
		20 PINS					
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	92.1	77.0	57.0	74.1	99.7	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	53.9	41.5	48.6	40.6	34.0	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	47.2	44.8	38.0	41.6	50.7	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	16.5	16.8	25.4	14.8	1.8	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	46.8	44.3	37.8	41.2	50.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC245		SN74HC245		UNIT
					MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	High-Level Output Voltage		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9		1.9		V
					4.5 V	4.4	4.499	4.4		4.4		
					6 V	5.9	5.999	5.9		5.9		
				I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.3	3.7		3.84		
					6 V	5.48	5.8	5.2		5.34		
V <sub>OL</sub>	Low-Level Output Voltage		V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002	0.1	0.1		0.1		V
					4.5 V	0.001	0.1	0.1		0.1		
					6 V	0.001	0.1	0.1		0.1		
				I <sub>OL</sub> = 6 mA	4.5 V	0.17	0.26	0.4		0.33		
					6 V	0.15	0.26	0.4		0.33		
I <sub>I</sub>	Input Current	DIR or $\overline{OE}$	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V		±0.1	±100	±1000		±1000		nA
I <sub>OZ</sub>	Off-State (High-Impedance State) Output Current	A or B	V <sub>O</sub> = V <sub>CC</sub> or 0	6 V		±0.01	±0.5	±10		±5		μA
I <sub>CC</sub>	Supply Current		V <sub>I</sub> = V <sub>CC</sub> I <sub>O</sub> = 0 or 0,	6 V			8	160		80		μA
C <sub>i</sub>	Input Capacitance	DIR or $\overline{OE}$		2 V to 6 V		3	10	10		10		pF

## 6.6 Switching Characteristics, $C_L = 50 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted)  
(see [Figure 7-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	B or A	2 V		40	105		160		130	ns
			4.5 V		15	21		32		26	
			6 V		12	18		27		22	
$t_{en}$	$\overline{OE}$	A or B	2 V		125	230		340		290	ns
			4.5 V		23	46		68		58	
			6 V		20	39		58		49	
$t_{dis}$	$\overline{OE}$	A or B	2 V		74	200		300		250	ns
			4.5 V		25	40		60		50	
			6 V		21	34		51		43	
$t_t$		A or B	2 V		20	60		90		75	ns
			4.5 V		8	12		18		15	
			6 V		6	10		15		13	

## 6.7 Switching Characteristics, $C_L = 150 \text{ pF}$

over recommended operating free-air temperature range (unless otherwise noted)  
(see [Figure 7-1](#))

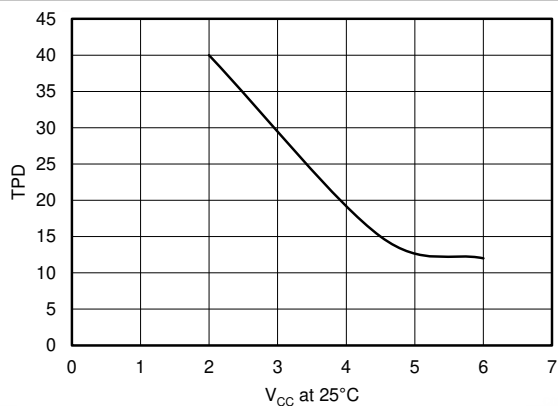
PARAMETER	FROM (INPUT)	TO (OUTPUT )	$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC245		SN74HC245		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$t_{pd}$	A or B	B or A	2 V		54	135		200		170	ns
			4.5 V		18	27		40		34	
			6 V		15	23		34		29	
$t_{en}$	$\overline{OE}$	A or B	2 V		150	270		405		335	ns
			4.5 V		31	54		81		67	
			6 V		25	46		69		56	
$t_t$		A or B	2 V		45	210		315		265	ns
			4.5 V		17	42		63		53	
			6 V		13	36		53		45	

## 6.8 Operating Characteristics

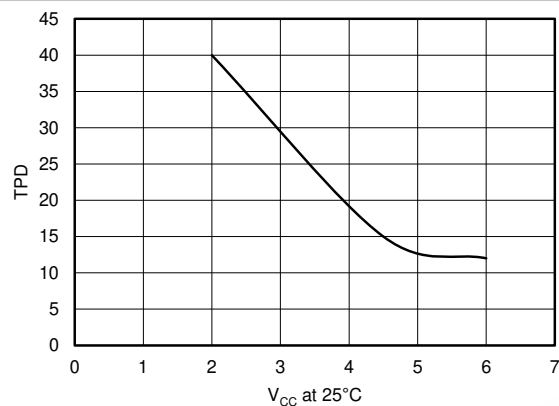
$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
$C_{pd}$ Power dissipation capacitance per transceiver	No load	40	pF

## 6.9 Typical Characteristics



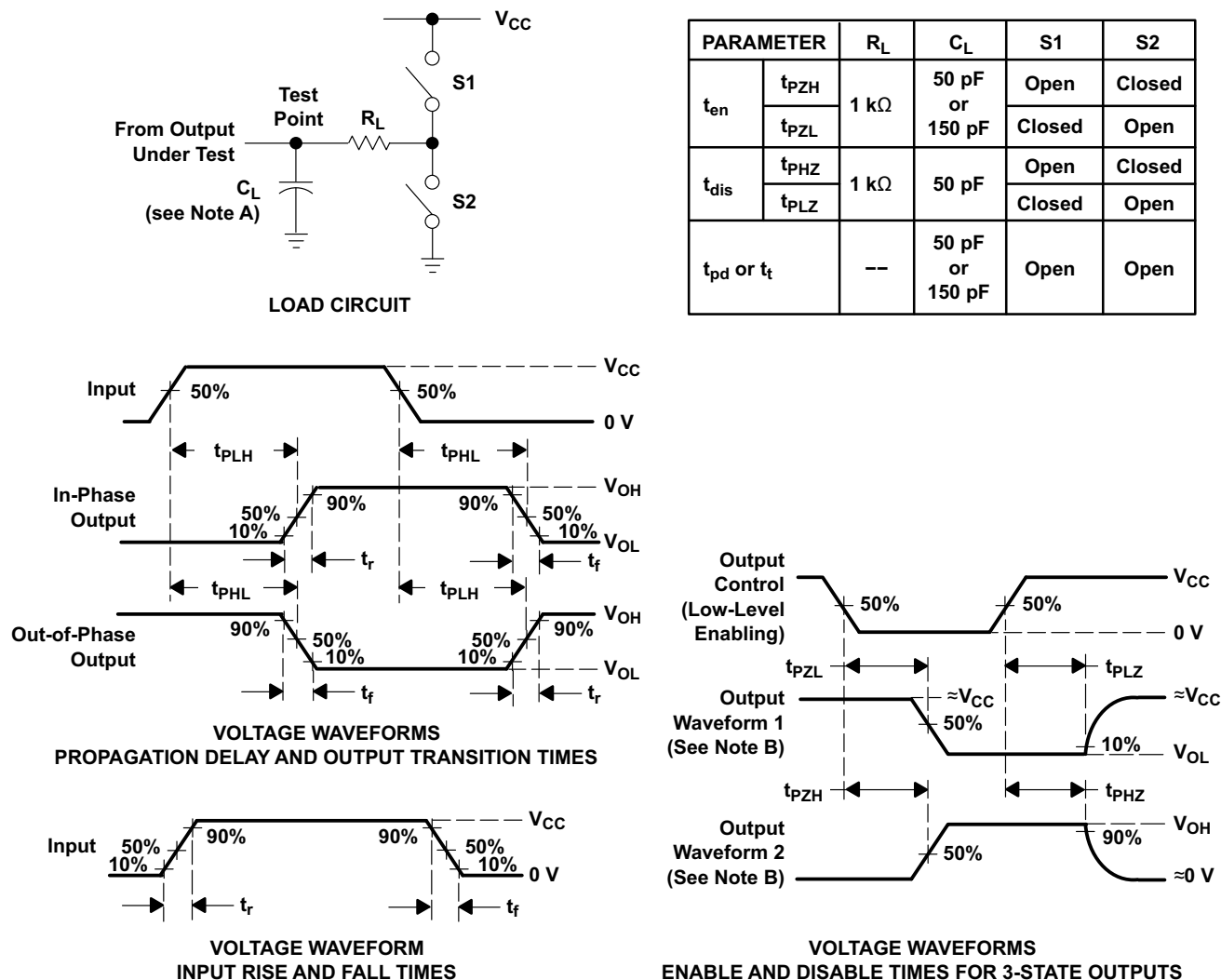
**Figure 6-1. TPD vs  $V_{CC}$  at 25°C**



**Figure 6-2. TPD vs  $V_{CC}$  at 25°C**

## 7 Parameter Measurement Information

### 7.1



- A.  $C_L$  includes probe and test-fixture capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
- D. The outputs are measured one at a time with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

**Figure 7-1. Load Circuit and Voltage Waveforms**

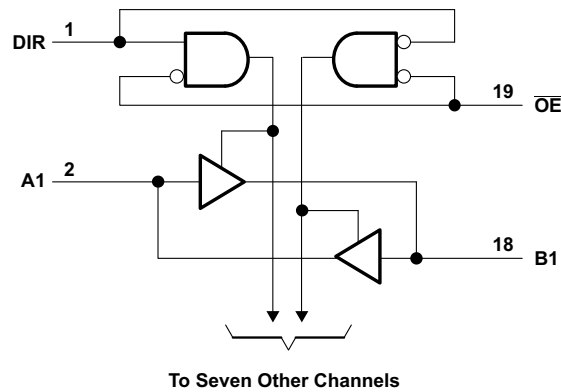


## 8 Detailed Description

## 8.1 Overview

These octal bus transceivers are designed for asynchronous two-way communication between data buses. The control-function implementation minimizes external timing requirements. The SNx4HC245 devices allow data transmission from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable (OE) input can be used to disable the device so that the buses are effectively isolated. To ensure the high-impedance state during power up or power down, OE should be tied to VCC through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## 8.2 Functional Block Diagram



### Logic Diagram (Positive Logic)

### 8.3 Feature Description

The SNx4HC245 devices have a wide operating VCC range from 2 V to 6 V with slower edge rates to minimize output ringing.

## 8.4 Device Functional Modes

Table 8-1 lists the function modes of the SNx4HC245.

### Table 8-1. Function Table

INPUTS (1)		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

The SNx4HC245 is a low-drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs.

### 9.2 Typical Application

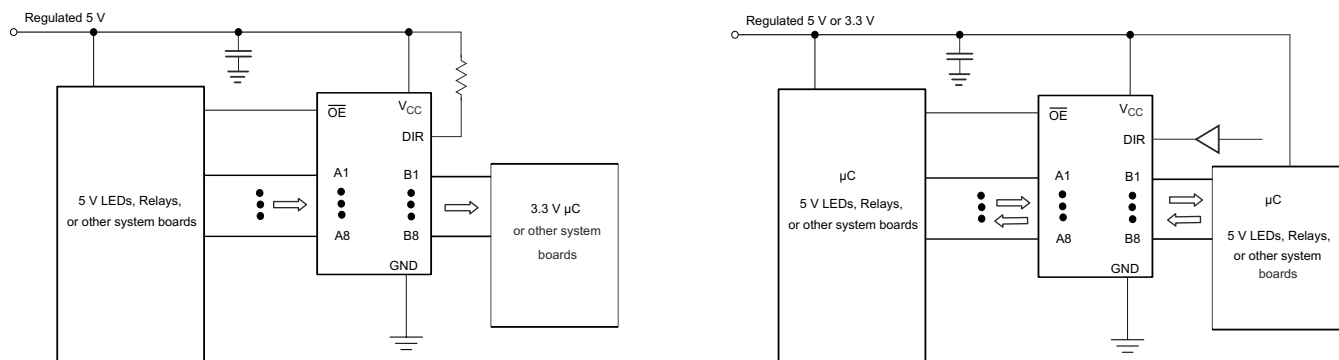


Figure 9-1. Typical Application Schematic

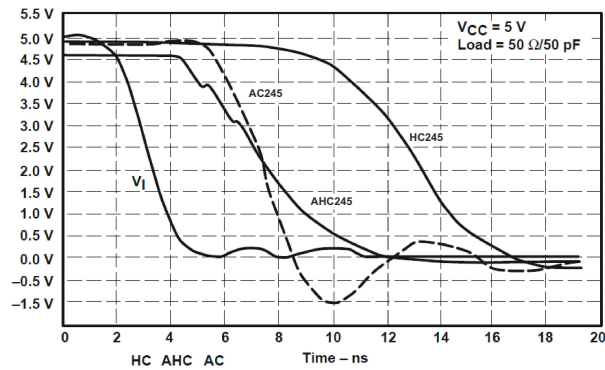
#### 9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads, so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

- Recommended Input Conditions
  - Rise time and fall time specs: See  $(\Delta t/\Delta V)$  in the [Section 6.3](#).
  - Specified high and low levels: See  $(V_{IH}$  and  $V_{IL})$  in the [Section 6.3](#).
- Recommend Output Conditions
  - Load currents should not exceed 25 mA per output and 75 mA total for the part.
  - Outputs should not be pulled above  $V_{CC}$ .

### 9.2.3 Application Curve



**Figure 9-2. Switching Characteristics Comparison**

## 10 Power Supply Recommendations

The power supply can be any voltage between the MIN and MAX supply voltage rating located in the [Section 6.3](#).

Each  $V_{CC}$  pin should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, 0.1  $\mu\text{F}$  is recommended; if there are multiple  $V_{CC}$  pins, then 0.01  $\mu\text{F}$  or 0.022  $\mu\text{F}$  is recommended for each power pin. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and a 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power pin as possible for best results.

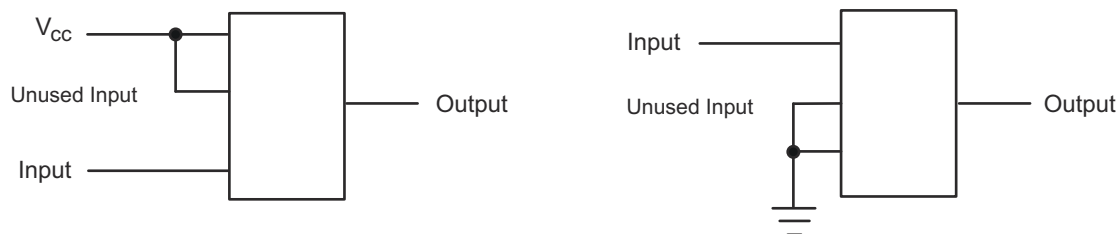
## 11 Layout

### 11.1 Layout Guidelines

When using multiple-bit logic devices, inputs should never float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. [Figure 11-1](#) specifies the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$ , whichever makes more sense or is more convenient. It is generally acceptable to float outputs, unless the part is a transceiver. If the transceiver has an output enable pin, it will disable the output section of the part when asserted. This will not disable the input section of the IOs, so they cannot float when disabled.

### 11.2 Layout Example



**Figure 11-1. Layout Diagram**

## 12 Device and Documentation Support

### 12.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 12-1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54HC245	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74HC245	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](#). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

### 12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

All trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8408501VRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8408501VR A SNV54HC245J	<a href="#">Samples</a>
5962-8408501VSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8408501VS A SNV54HC245W	<a href="#">Samples</a>
84085012A	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK	<a href="#">Samples</a>
8408501RA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J	<a href="#">Samples</a>
8408501SA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W	<a href="#">Samples</a>
JM38510/65503BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BRA	<a href="#">Samples</a>
JM38510/65503BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BSA	<a href="#">Samples</a>
M38510/65503BRA	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BRA	<a href="#">Samples</a>
M38510/65503BSA	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 65503BSA	<a href="#">Samples</a>
SN54HC245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	SN54HC245J	<a href="#">Samples</a>
SN74HC245DBR	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245DBRG4	ACTIVE	SSOP	DB	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245DWR	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245DWRE4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245DWRG4	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245N	ACTIVE	PDIP	N	20	20	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	SN74HC245N	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HC245NSR	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245NSRE4	ACTIVE	SO	NS	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245PWR	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SN74HC245PWRG4	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HC245	<a href="#">Samples</a>
SNJ54HC245FK	ACTIVE	LCCC	FK	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	84085012A SNJ54HC 245FK	<a href="#">Samples</a>
SNJ54HC245J	ACTIVE	CDIP	J	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501RA SNJ54HC245J	<a href="#">Samples</a>
SNJ54HC245W	ACTIVE	CFP	W	20	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	8408501SA SNJ54HC245W	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN54HC245, SN54HC245-SP, SN74HC245 :**

- Catalog : [SN74HC245](#), [SN54HC245](#)
- Military : [SN54HC245](#)
- Space : [SN54HC245-SP](#)

**NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
- Space - Radiation tolerant, ceramic packaging and qualified for use in Space-based application



## TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC245DBR	SSOP	DB	20	2000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
SN74HC245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC245DWR	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
SN74HC245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC245NSR	SO	NS	20	2000	330.0	24.4	8.4	13.0	2.5	12.0	24.0	Q1
SN74HC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
SN74HC245PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74HC245PWRG4	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HC245DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC245DBR	SSOP	DB	20	2000	356.0	356.0	35.0
SN74HC245DWR	SOIC	DW	20	2000	367.0	367.0	45.0
SN74HC245DWR	SOIC	DW	20	2000	356.0	356.0	41.0
SN74HC245NSR	SO	NS	20	2000	356.0	356.0	41.0
SN74HC245NSR	SO	NS	20	2000	367.0	367.0	45.0
SN74HC245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC245PWR	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74HC245PWR	TSSOP	PW	20	2000	364.0	364.0	27.0
SN74HC245PWGR4	TSSOP	PW	20	2000	356.0	356.0	35.0

## TUBE



\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
5962-8408501VSA	W	CFP	20	1	506.98	26.16	6220	NA
84085012A	FK	LCCC	20	1	506.98	12.06	2030	NA
8408501SA	W	CFP	20	1	506.98	26.16	6220	NA
JM38510/65503BSA	W	CFP	20	1	506.98	26.16	6220	NA
M38510/65503BSA	W	CFP	20	1	506.98	26.16	6220	NA
SN74HC245N	N	PDIP	20	20	506	13.97	11230	4.32
SNJ54HC245FK	FK	LCCC	20	1	506.98	12.06	2030	NA
SNJ54HC245W	W	CFP	20	1	506.98	26.16	6220	NA

W (R-GDFP-F20)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only.
  - E. Falls within Mil-Std 1835 GDFP2-F20



4220206/A 02/2017

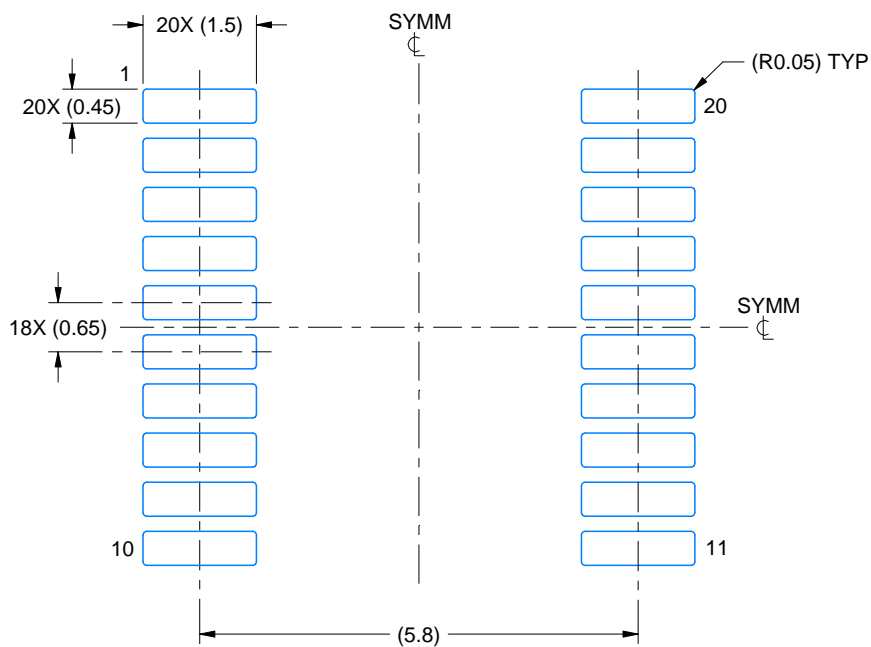
## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

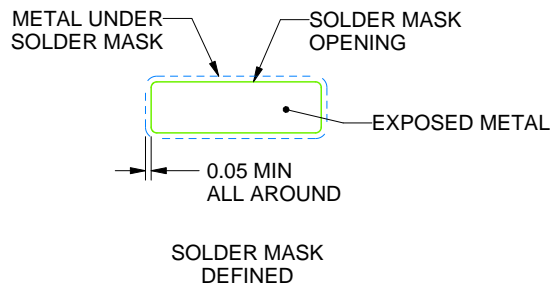
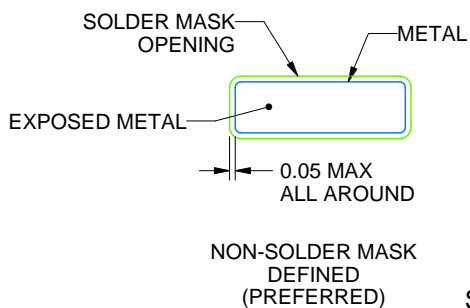
**PW0020A**

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



## SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.  
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.





4214851/B 08/2019

## NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.

# EXAMPLE BOARD LAYOUT

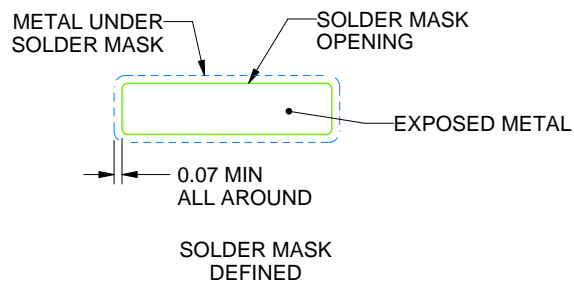
DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## GENERIC PACKAGE VIEW

**FK 20**

**LCCC - 2.03 mm max height**

8.89 x 8.89, 1.27 mm pitch

LEADLESS CERAMIC CHIP CARRIER

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



4229370VA\

N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



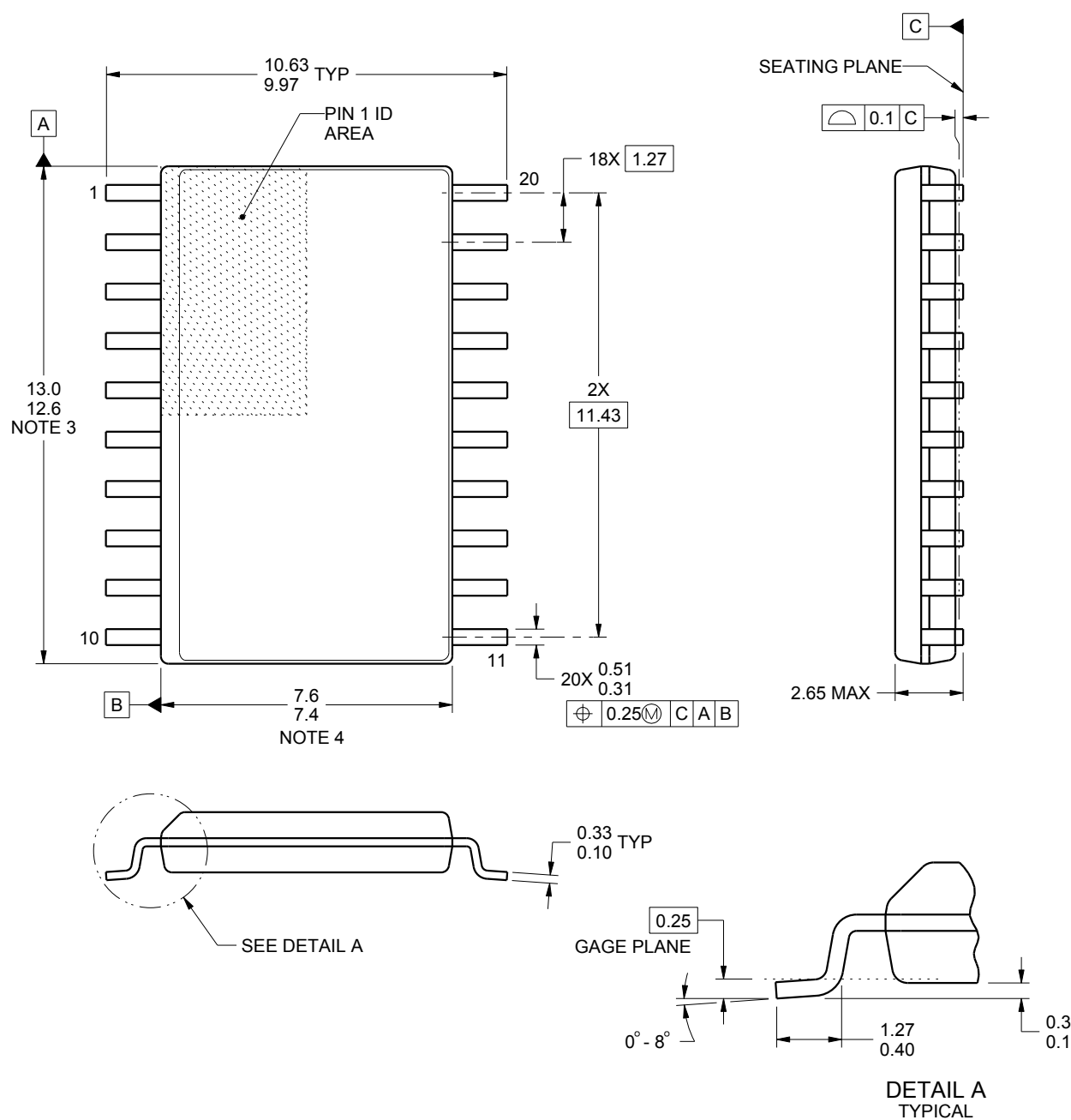
PINS ** DIM	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



4040049/E 12/2002

NOTES:

- A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.
-  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).  
 The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220724/A 05/2016

## NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

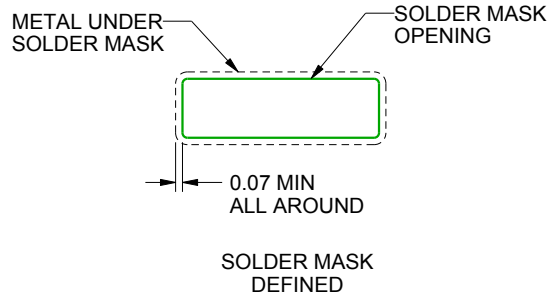
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

## EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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