

## SN74LVC2G32 Dual 2-Input Positive-OR Gate

### 1 Features

- Available in the Texas Instruments NanoFree™ Package
- Supports 5-V  $V_{CC}$  Operation
- Inputs Accept Voltages to 5.5 V
- Maximum  $t_{pd}$  of 3.8 ns at 3.3 V
- Low Power Consumption, 10- $\mu$ A Maximum  $I_{CC}$
- $\pm 24$ -mA Output Drive at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $< 0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $> 2$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- $I_{off}$  Supports Live Insertion, Partial-Power-Down Mode, and Back-Drive Protection
- Can Be Used as a Down Translator to Translate Inputs From a Maximum of 5.5 V Down to the  $V_{CC}$  Level
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- Down Translation
- Logical OR

### 3 Description

This dual 2-input positive-OR gate is designed for 1.65-V to 5.5-V  $V_{CC}$  operation.

The SN74LVC2G32 device performs the Boolean function  $Y = A + B$  or  $Y = \overline{\overline{A} \cdot \overline{B}}$  in positive logic.

NanoFree package technology is a major breakthrough in IC packaging concepts, using the die as the package.

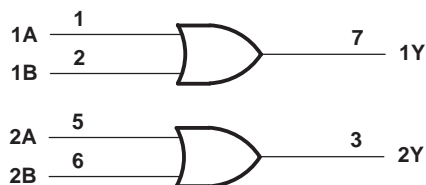
This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE
SN74LVC2G32DCT	SSOP (8)	2.95 mm x 2.80 mm
SN74LVC2G32DCU	VSSOP (8)	2.30 mm x 2.00 mm
SN74LVC2G32YZP	DSBGA (8)	1.91 mm x 0.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram (Positive Logic)



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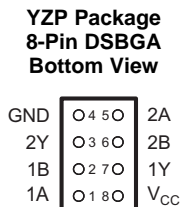
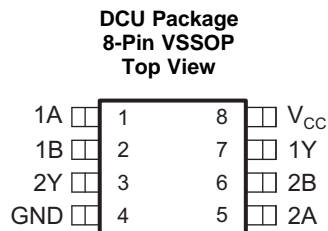
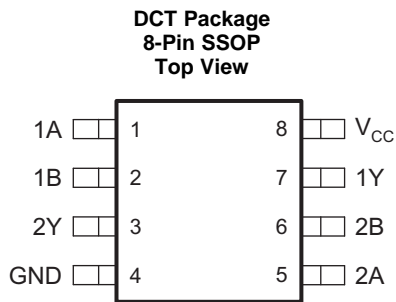
## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision M (November 2013) to Revision N</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>• Added <i>Applications</i> section, <i>Device Information</i> table, <i>Pin Configuration and Functions</i> section, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Feature Description</i> section, <i>Device Functional Modes</i>, <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....</li> </ul>	<b>1</b>

<b>Changes from Revision L (February 2007) to Revision M</b>	<b>Page</b>
<ul style="list-style-type: none"> <li>• Updated document to new TI data sheet format .....</li> <li>• Removed <i>Ordering Information</i> table .....</li> <li>• Updated <i>Features</i> .....</li> <li>• Updated operating temperature range .....</li> </ul>	<b>1</b> <b>1</b> <b>1</b> <b>5</b>

## 5 Pin Configuration and Functions



See mechanical drawing for dimensions

### Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	I	Input for first OR gate
1B	2	I	Input for first OR gate
1Y	7	O	Output for first OR gate
2A	5	I	Input for second OR gate
2B	6	I	Input for second OR gate
2Y	3	O	Output for second OR gate
GND	4	—	Ground
V <sub>CC</sub>	8	—	Power

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage range	-0.5	6.5	V
V <sub>I</sub>	Input voltage range <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	6.5	V
V <sub>O</sub>	Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>	-0.5	V <sub>CC</sub> + 0.5	V
I <sub>IK</sub>	Input clamp current	V <sub>I</sub> < 0	-50	mA
I <sub>OK</sub>	Output clamp current	V <sub>O</sub> < 0	-50	mA
I <sub>O</sub>	Continuous output current		±50	mA
	Continuous current through V <sub>CC</sub> or GND		±100	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The value of V<sub>CC</sub> is provided in the *Recommended Operating Conditions* table.

### 6.2 ESD Ratings

PARAMETER	DEFINITION	VALUE	UNIT
V <sub>(ESD)</sub>	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins <sup>(1)</sup>	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins <sup>(2)</sup>	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions<sup>(1)</sup>

			MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	Operating	1.65	5.5	V
		Data retention only	1.5		
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.65 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	1.7		
		V <sub>CC</sub> = 3 V to 3.6 V	2		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.7 × V <sub>CC</sub>		
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 1.65 V to 1.95 V	0.35 × V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.3 V to 2.7 V	0.7		
		V <sub>CC</sub> = 3 V to 3.6 V	0.8		
		V <sub>CC</sub> = 4.5 V to 5.5 V	0.3 × V <sub>CC</sub>		
V <sub>I</sub>	Input voltage		0	5.5	V
V <sub>O</sub>	Output voltage		0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 1.65 V	–4		mA
		V <sub>CC</sub> = 2.3 V	–8		
		V <sub>CC</sub> = 3 V	–16		
			–24		
		V <sub>CC</sub> = 4.5 V	–32		
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 1.65 V	4		mA
		V <sub>CC</sub> = 2.3 V	8		
		V <sub>CC</sub> = 3 V	16		
			24		
		V <sub>CC</sub> = 4.5 V	32		
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V	20		ns/V
		V <sub>CC</sub> = 3.3 V ± 0.3 V	10		
		V <sub>CC</sub> = 5 V ± 0.5 V	5		
T <sub>A</sub>	Operating free-air temperature	DCT and DCU packages	–40	125	°C
		YZP package	–40	85	

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	SN74LVC2G32			UNIT	
	DCT (SSOP)	DCU (VSSOP)	YZP (DSBGA)		
	8 PINS	8 PINS	8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	220	227	102	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	–40°C to 85°C			–40°C to 125°C			UNIT
			MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –100 μA	1.65 V to 5.5 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –4 mA	1.65 V	1.2			1.2			
	I <sub>OH</sub> = –8 mA	2.3 V	1.9			1.9			
	I <sub>OH</sub> = –16 mA	3 V	2.4			2.4			
	I <sub>OH</sub> = –24 mA		2.3			2.3			
	I <sub>OH</sub> = –32 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 100 μA	1.65 V to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 4 mA	1.65 V	0.45			0.45			
	I <sub>OL</sub> = 8 mA	2.3 V	0.3			0.3			
	I <sub>OL</sub> = 16 mA	3 V	0.4			0.4			
	I <sub>OL</sub> = 24 mA		0.55			0.6			
	I <sub>OL</sub> = 32 mA	4.5 V	0.55			0.6			
I <sub>I</sub> A or B inputs	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	±5			±5			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 5.5 V	0	±10			±10			μA
I <sub>CC</sub>	V <sub>I</sub> = 5.5 V or GND, I <sub>O</sub> = 0	1.65 V to 5.5 V	10			10			μA
ΔI <sub>CC</sub>	One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND	3 V to 5.5 V	500			500			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	5			5			pF

 (1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

## 6.6 Switching Characteristics

 over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 2](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEMPERATURE	V <sub>CC</sub> = 1.8 V ± 0.15 V		V <sub>CC</sub> = 2.5 V ± 0.2 V		V <sub>CC</sub> = 3.3 V ± 0.3 V		V <sub>CC</sub> = 5 V ± 0.5 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	A or B	Y	–40°C to 85°C	2.4	8	1	4.4	1	3.8	1	3.2	ns
			–40°C to 125°C	2.4	10	1	5.6	1	4.8	1	3.9	

## 6.7 Operating Characteristics

 T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	V <sub>CC</sub> = 1.8 V	V <sub>CC</sub> = 2.5 V	V <sub>CC</sub> = 3.3 V	V <sub>CC</sub> = 5 V	UNIT	
		TYP	TYP	TYP	TYP		
C <sub>pd</sub>	Power dissipation capacitance	f = 10 MHz	17	17	17	19	pF

## 6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

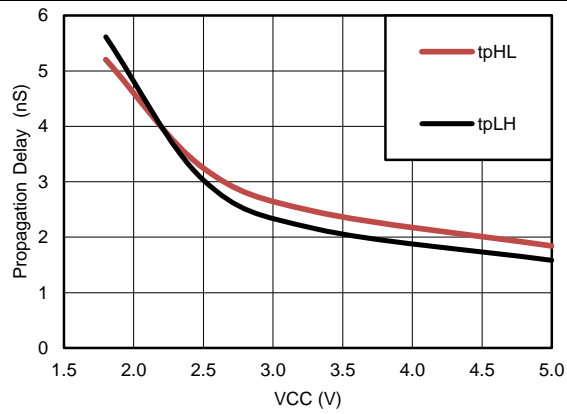
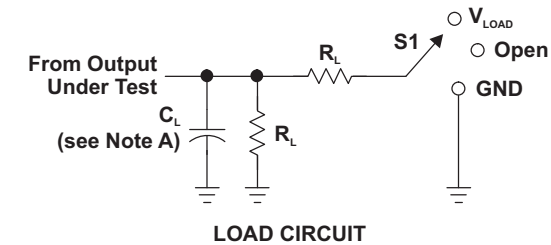


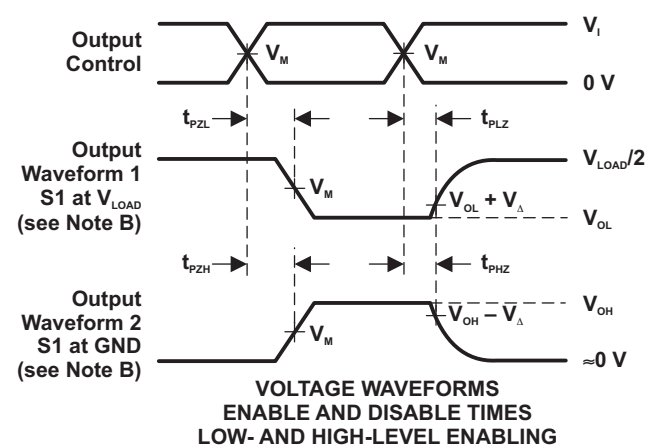
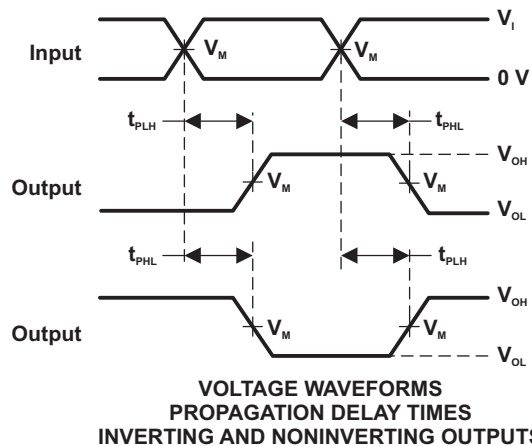
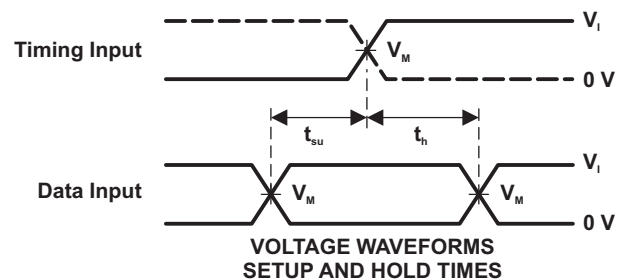
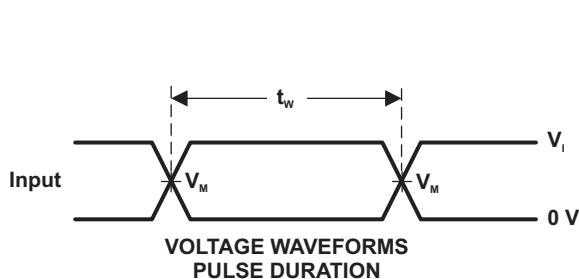
Figure 1. Propagation Delay vs.  $V_{CC}$

## 7 Parameter Measurement Information



TEST	S1
$t_{PLH}/t_{PHL}$	Open
$t_{PLZ}/t_{PZL}$	$V_{LOAD}$
$t_{PHZ}/t_{PZH}$	GND

$V_{CC}$	INPUTS		$V_M$	$V_{LOAD}$	$C_L$	$R_L$	$V_{\Delta}$
	$V_i$	$t_i/t_r$					
$1.8\text{ V} \pm 0.15\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k $\Omega$	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	$V_{CC}$	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 $\Omega$	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 $\Omega$	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	$V_{CC}$	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 $\Omega$	0.3 V



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq$  10 MHz,  $Z_o = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

**Figure 2. Load Circuit and Voltage Waveforms**



## 8 Detailed Description

### 8.1 Overview

The SN74LVC2G32 provides two logical OR gates per device and each gate has two inputs. Both input paths use identical circuitry for matching propagation delays. Supply voltage from 1.65 V to 5.5 V is supported.

### 8.2 Functional Block Diagram

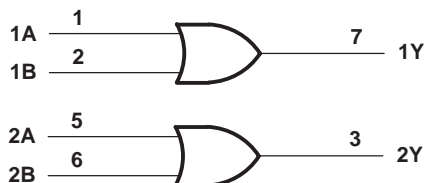


Figure 3. Logic Diagram (Positive Logic)

### 8.3 Feature Description

The SN74LVC2G32 inputs per gate can accept up to 5.5 V regardless of  $V_{CC}$ .

### 8.4 Device Functional Modes

Table 1 lists the functional modes for the SN74LVC2G32.

Table 1. Function Table (Each Gate)<sup>(1)</sup>

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

(1)  $Y = A + B$  in positive logic.

## 9 Application and Implementation

### NOTE

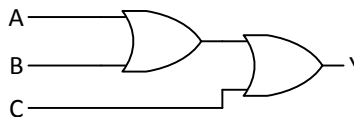
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The SN74LVC2G32 device is dual 2-input OR gate. High-output current capability is ideal for driving multiple outputs.

### 9.2 Typical Application

3-input OR configuration,  $Y = A + B + C$



**Figure 4. 3-input OR gate**

#### 9.2.1 Design Requirements

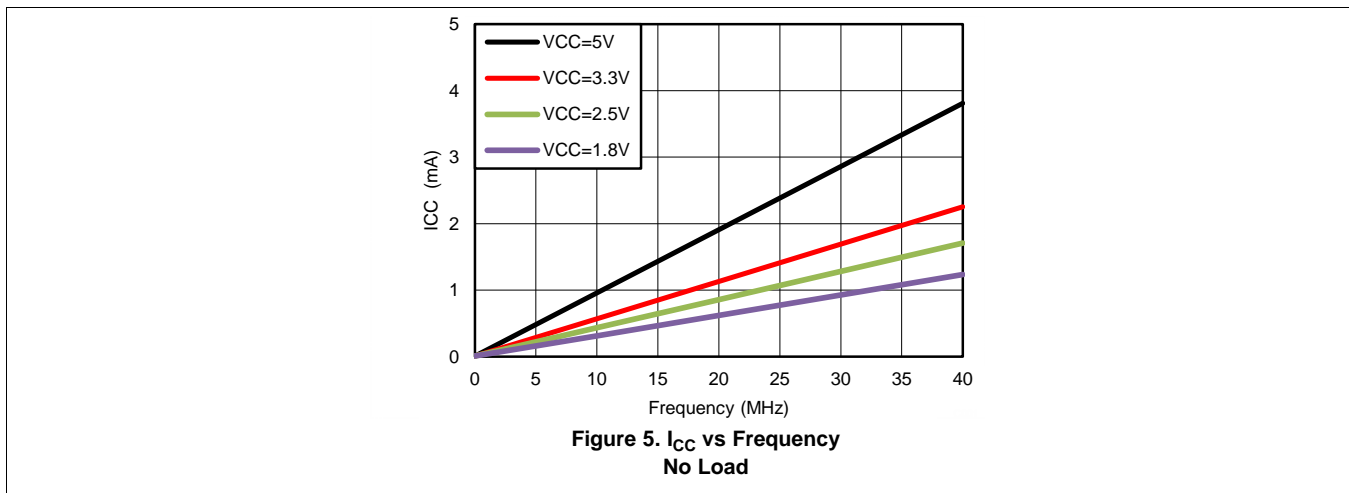
This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. Outputs can be combined to produce higher drive but the high drive will also create faster edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 9.2.2 Detailed Design Procedure

1. Recommended Input Conditions:
  - For rise time and fall time specifications, see  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#) table.
  - For specified high and low levels, see  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#) table.
  - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid  $V_{CC}$ .
2. Recommend Output Conditions:
  - Load currents should not exceed 50 mA per output and 100 mA total for the part.
  - Series resistors on the output may be used if the user desires to slow the output edge signal or limit the output current.

## Typical Application (continued)

### 9.2.3 Application Curve



## 10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#) table.

Each V<sub>CC</sub> terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, a 0.1-μF capacitor is recommended. If there are multiple V<sub>CC</sub> terminals then 0.01-μF or 0.022-μF capacitors are recommended for each power terminal. It is ok to parallel multiple bypass capacitors to reject different frequencies of noise. Multiple bypass capacitors may be paralleled to reject different frequencies of noise. The bypass capacitor should be installed as close to the power terminal as possible for the best results.

## 11 Layout

### 11.1 Layout Guidelines

When using multiple bit logic devices, inputs should not float. In many cases, functions or parts of functions of digital logic devices are unused. Some examples are when only two inputs of a triple-input AND gate are used, or when only 3 of the 4-buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states.

Specified in [Figure 6](#) are rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V<sub>CC</sub>, whichever makes more sense or is more convenient.

### 11.2 Layout Example

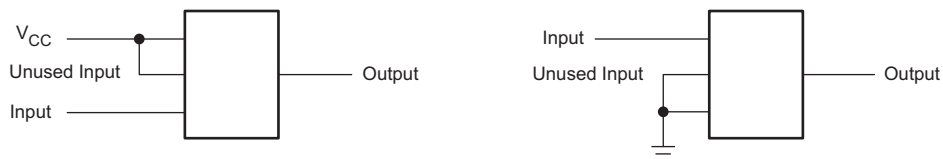


Figure 6. Layout Diagram

## 12 Device and Documentation Support

### 12.1 Related Documentation

For related documentation, see the following:

*Implications of Slow or Floating CMOS Inputs*, [SCBA004](#)

### 12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](#), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.3 Trademarks

NanoFree, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LVC2G32DCTR	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(2WQ5, C32) (R, Z)	<a href="#">Samples</a>
SN74LVC2G32DCTRE4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2WQ5, C32) (R, Z)	<a href="#">Samples</a>
SN74LVC2G32DCTRG4	ACTIVE	SM8	DCT	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	(2WQ5, C32) (R, Z)	<a href="#">Samples</a>
SN74LVC2G32DCUR	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C32J, C32Q, C32R)  CR	<a href="#">Samples</a>
SN74LVC2G32DCURE4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C32R	<a href="#">Samples</a>
SN74LVC2G32DCURG4	ACTIVE	VSSOP	DCU	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	C32R	<a href="#">Samples</a>
SN74LVC2G32DCUT	ACTIVE	VSSOP	DCU	8	250	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-40 to 125	(C32J, C32Q, C32R)  CR	<a href="#">Samples</a>
SN74LVC2G32YZPR	ACTIVE	DSBGA	YZP	8	3000	RoHS & Green	SNAGCU	Level-1-260C-UNLIM	-40 to 85	CGN	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LVC2G32 :**

- Automotive : [SN74LVC2G32-Q1](#)
- Enhanced Product : [SN74LVC2G32-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LVC2G32DCTR	SM8	DCT	8	3000	180.0	13.0	3.35	4.5	1.55	4.0	12.0	Q3
SN74LVC2G32DCTR	SM8	DCT	8	3000	180.0	12.4	3.15	4.35	1.55	4.0	12.0	Q3
SN74LVC2G32DCUR	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G32DCUR	VSSOP	DCU	8	3000	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G32DCURG4	VSSOP	DCU	8	3000	180.0	8.4	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G32DCUT	VSSOP	DCU	8	250	178.0	9.0	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G32DCUT	VSSOP	DCU	8	250	178.0	9.5	2.25	3.35	1.05	4.0	8.0	Q3
SN74LVC2G32YZPR	DSBGA	YZP	8	3000	178.0	9.2	1.02	2.02	0.63	4.0	8.0	Q1

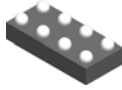
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LVC2G32DCTR	SM8	DCT	8	3000	182.0	182.0	20.0
SN74LVC2G32DCTR	SM8	DCT	8	3000	190.0	190.0	30.0
SN74LVC2G32DCUR	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G32DCUR	VSSOP	DCU	8	3000	180.0	180.0	18.0
SN74LVC2G32DCURG4	VSSOP	DCU	8	3000	202.0	201.0	28.0
SN74LVC2G32DCUT	VSSOP	DCU	8	250	180.0	180.0	18.0
SN74LVC2G32DCUT	VSSOP	DCU	8	250	202.0	201.0	28.0
SN74LVC2G32YZPR	DSBGA	YZP	8	3000	220.0	220.0	35.0



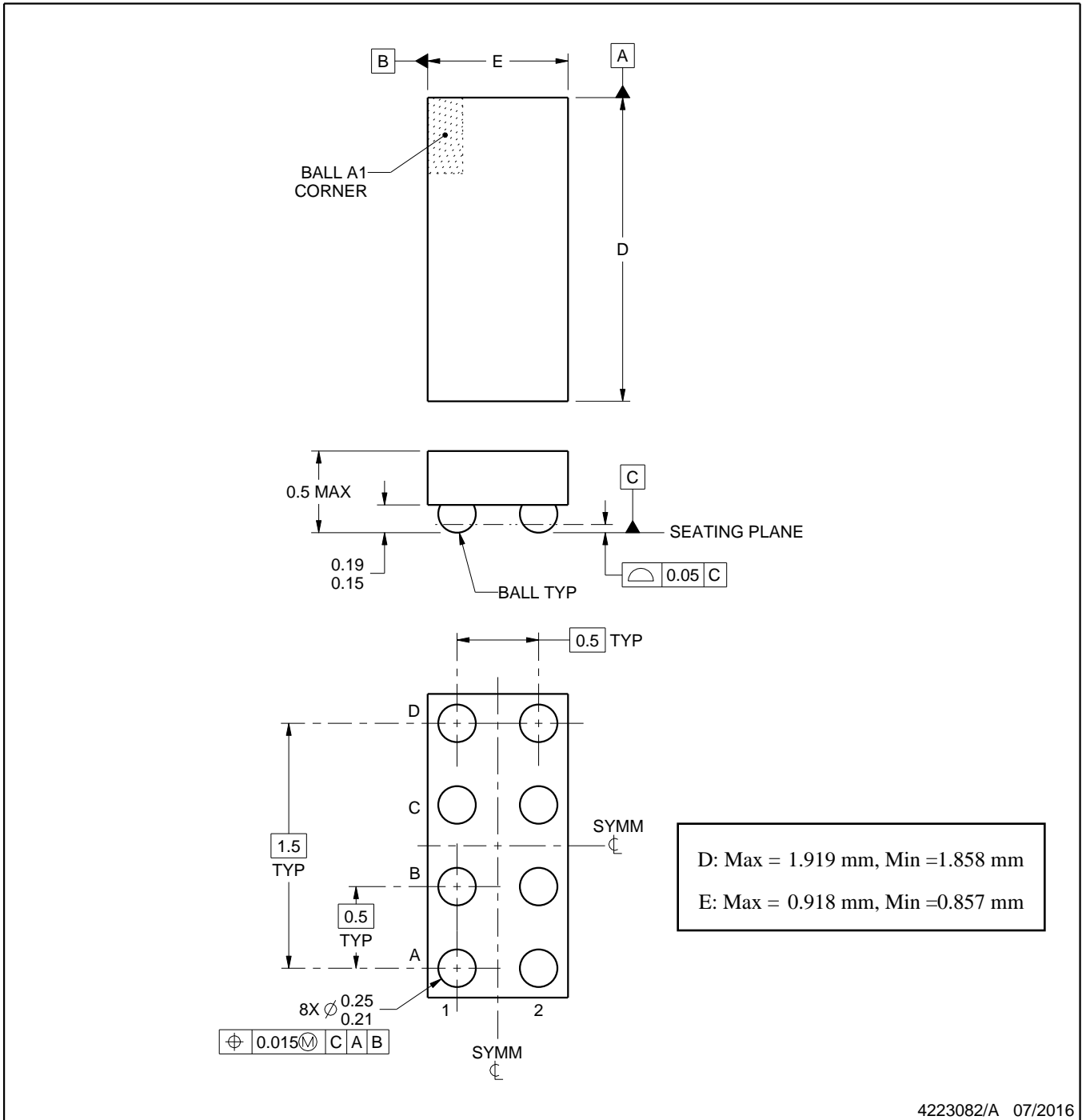
YZP0008



PACKAGE OUTLINE

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

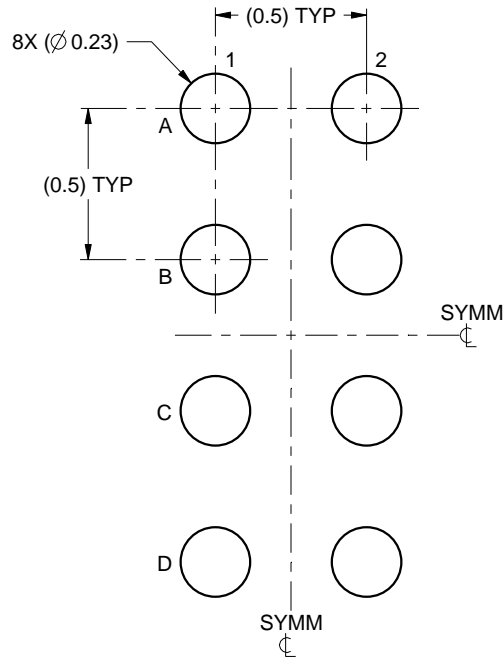
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.

# EXAMPLE BOARD LAYOUT

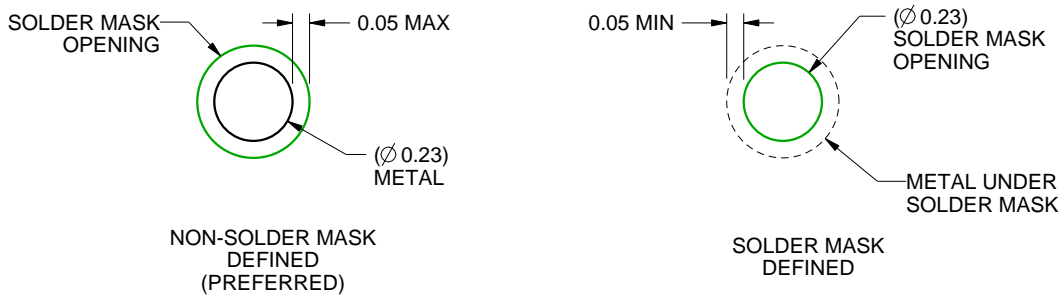
YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE  
SCALE:40X



SOLDER MASK DETAILS  
NOT TO SCALE

4223082/A 07/2016

NOTES: (continued)

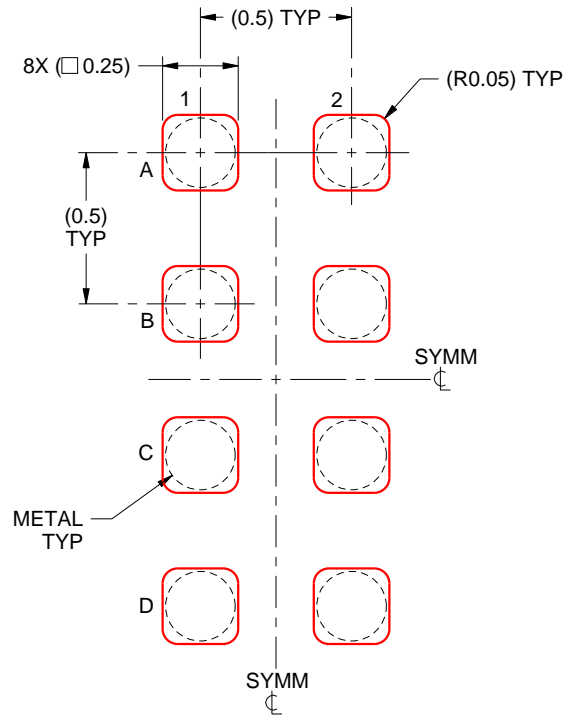
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SNVA009 ([www.ti.com/lit/snva009](http://www.ti.com/lit/snva009)).

# EXAMPLE STENCIL DESIGN

YZP0008

DSBGA - 0.5 mm max height

DIE SIZE BALL GRID ARRAY

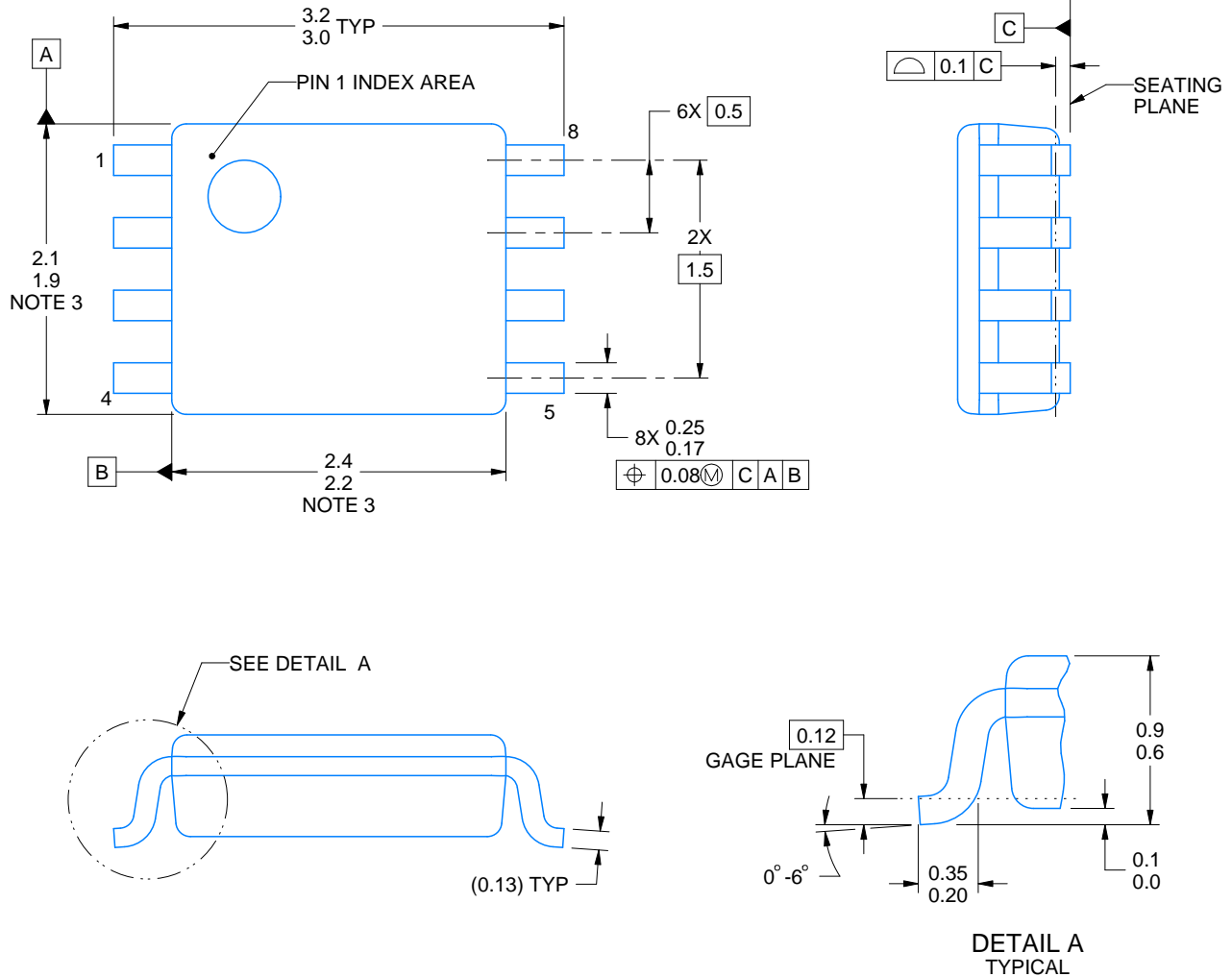


SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE:40X

4223082/A 07/2016

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



4225266/A 09/2014

NOTES:

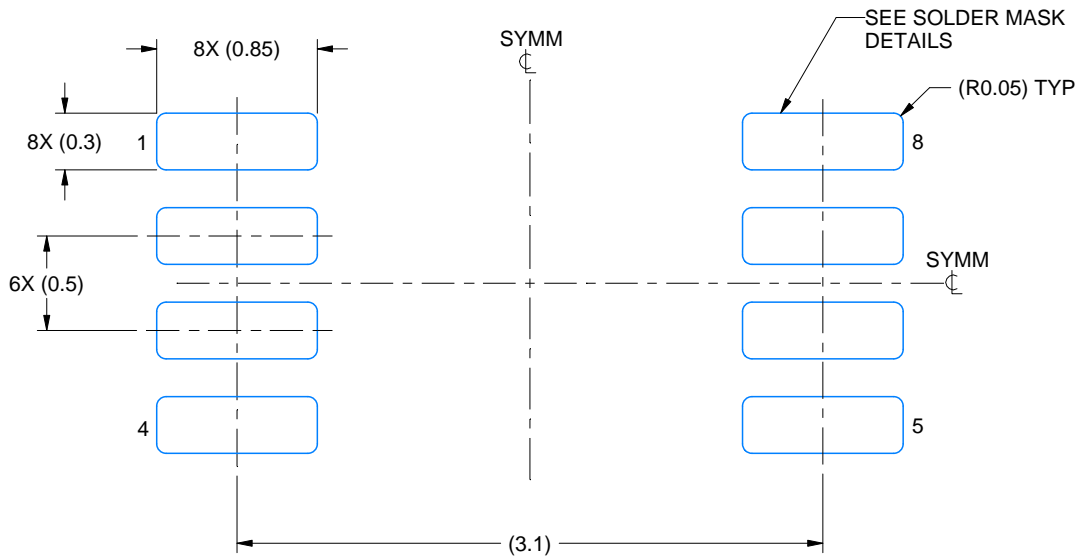
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-187 variation CA.

# EXAMPLE BOARD LAYOUT

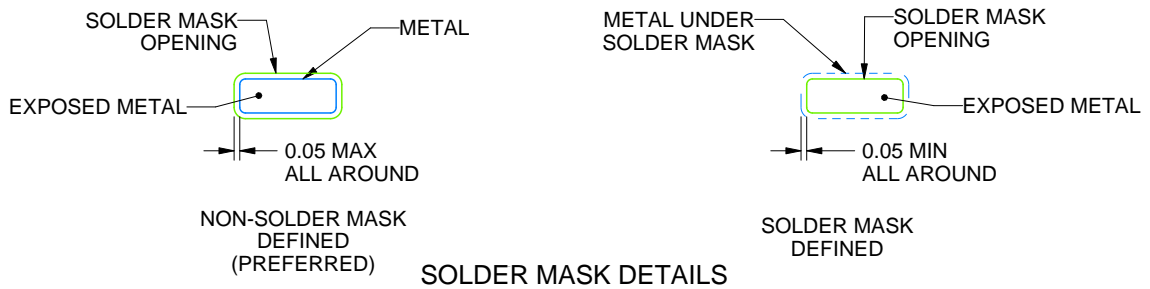
DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 25X



4225266/A 09/2014

NOTES: (continued)

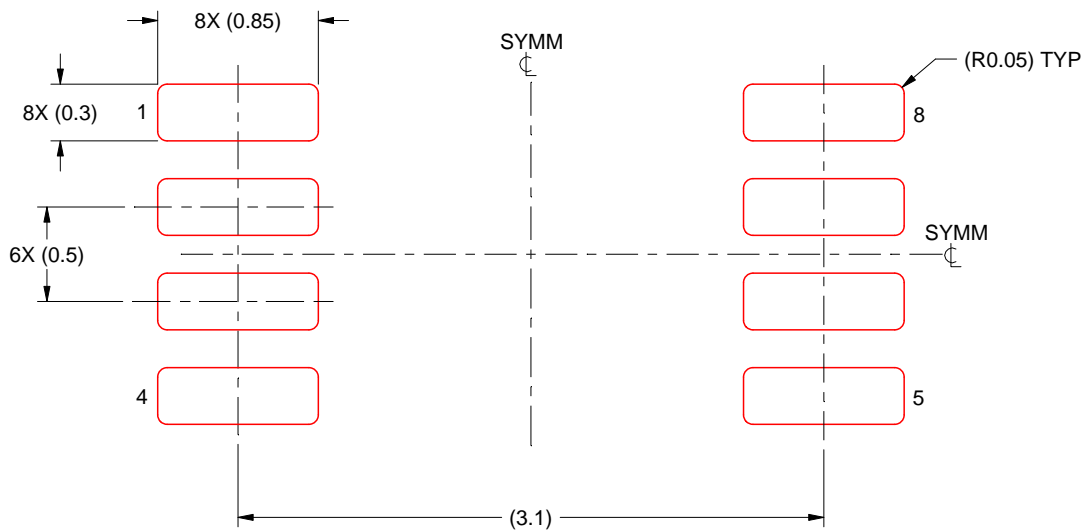
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DCU0008A

VSSOP - 0.9 mm max height

SMALL OUTLINE PACKAGE

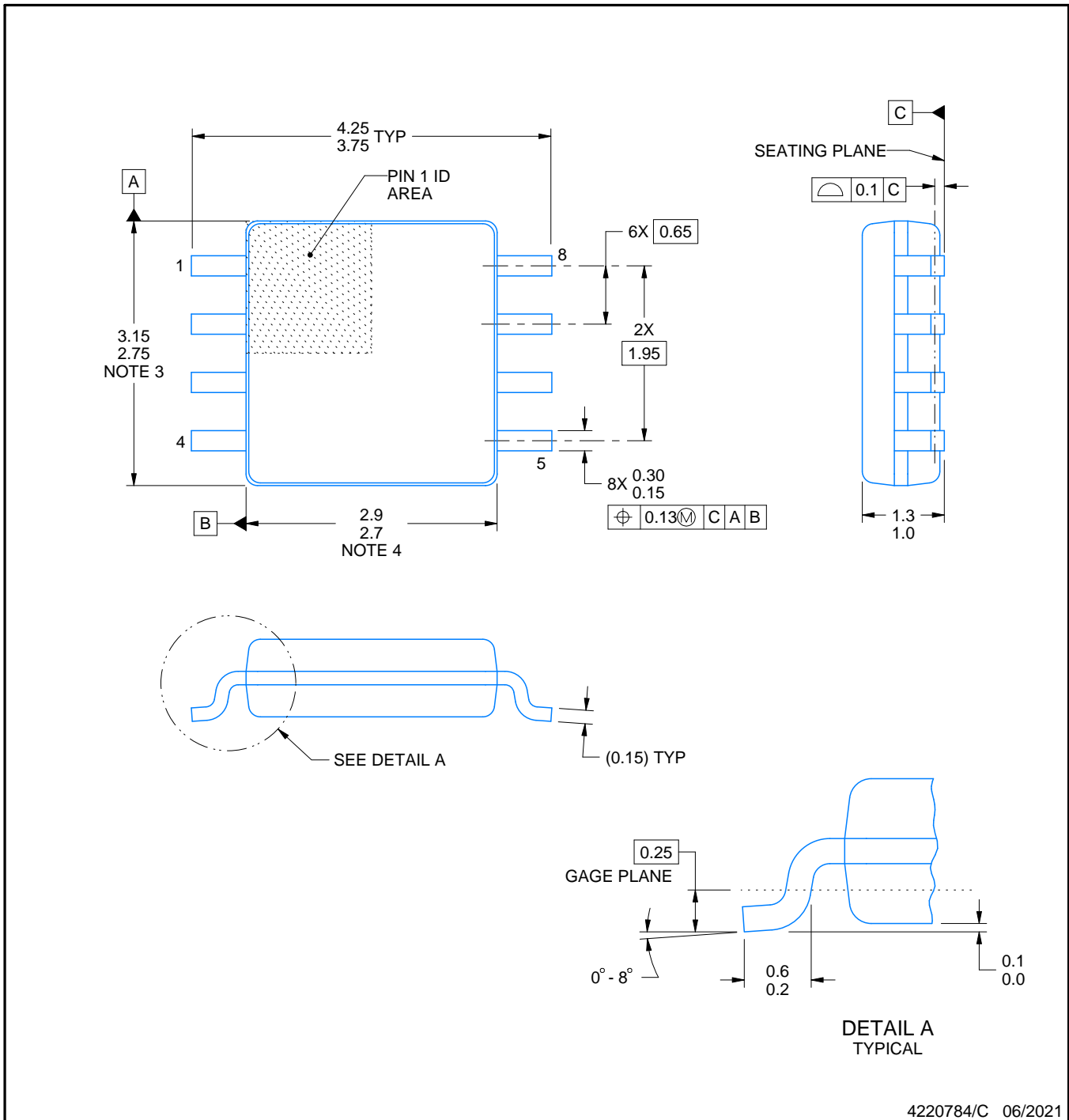
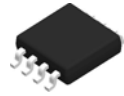


SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 25X

4225266/A 09/2014

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



4220784/C 06/2021

NOTES:

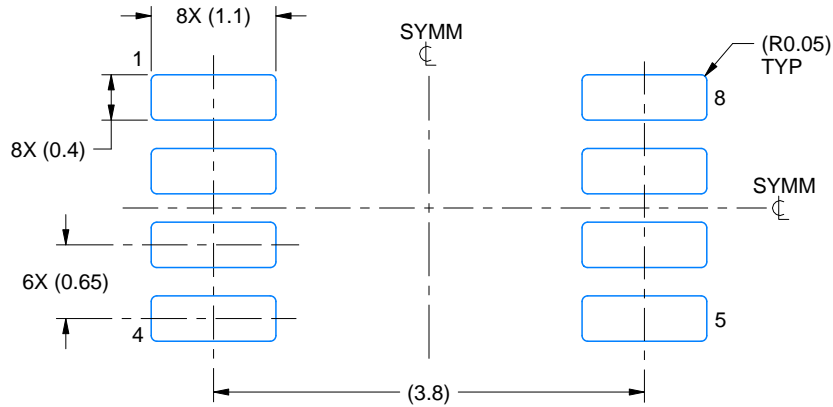
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.

# EXAMPLE BOARD LAYOUT

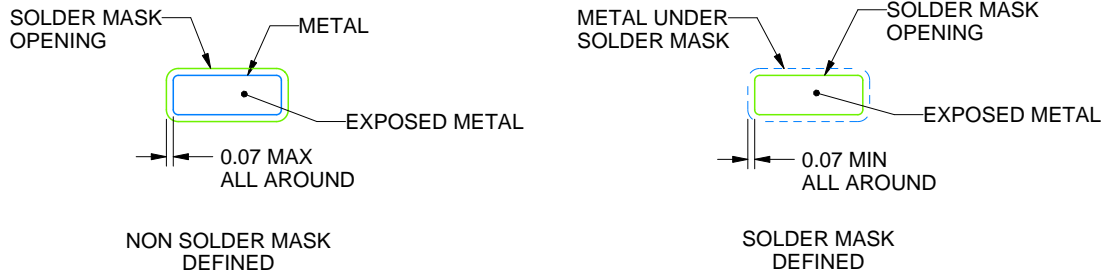
DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4220784/C 06/2021

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

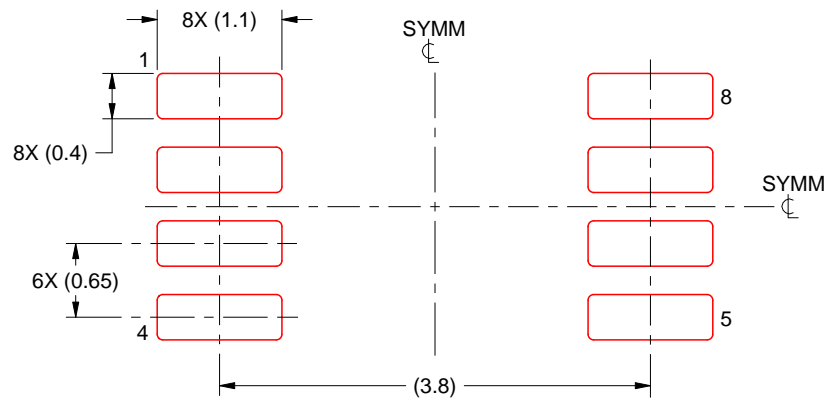


# EXAMPLE STENCIL DESIGN

DCT0008A

SSOP - 1.3 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4220784/C 06/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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