Low-Power Differential Line Driver and Receiver Pairs

1 Features

- Designed for high-speed multipoint data transmission over long cables
- Operates with pulse widths as low as 30 ns
- Low supply current: 5 mA max
- Meets or exceeds the standard requirementsof ANSI RS-485 and ISO 8482:1987(E)
- Common-mode voltage range of − 7 V to 12 V
- Positive-and negative-output current limiting
- Driver thermal shutdown protection
- Pin compatible with the SN75179B

2 Description

The SN65LBC179, SN65LBC179Q, and SN75LBC179 differential driver and receiver pairs are monolithic integrated circuits designed for bidirectional data communication over long cables that take on the characteristics of transmission lines. The devices are balanced, or differential, voltage mode devices that meet or exceed the requirements of industry standards ANSIRS-485 and ISO 8482:1987(E). Both devices are designed using TI's proprietary LinBiCMOS™ with the low power consumption of CMOS and the precision and robustness of bipolar transistors in the same circuit.

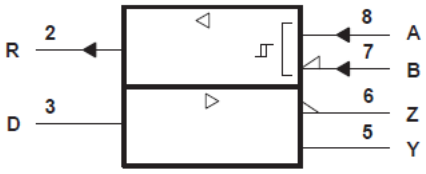
The SN65LBC179, SN65LBC179Q, and SN75LBC179 combine a differential line driver and differential line receiver and operate from a single 5-V supply. The driver differential outputs and the receiver differential inputs are connected to separate terminals for full-duplex operation and are designed to present minimum loading to the bus when powered off (V_{CC} = 0). These parts feature a wide common-mode voltage range making them suitable for point-to-point or multipoint data bus applications. The devices also provide positive and negative-current limiting and thermal shutdown for protection from line fault conditions. The line driver shuts down at a junction temperature of approximately 172°C.

The SN65LBC179, SN65LBC179Q, and SN75LBC179 are available in the 8-pin dual-in-line and small-outline packages. The SN75LBC179 is characterized for operation over the commercial temperature range of 0°C to 70°C. The SN65LBC179 is characterized over the industrial temperature range of −40°C to 85°C. The SN65LBC179Q is characterized over the extended industrial or automotive temperature range of −40°C to 125°C.

Package Information

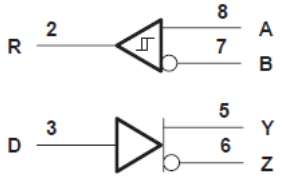
PART NUMBER	PACKAGE(1)	BODY SIZE (NOM)
SN75179B	D (SOIC)	4.9 mm x 3.91 mm
	P (PDIP)	9.81 mm x 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



A. This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Logic Symbol



Logic Diagram (Positive Logic)

Table of Contents

3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (April 2006) to Revision G (October 2022)	Page
• Changed the data sheet format to the latest data sheet format	1
• Added the *Thermal Information* table	5

4 Pin Configuration and Functions

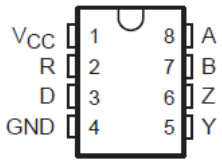


Figure 4-1. D or P Package (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
1	V_{CC}	P	5 V Voltage Supply
2	R	O	RS485 Logic Output
3	D	I	RS485 Logic Input
4	GND	G	Ground
5	Y	O	Non-Inverting RS485 Bus Output
6	Z	O	Inverted RS485 Bus Output
7	B	I	Inverted RS485 Bus Input
8	A	I	Non-Inverting RS485 Bus Input

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

5 Specifications

5.1 Absolute Maximum Ratings

See note (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage range	-0.3	7	V
	Voltage range at A, B, Y, or Z(2)	-10	15	V
	Voltage range at D or R(2)	-0.3	V_{CC} + 0.5	V
I_O	Receiver output current		±10	mA
	Continuous total power dissipation(3)	Internally limited		
$P_{(AVG)}$	Average power dissipation R_L = 54 Ω, input to D is 10 Mbps 50% duty cycle square wave, V_{CC} = 5.25 V, T_J = 130°C		330	mW
T_{SD}	Thermal shutdown junction temperature		165	°C
	Total power dissipation	See Section 5.4		

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The maximum operating junction temperature is internally limited. Uses the dissipation rating table to operate below this temperature.

5.2 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage	D	2			V
V_{IL}	Low-level input voltage	D			0.8	V
V_{ID}	Differential input voltage		−6(1)		6	V
V_O, V_I, or V_{IC}	Voltage at any bus terminal (separately or common-mode)	A, B, Y, or Z	−7		12	V
I_{OH}	High-level output current	Y or Z			−60	mA
		R			−8	
I_{OL}	Low-level output current	Y or Z			60	mA
		R			8	
T_J	Junction temperature				140	°C
T_A	Operating free-air temperature	SN65LBC179	−40		85	°C
		SN65LBC179Q	−40		125	
		SN75LBC179	0		70	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum, is used in this data sheet for differential input voltage, voltage at any bus terminal (separately or common mode), operating temperature, input threshold voltage, and common-mode output voltage.

5.3 Thermal Information

THERMAL METRIC[1]		D (SOIC)	P (PDIP)	UNIT
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	65.6.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	63.4	54.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	56.3	42.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	22.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	41.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	n/a	°C/W

(1) See TI application note literature number SZZA003, Package Thermal Characterization Methodologies, for an explanation of this parameter.

5.4 Dissipation Rating Table

PACKAGE	THERMAL MODEL	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING
D	Low K[1]	526 mW	5.0 mW/°C	301 mW	226 mW
		882 mW	8.4 mW/°C	504 mW	378 mW
P	High K[2]	840 mW	8.0 mW/°C	480 mW	360 mW

(1) In accordance with the low effective thermal conductivity metric definitions of EIA/JESD 51−3.
(2) In accordance with the high effective thermal conductivity metric definitions of EIA/JESD 51−7.

5.5 Electrical Characteristics - Driver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I= − 18 mA				−1.5	V
$\|V_{OD}\|$	Differential output voltage(2)	R_L = 54 Ω See Figure 6-1	SN65LBC179, SN65LBC179Q	1.1	2.2	5	V
			SN75LBC179	1.5	2.2	5	
		R_L = 60 Ω See Figure 6-2	SN65LBC179, SN65LBC179Q	1.1	2.2	5	
			SN75LBC179	1.5	2.2	5	
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)	See Figure 6-1 and Figure 6-2				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω	See Figure 6-1	1	2.5	3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)					±0.2	V
I_O	Output current with power off	V_{CC} = 0,	V_O = − 7 V to 12 V			±100	µA
I_{IH}	High-level input current	V_I = 2.4 V				−100	µA
I_{IL}	Low-level input current	V_I = 0.4 V				−100	µA
I_{OS}	Short-circuit output current	−7 V ≤ V_O ≤ 12 V				±250	mA
I_{CC}	Supply current	No load	SN65LBC179, SN75LBC179		4.2	5	mA
			SN65LBC179Q		4.2	7	mA

(1) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(2) The minimum V_{OD} specification of the SN65179 may not fully comply with ANSI RS-485 at operating temperatures below 0°C. System designers should take the possibly lower output signal into account in determining the maximum signal transmission distance.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in the steady-state magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.

5.6 Switching Characteristics - Driver

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω	See Figure 6-3	7	18	ns
$t_{t(OD)}$	Differential transition time			5	20	ns

5.7 Electrical Characteristics - Receiver

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = − 8 mA				0.2	V
V_{IT-}	Negative-going input threshold voltage	I_O = 8 mA		−0.2			V
V_{hys}	Hysteresis voltage (V_{IT+} − V_{IT-})				45		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV,	I_{OH} = − 8 mA	3.5	4.5		V
V_{OL}	Low-level output voltage	V_{ID} = − 200 mV,	I_{OL} = 8 mA		0.3	0.5	V
I_I	Bus input current	V_I = 12 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		0.7	1	mA
		V_{CC} = 5 V	SN65LBC179Q		0.7	1.2	mA
		V_I = 12 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		0.8	1	mA
		V_{CC} = 0 V	SN65LBC179Q		0.8	1.2	mA
		V_I = − 7 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		−0.5	−0.8	mA
		V_{CC} = 5 V	SN65LBC179Q		−0.5	−1.0	mA
		V_I = − 7 V, Other inputs at 0 V,	SN65LBC179, SN75LBC179		−0.5	−0.8	mA
		V_{CC} = 0 V	SN65LBC179Q		−0.5	−1.0	mA

5.8 Switching Characteristics - Receiver

V_{CC} = 5 V, T_A = 25°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PHL}	Propagation delay time, high- to low-level output	V_{ID} = −1.5 V to 1.5 V,	See Figure 6-4	15		30	ns
t_{PLH}	Propagation delay time, low- to high-level output			15		30	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 6-4			3	6	ns
t_t	Transition time				3	5	ns

5.9 Typical Characteristics

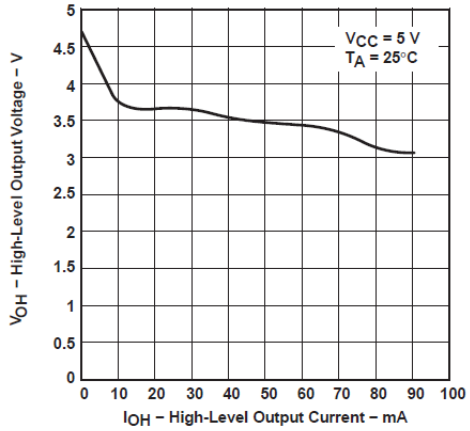


Figure 5-1. Driver High-Level Output Voltage vs High-Level Output Current

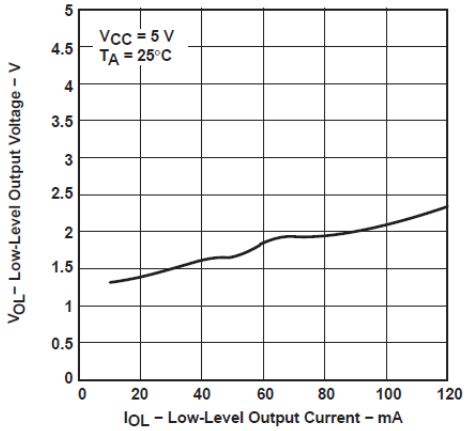


Figure 5-2. Driver Low-Level Output Voltage vs Low-Level Output Current

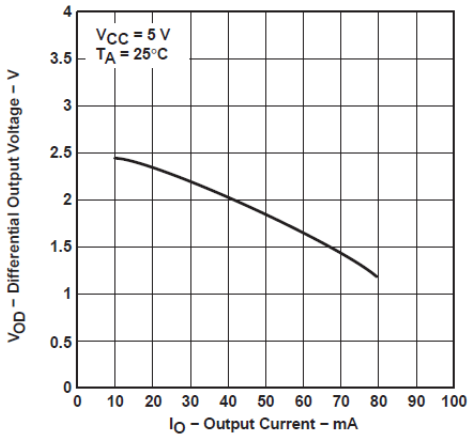


Figure 5-3. Driver Differential Output Voltage vs Output Current

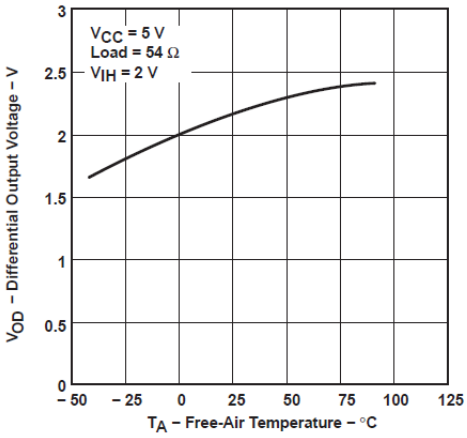


Figure 5-4. Driver Differential Output Voltage vs Free-Air Temperature

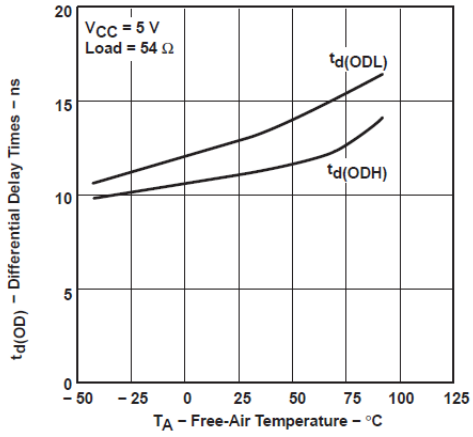


Figure 5-5. Driver Differential Delay Time vs Free-Air Temperature

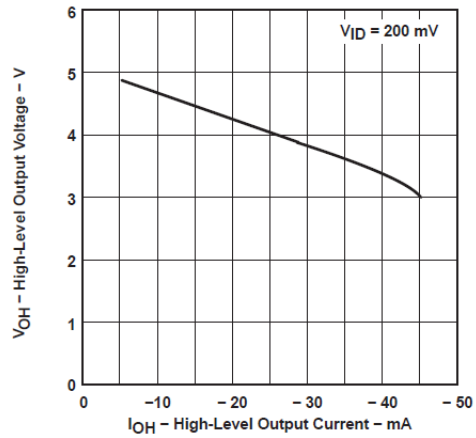


Figure 5-6. Receiver High-Level Output Voltage vs High-Level Output Current

5.9 Typical Characteristics (continued)

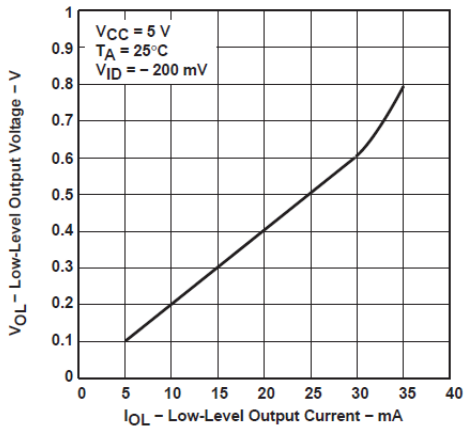


Figure 5-7. Receiver Low-Level Output Voltage vs Low-Level Output Current

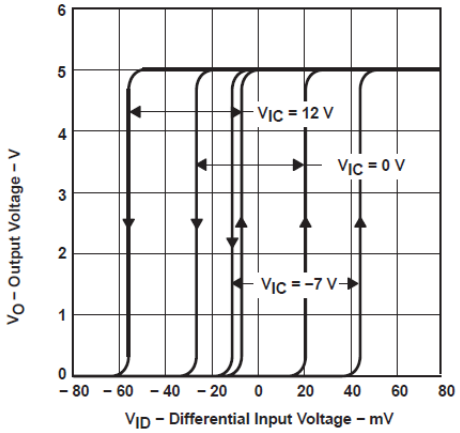


Figure 5-8. Receiver Output Voltage vs Differential Input Voltage

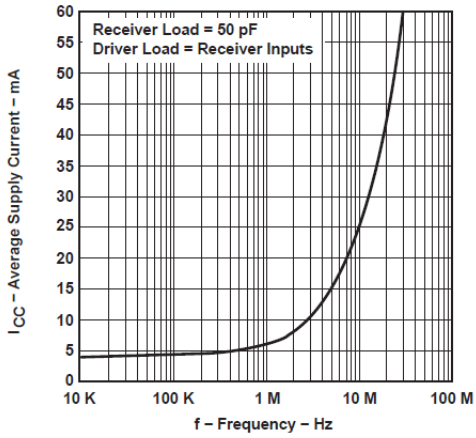


Figure 5-9. Average Supply Current vs Frequency

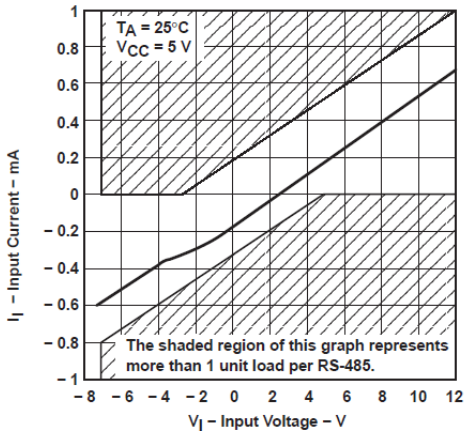


Figure 5-10. Receiver Input Current vs Input Voltage (Complementary Input at 0 V)

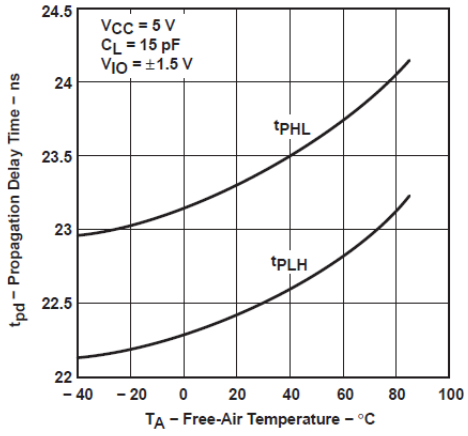


Figure 5-11. Receiver Propagation Delay Time vs Free-Air Temperature

6 Parameter Measurement Information

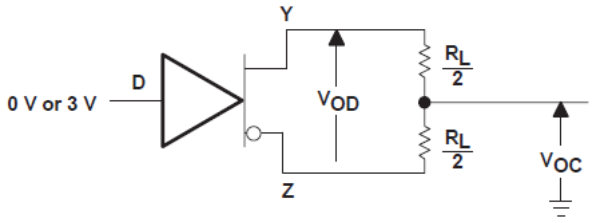


Figure 6-1. Differential and Common-Mode Output Voltage Test Circuit

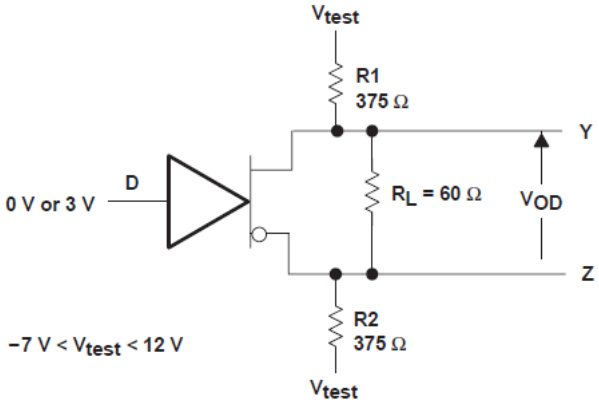
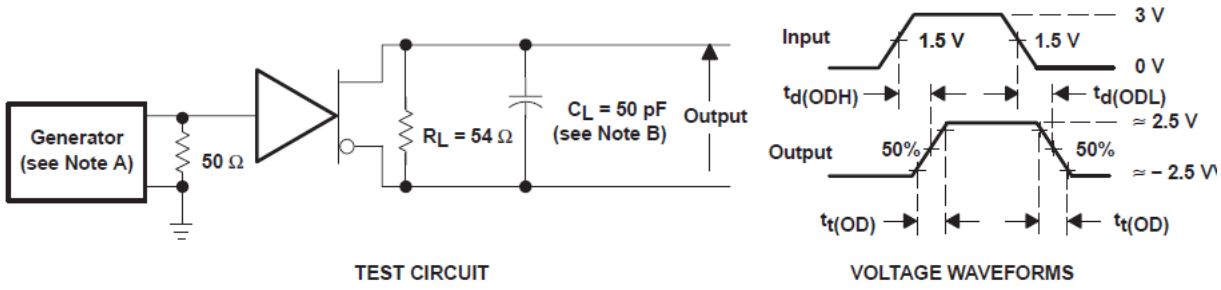


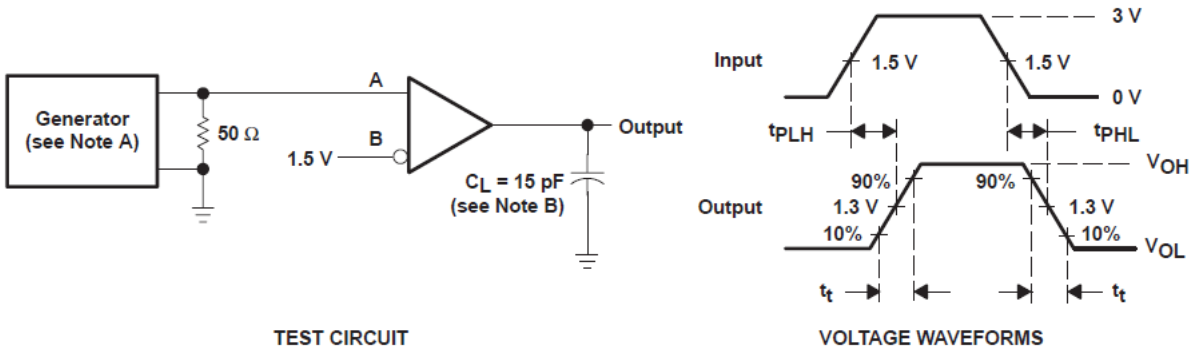
Figure 6-2. Differential Output Voltage Test Circuit



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-3. Driver Test Circuits and Differential Output Delay and Transition Time Voltage Waveforms



A. The input pulse is supplied by a generator having the following characteristics: PRR ≤ 1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f≤ 6 ns, Z_O = 50 Ω.

B. C_L includes probe and jig capacitance.

Figure 6-4. Receiver Test Circuit and Propagation Delay and Transition Time Voltage Waveforms

7 Detailed Description

7.1 Functional Block Diagram

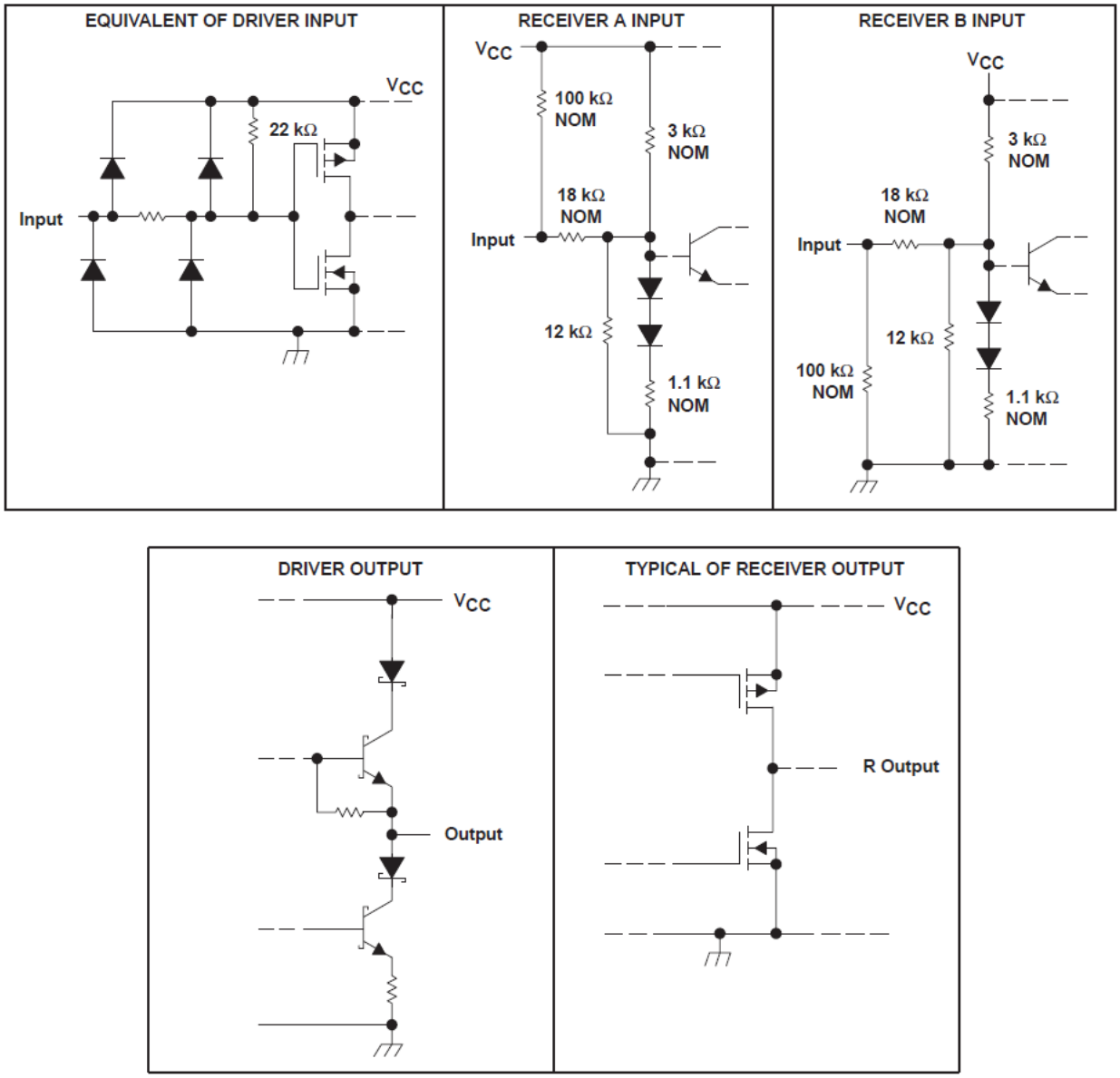


Figure 7-1. Schematics of Inputs and Outputs

7.2 Device Functional Modes

Function Tables

Table 7-1. Driver(1)

INPUT D	OUTPUTS	
	Y	Z
H	H	L
L	L	H

(1) H = high level, L = low level, ? = indeterminate

Table 7-2. Receiver[1]

DIFFERENTIAL INPUTS A−B	OUTPUT R
$V_{ID} \geq 0.2$ V	H
−0.2 V < V_{ID} < 0.2 V	?
$V_{ID} \leq -0.2$ V	L
Open circuit	H

(1) H = high level, L = low level, ? = indeterminate

7.3 Thermal Characteristics of IC Packages

θ_{JA} (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

θ_{JA} is not a constant and is a strong function of:

- the PCB design (50% variation
- altitude (20% variation)
- device power (5% variation

θ_{JA} can be used to compare the thermal performance of packages if the specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. θ_{JA} is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives *average* in-use condition thermal performance and consists of a single trace layer 25 mm long and 2-oz thick copper. The high-k board gives *best case* in−use condition and consists of two 1-oz buried power planes with a single trace layer 25 mm long with 2-oz thick copper. A 4% to 50% difference in θ_{JA} can be measured between these two test cards.

θ_{JC} (Junction-to-Case Thermal Resistance) is defined as difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from die, through the mold compound into the copper block.

θ_{JC} is a useful thermal characteristic when a heatsink is applied to package. It is not a useful characteristic to predict junction temperature as it provides pessimistic numbers if the case temperature is measured in a non-standard system and junction temperatures are backed out. It can be used with θ_{jb} in 1-dimensional thermal simulation of a package system.

θ_{JB} (Junction-to-Board Thermal Resistance) is defined to be the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold−plate structure. θ_{jb} is only defined for the high-k test card.

θ_{JB} provide an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system (see Figure 7-2).

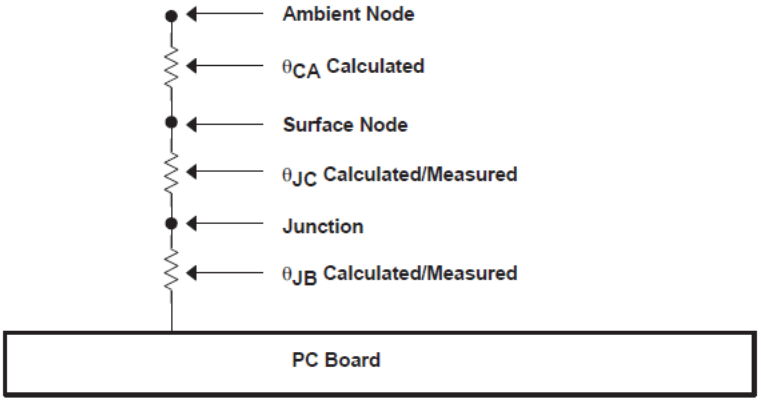


Figure 7-2. Thermal Resistance

8 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

8.1 Device Support

8.2 Documentation Support

8.2.1 Related Documentation

8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

8.5 Trademarks

LinBiCMOS™ is a trademark of LinBiCMOS.
TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65LBC179D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179	
SN65LBC179DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179	Samples
SN65LBC179DRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	6LB179	Samples
SN65LBC179P	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 85	65LBC179	
SN65LBC179QD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	
SN65LBC179QDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	
SN65LBC179QDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	Samples
SN65LBC179QDRG4	NRND	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LB179Q	
SN75LBC179D	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB179	
SN75LBC179DR	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB179	
SN75LBC179DRG4	LIFEBUY	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	7LB179	
SN75LBC179P	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	75LBC179	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

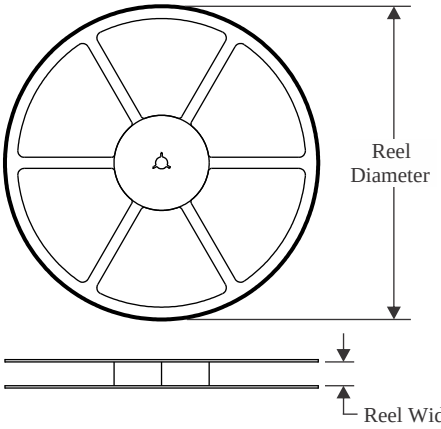
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

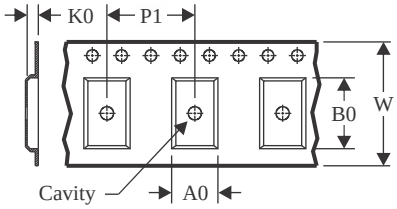
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

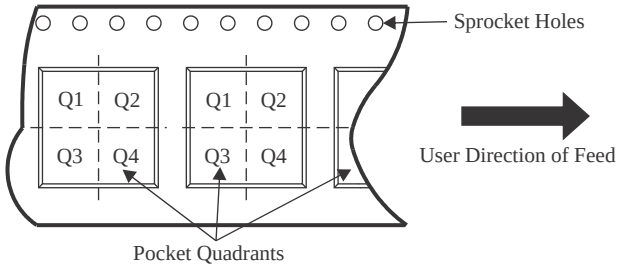


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

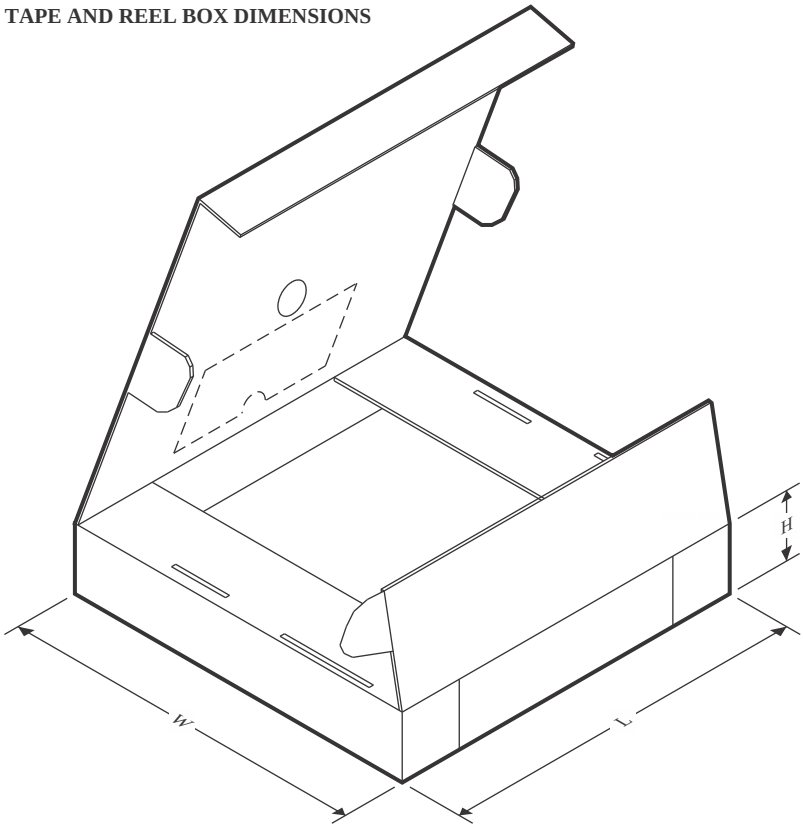
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65LBC179QDR	SOIC	D	8	2500	330.0	12.5	6.4	5.2	2.1	8.0	12.0	Q1
SN75LBC179DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

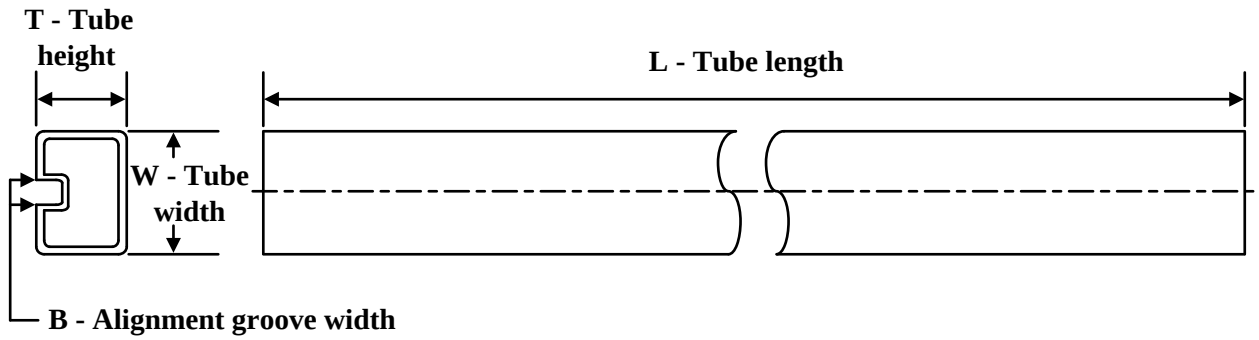
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

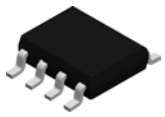
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65LBC179DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65LBC179QDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75LBC179DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65LBC179D	D	SOIC	8	75	507	8	3940	4.32
SN65LBC179P	P	PDIP	8	50	506	13.97	11230	4.32
SN65LBC179QD	D	SOIC	8	75	507	8	3940	4.32
SN65LBC179QDG4	D	SOIC	8	75	507	8	3940	4.32
SN75LBC179D	D	SOIC	8	75	507	8	3940	4.32
SN75LBC179P	P	PDIP	8	50	506	13.97	11230	4.32

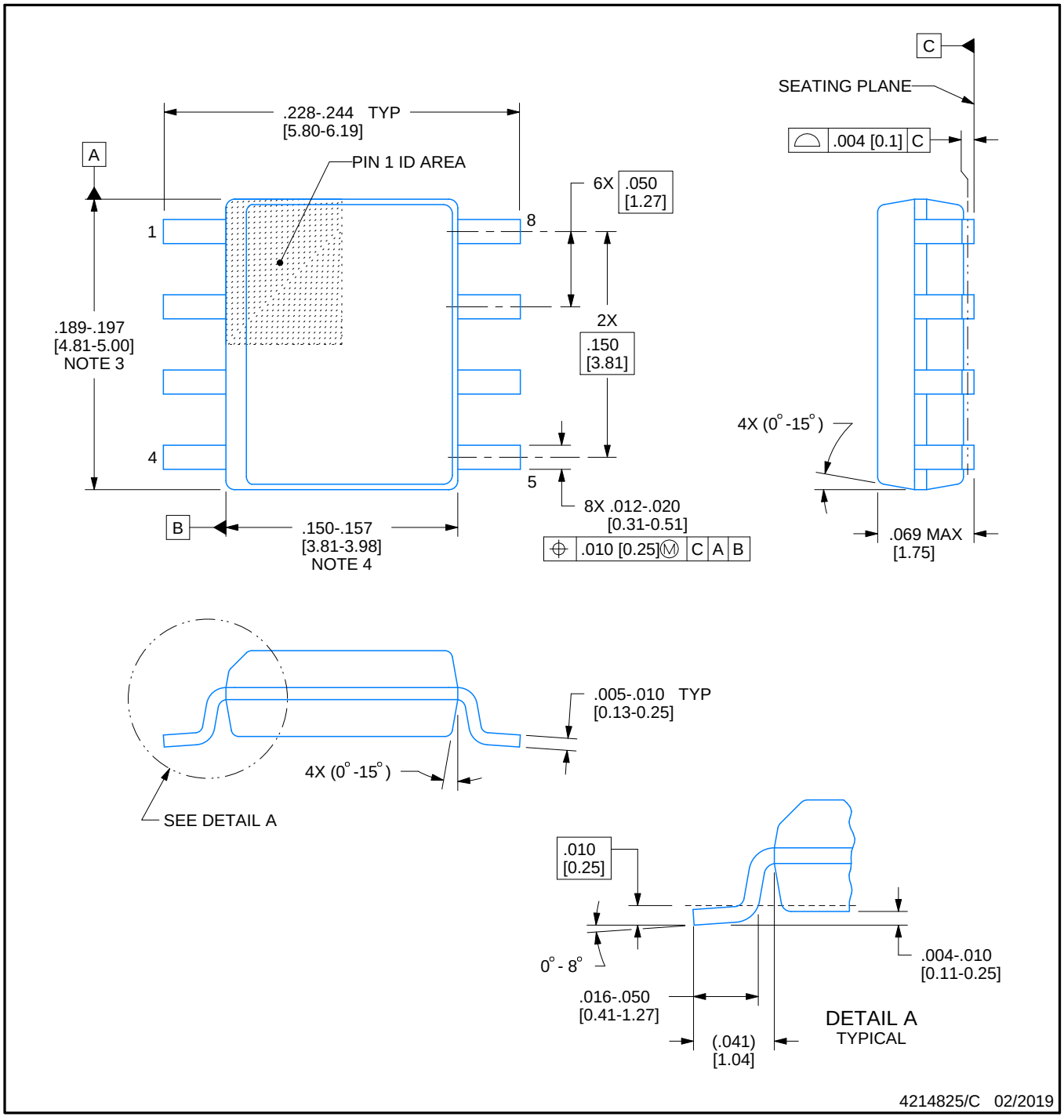


PACKAGE OUTLINE

D0008A

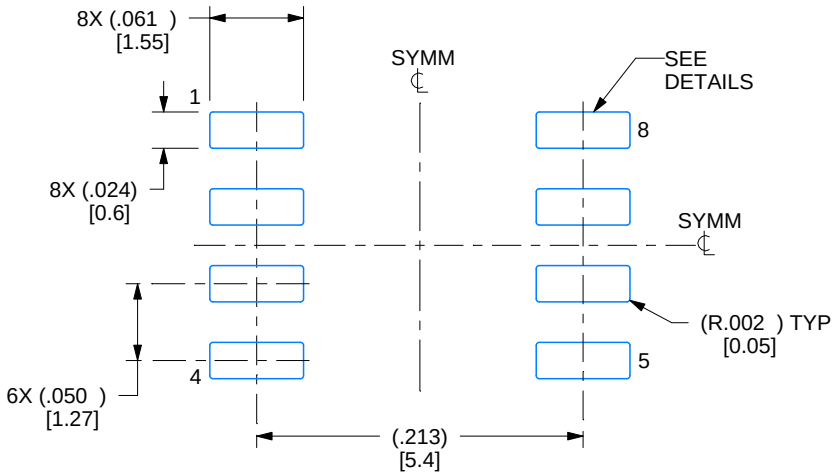
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

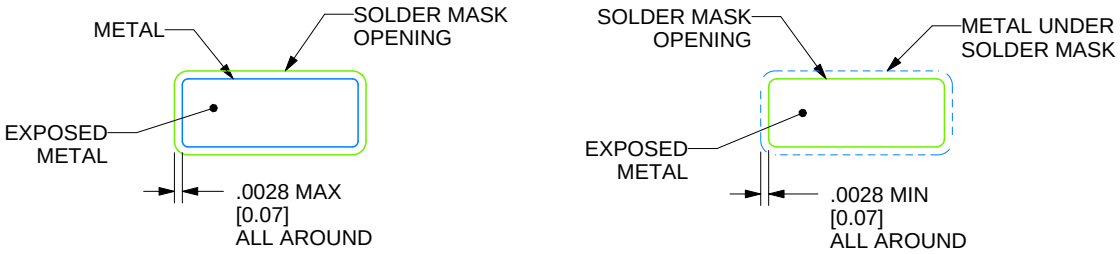


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

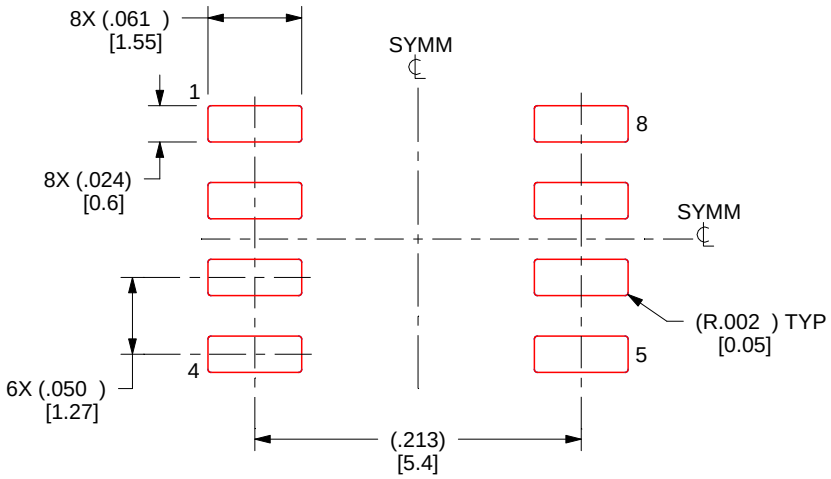
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



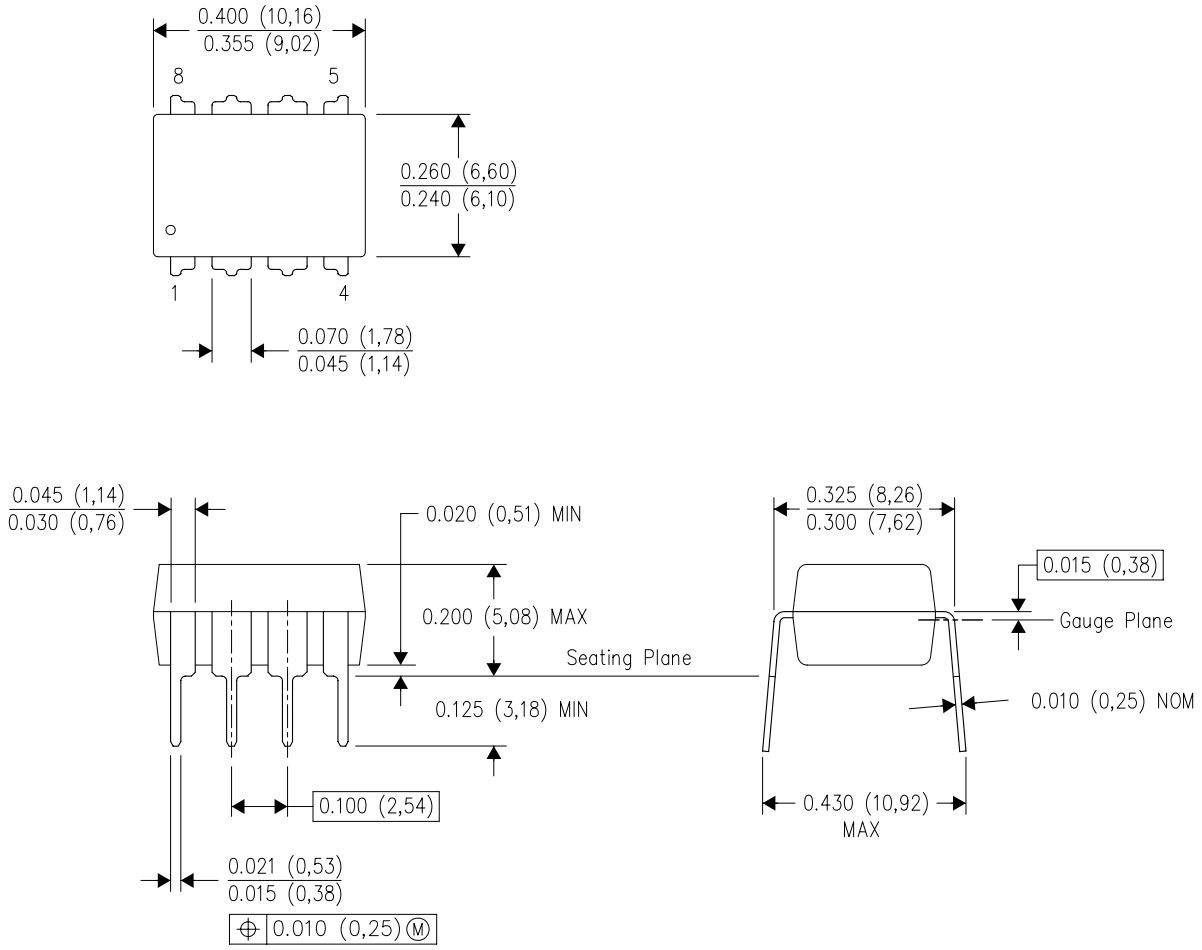
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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