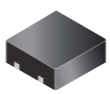
A3211 and A3212

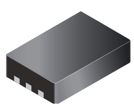
Micropower, Ultrasensitive Hall-Effect Switches

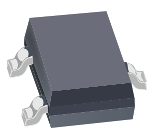
FEATURES AND BENEFITS

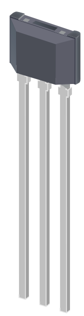
- Micropower operation
- Operation with north or south pole
- 2.5 to 3.5 V battery operation
- Chopper stabilized
  - □ Superior temperature stability
  - □ Extremely low switchpoint drift
  - □ Insensitive to physical stress
- High ESD protection
- Solid-state reliability
- Small size
- Easily manufacturable with magnet pole independence

Packages:


DFN (EL)


DFN (EH)


SOT23W (LH)


SIP (UA)

Not to scale

DESCRIPTION

The A3211 and A3212 integrated circuits are ultrasensitive, pole independent Hall-effect switches with latched digital output. These devices are especially suited for operation in battery-operated, hand-held equipment such as cellular and cordless telephones, pagers, and palmtop computers. A 2.5 to 3.5 V operation and a unique clocking scheme reduce the average operating power requirements to less than 15 µW with a 2.75 V supply.

Unlike other Hall-effect switches, either a north or south pole of sufficient strength will turn the output on in the A3212, and in the absence of a magnetic field, the output is off. The A3211 provides an inverted output. The polarity independence and minimal power requirements allow these devices to easily replace reed switches for superior reliability and ease of manufacturing, while eliminating the requirement for signal conditioning.

Improved stability is made possible through chopper stabilization (dynamic offset cancellation), which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress.

This device includes on a single silicon chip a Hall-voltage generator, small-signal amplifier, chopper stabilization, a latch, and a MOSFET output. Advanced CMOS processing is used to take advantage of low-voltage and low-power

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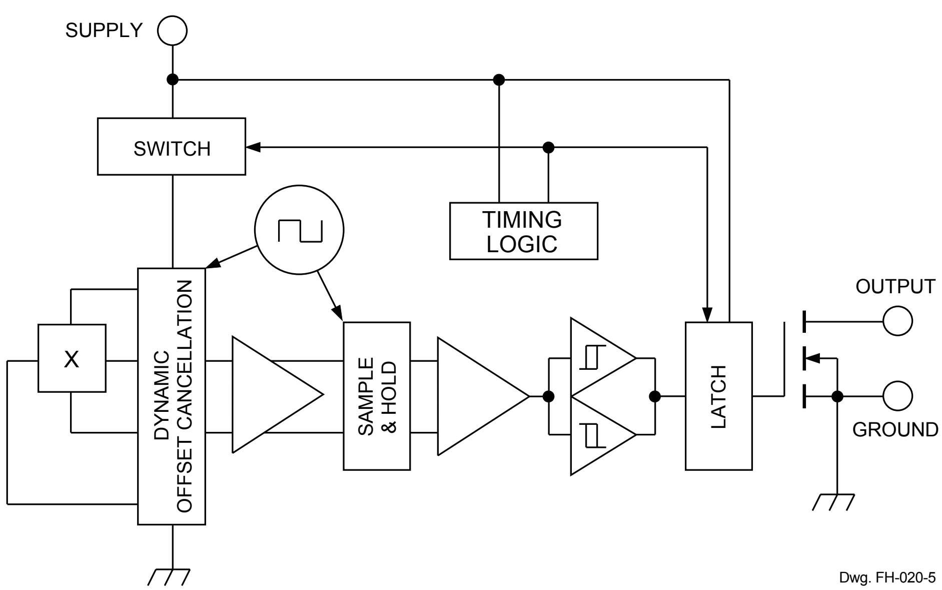


Functional Block Diagram

Description (continued)

requirements, component matching, very low input-offset errors, and small component geometries.

Four package styles provide magnetically optimized solutions for most applications. Miniature low-profile surface-mount package types *EH* and *EL* (0.75 and 0.50 mm nominal height) are leadless, *LH* is a 3-pin low-profile SMD, and *UA* is a three-pin SIP for through-hole mounting. Packages are lead (Pb) free (suffix, *–T*) with 100% matte tin plated leadframes.

SPECIFICATIONS

Selection Guide

Part Number	Packing[1]	Package	Ambient Temperature T_A (°C)	State in Magnetic Field
A3211EEHLT–T[2,4]	3000 pieces per reel	2 mm x 3 mm, 0.75 mm nominal height DFN	–40 to 85	Off
A3211EELLT–T[2,4]	3000 pieces per reel	2 mm x 2 mm, 0.50 mm nominal height DFN		
A3211ELHLT–T[4]	3000 pieces per reel	3-pin surface mount SOT23W		
A3211ELHLX–T[4]	10000 pieces per 13-in. reel	3-pin surface mount SOT23W		
~~A3212EEHLT–T~~[2,3]	3000 pieces per reel	2 mm x 3 mm, 0.75 mm nominal height DFN	–40 to 85	On
A3212EELLT–T[2]	3000 pieces per reel	2 mm x 2 mm, 0.50 mm nominal height DFN		
A3212ELHLT–T	3000 pieces per reel	3-pin surface mount SOT23W		
A3212ELHLX–T	10000 pieces per 13-in. reel	3-pin surface mount SOT23W		
A3212EUA–T	500 pieces per bulk bag	SIP-3 through hole		
A3212LLHLT–T	3000 pieces per reel	3-pin surface mount SOT23W	–40 to 150	
A3212LLHLX–T	10000 pieces per 13-in. reel	3-pin surface mount SOT23W		
A3212LUA–T	500 pieces per bulk bag	SIP-3 through hole		

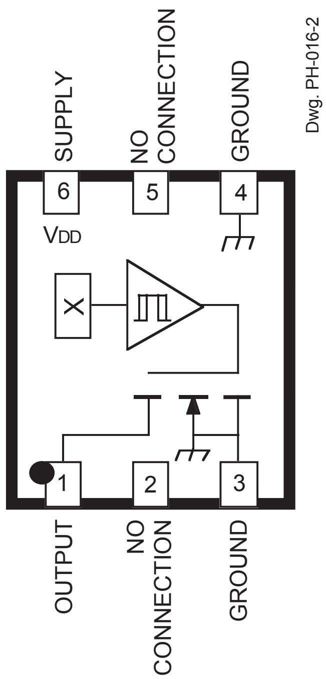
[1]Contact Allegro for additional packaging and handling options.
[2]Allegro products sold in DFN package types are not intended for automotive applications.
[3]Variant is in production but has been determined to be NOT FOR NEW DESIGN. This classification indicates that sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because obsolescence in the near future is probable. Samples are no longer available. Status change: December 3, 2013. Recommended substitute: A3212EELLT-T.
[4]For automotive sales, please contact the field applications engineer.

Absolute Maximum Ratings

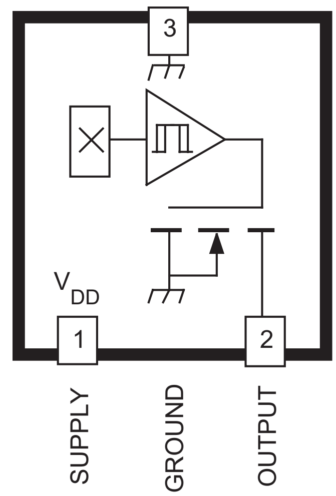
Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	V_{DD}		5	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	V_{OUT}		5	V
Output Current	I_{OUT}		1	mA
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
		Range L	–40 to 150	ºC
Maximum Junction Temperature	T_J(max)		165	ºC
Storage Temperature	T_{stg}		–65 to 170	ºC

Pinout Drawings

Package Suffix 'EH' Pinning
(Leadless Chip Carrier)



Package Suffix 'EL' Pinning
(Leadless Chip Carrier)



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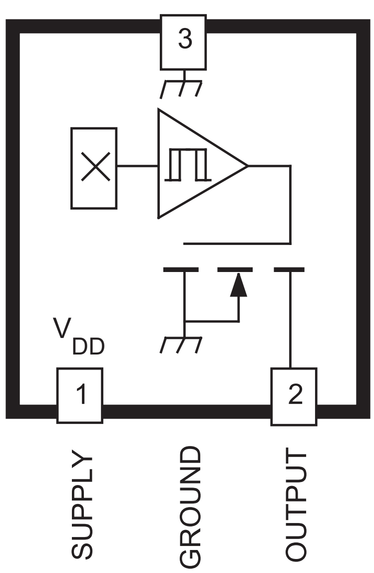
Package Suffix 'LH' Pinning
(SOT23W)



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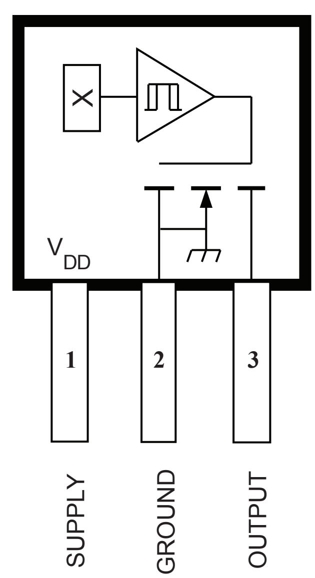
Package Suffix 'UA' Pinning
(SIP)



Dwg. PH-016

Pinning is shown viewed from branded side.

ELECTRICAL CHARACTERISTICS: over operating voltage and temperature range (unless otherwise specified).

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.*	Max.	Units
Supply Voltage Range	V_{DD}	Operating	2.5	2.75	3.5	V
Output Leakage Current	I_{OFF}	V_{OUT} = 3.5 V, Output off	–	<1.0	1.0	µA
Output On Voltage	V_{OUT}	I_{OUT} = 1 mA, V_{DD} = 2.75 V	–	100	300	mV
Awake Time	t_{awake}		–	45	90	µs
Period	t_{period}		–	45	90	ms
Duty Cycle	d.c.		–	0.1	–	%
Chopping Frequency	f_C		–	340	–	kHz
Supply Current	$I_{DD(EN)}$	Chip awake (enabled)	–	–	2.0	mA
	$I_{DD(DIS)}$	Chip asleep (disabled)	–	–	8.0	µA
	$I_{DD(AVG)}$	V_{DD} = 2.75 V	–	5.1	10	µA
		V_{DD} = 3.5 V	–	6.7	10	µA

* Typical data is at T_A = 25°C and V_{DD} = 2.75 V, and is for design information only.

A3211 MAGNETIC CHARACTERISTICS over operating voltage range (unless otherwise specified)

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Over Temperature Range E: T_A = –40°C to 85°C						
Operate Points	B_{OPS}	South pole to branded side; B > B_{OP}, V_{OUT} = High (Output Off)	–	37	55	G
	B_{OPN}	North pole to branded side; B > B_{OP}, V_{OUT} = High (Output Off)	–55	–40	–	G
Release Points	B_{RPS}	South pole to branded side; B < B_{RP}, V_{OUT} = Low (Output On)	10	31	–	G
	B_{RPN}	North pole to branded side; B < B_{RP}, V_{OUT} = Low (Output On)	–	–34	–10	G
Hysteresis	B_{HYS}	$\|B_{OPx} - B_{RPx}\|$	–	5.9	–	G

NOTES:
1. Negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.
2. B_{OPx} = operate point (output turns off); B_{RPx} = release point (output turns on).
3. Typical Data is at T_A = +25°C and V_{DD} = 2.75 V and is for design information only.
4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

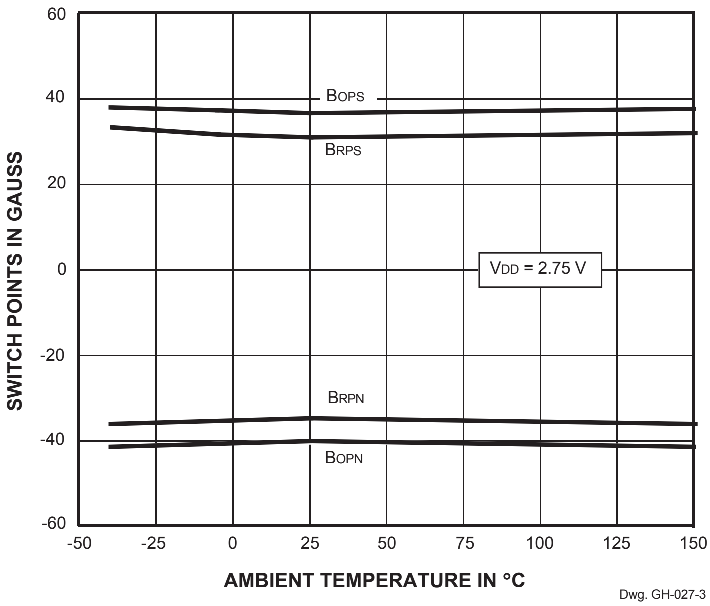
A3212 MAGNETIC CHARACTERISTICS over operating voltage range (unless otherwise specified)

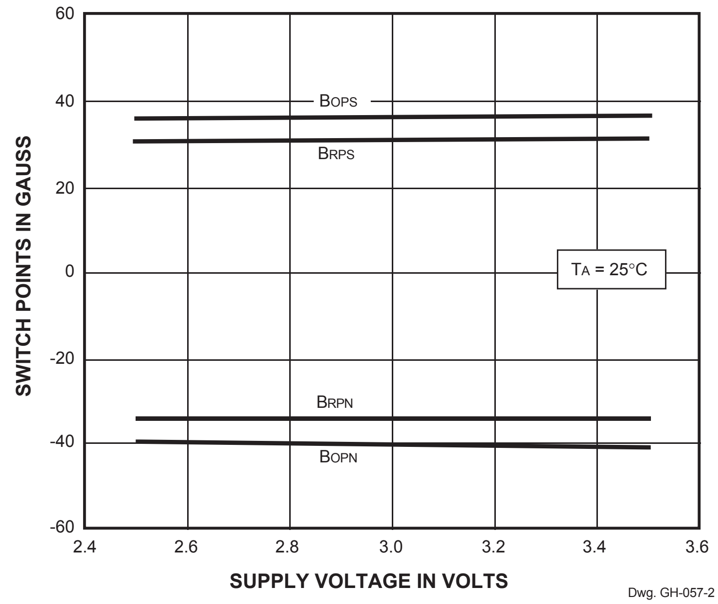
Characteristic	Symbol	Test Conditions	Limits			
			Min.	**Typ.**	**Max.**	**Units**
Over Temperature Range E: T_A = –40°C to 85°C						
Operate Points	B_{OPS}	South pole to branded side; B > B_{OP}, V_{OUT} = Low (Output On)	–	37	55	G
	B_{OPN}	North pole to branded side; B > B_{OP}, V_{OUT} = Low (Output On)	–55	–40	–	G
Release Points	B_{RPS}	South pole to branded side; B < B_{RP}, V_{OUT} = High (Output Off)	10	31	–	G
	B_{RPN}	North pole to branded side; B < B_{RP}, V_{OUT} = High (Output Off)	–	–34	–10	G
Hysteresis	B_{HYS}	$\|B_{OPx} - B_{RPx}\|$	–	5.9	–	G
Over Temperature Range L: T_A = –40°C to 150°C						
Operate Points	B_{OPS}	South pole to branded side; B > B_{OP}, V_{OUT} = Low (Output On)	–	37	65	G
	B_{OPN}	North pole to branded side; B > B_{OP}, V_{OUT} = Low (Output On)	–65	–40	–	G
Release Points	B_{RPS}	South pole to branded side; B < B_{RP}, V_{OUT} = High (Output Off)	10	31	–	G
	B_{RPN}	North pole to branded side; B < B_{RP}, V_{OUT} = High (Output Off)	–	–34	–10	G
Hysteresis	B_{HYS}	$\|B_{OPx} - B_{RPx}\|$	–	5.9	–	G

NOTES:
1. Negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.
2. B_{OPx} = operate point (output turns on); B_{RPx} = release point (output turns off).
3. Typical Data is at T_A = +25°C and V_{DD} = 2.75 V and is for design information only.
4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

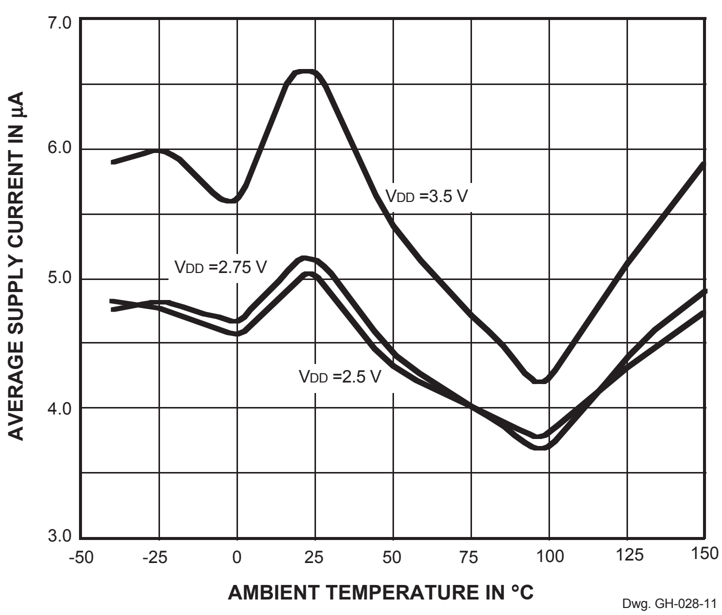
TYPICAL OPERATING CHARACTERISTICS

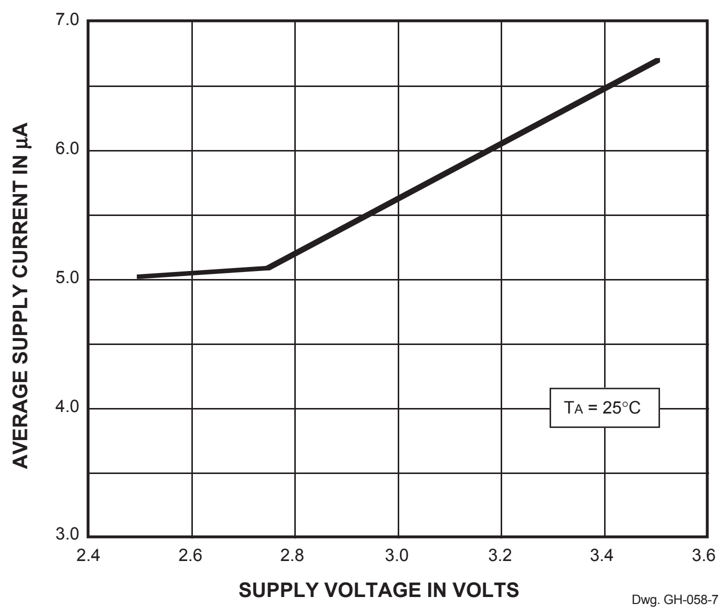
Switch Points





Supply Current





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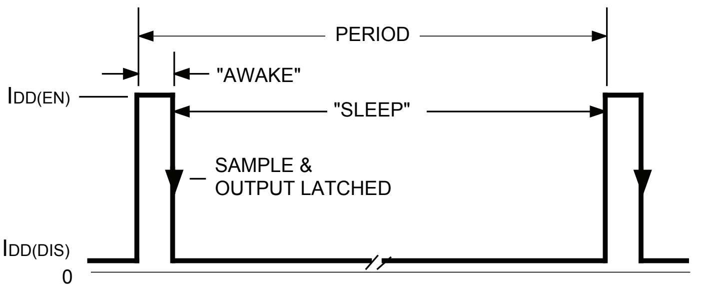
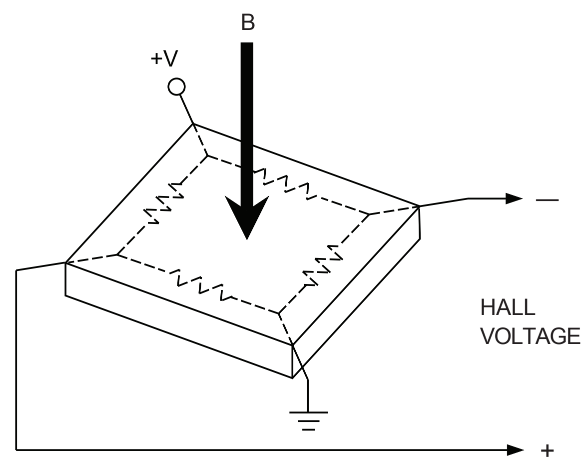
FUNCTIONAL DESCRIPTION

Low Average Power

Internal timing circuitry activates the IC for 45 µs and deactivates it for the remainder of the period (45 ms). A short "awake" time allows for stabilization prior to the sampling and data latching on the falling edge of the timing pulse. The output during the "sleep" time is latched in the last sampled state. The supply current is not affected by the output state.



Dwg. WH-017-2

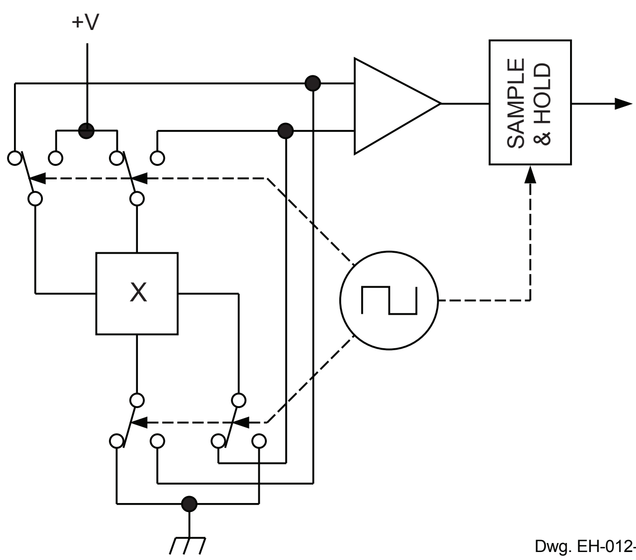


Dwg. AH-011-2

Chopper-Stabilized Technique

The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaing the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. A relatively high sampling frequency is used for faster signal processing capability can be processed.

More detailed descriptions of the circuit operation can be found in: Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.

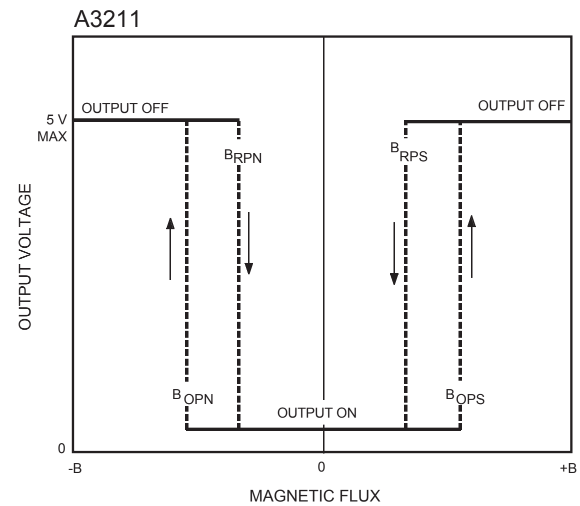


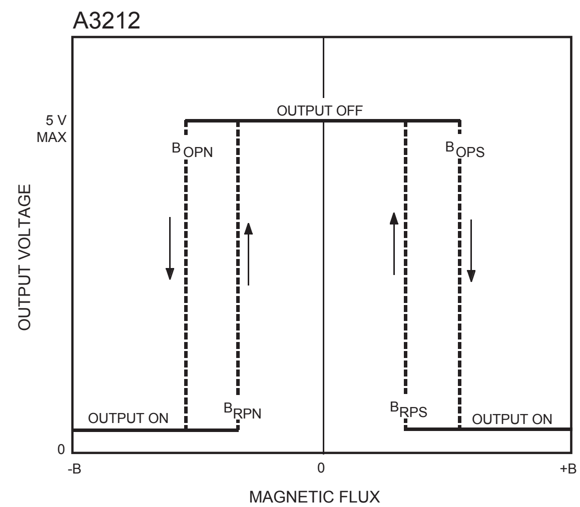
Dwg. EH-012-1

Operation

The output of the A3212 switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point B_{OPS} (or is less than B_{OPN}). After turn-on, the output is capable of sinking up to 1 mA and the output voltage is $V_{OUT(ON)}$. When the magnetic field is reduced below the release point B_{RPS} (or increased above B_{RPN}), the device output switches high (turns off). The difference in the magnetic operate and release points is the hysteresis (B_{hys}) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise. The A3211 functions in the same manner, except the output voltage is reversed from the A3212, as shown in the figures to the right.

As used here, negative flux densities are defined as less than zero (algebraic convention), i.e., -50 G is less than +10 G.





Applications

Allegro's pole-independent processing technique allows for operation with either a north pole or south pole magnet orientation, enhancing the manufacturability of the device. The state-of-the-art technology provides the same output polarity for either pole face.

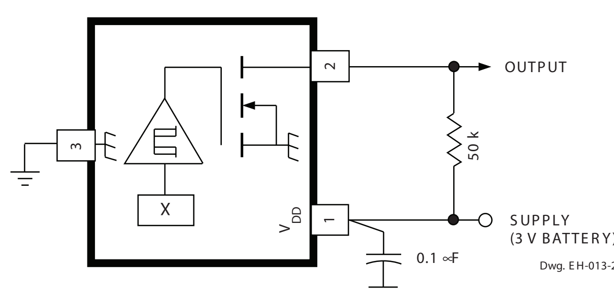
It is strongly recommended that an external bypass capacitor be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique. This is especially true due to the relatively high impedance of battery supplies.

The simplest form of magnet that will operate these devices is a bar magnet with either pole near the branded surface of the device. Many other methods of operation are possible. Extensive applications information for Hall-effect devices is available in:

• *Hall-Effect IC Applications Guide*, Application Note 27701;
• *Hall-Effect Devices: Soldering, Gluing, Potting, Encapsulating, and Lead Forming*, Application Note 27703.1;
• *Soldering Methods for Allegro's Products — SMD and Through-Hole*, Application Note 26009.

All are provided at

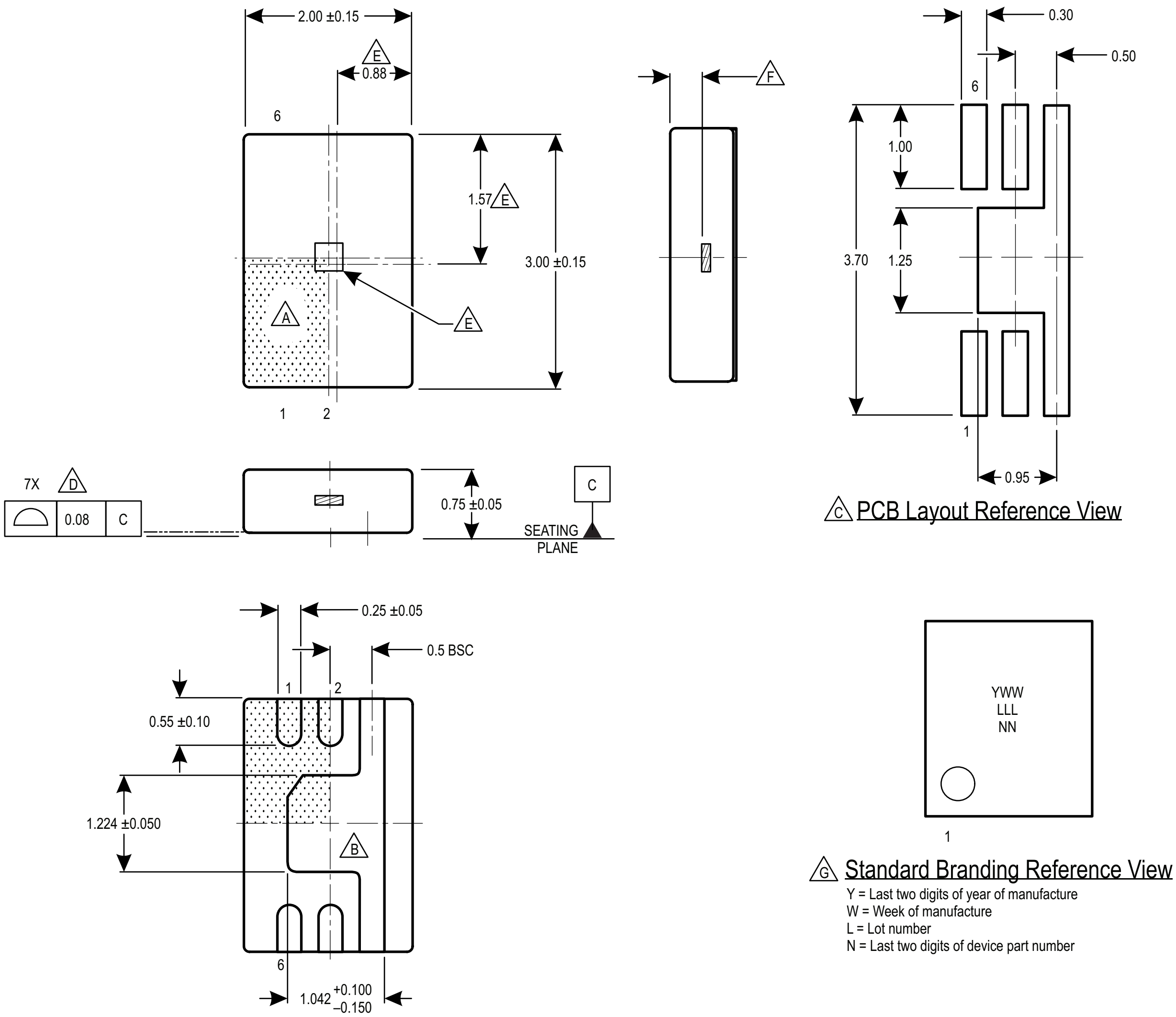
www.allegromicro.com



PACKAGE OUTLINE DRAWINGS

For Reference Only – Not for Tooling Use

(Reference DWG-2861 and JEDEC MO-229WCED, Type 1)
Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

E Hall Element (not to scale); U.S. customary dimensions controlling

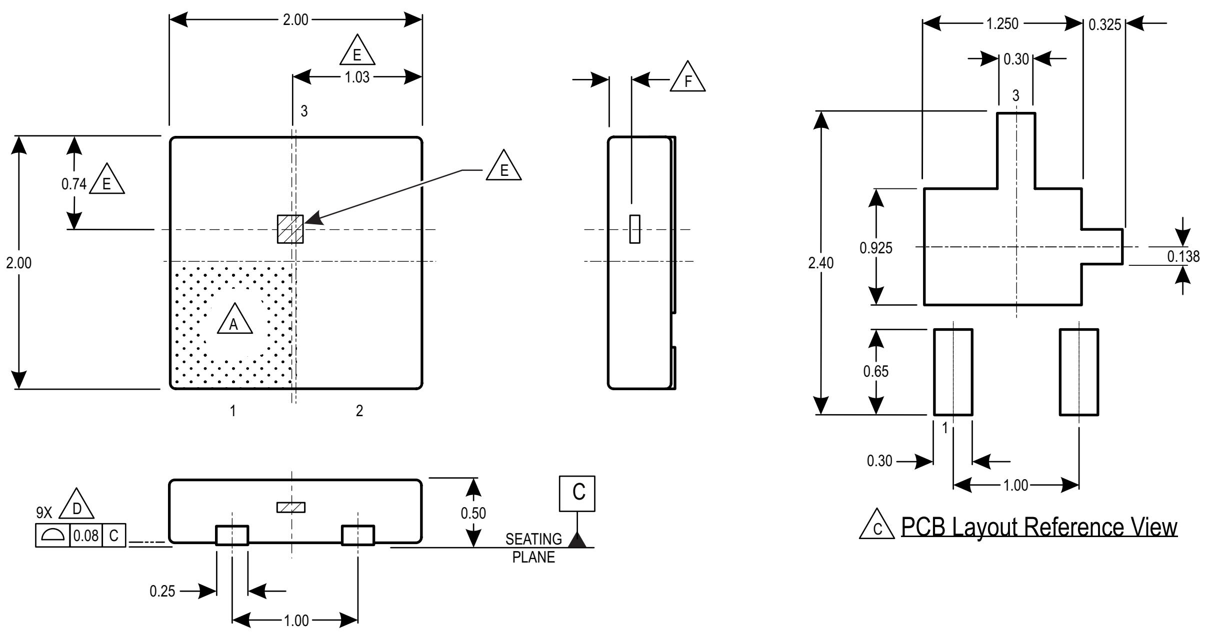
F Active Area Depth, 0.32 mm NOM

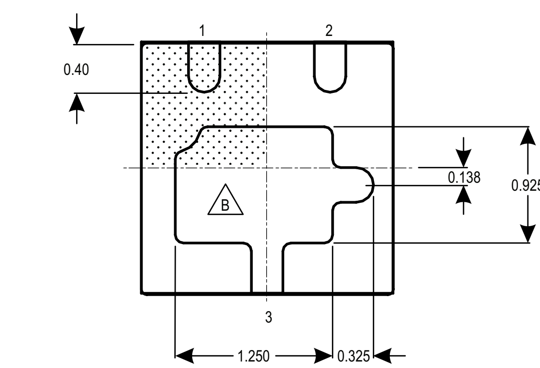
G Branding scale and appearance at supplier discretion

Package EH, 6-Pin DFN

For Reference Only – Not for Tooling Use

(Reference DWG-2861 and JEDEC MO-229UCCD)
All dimension nominal – Dimensions in millimeters – NOT TO SCALE
Exact case and lead configuration at supplier discretion within limits shown



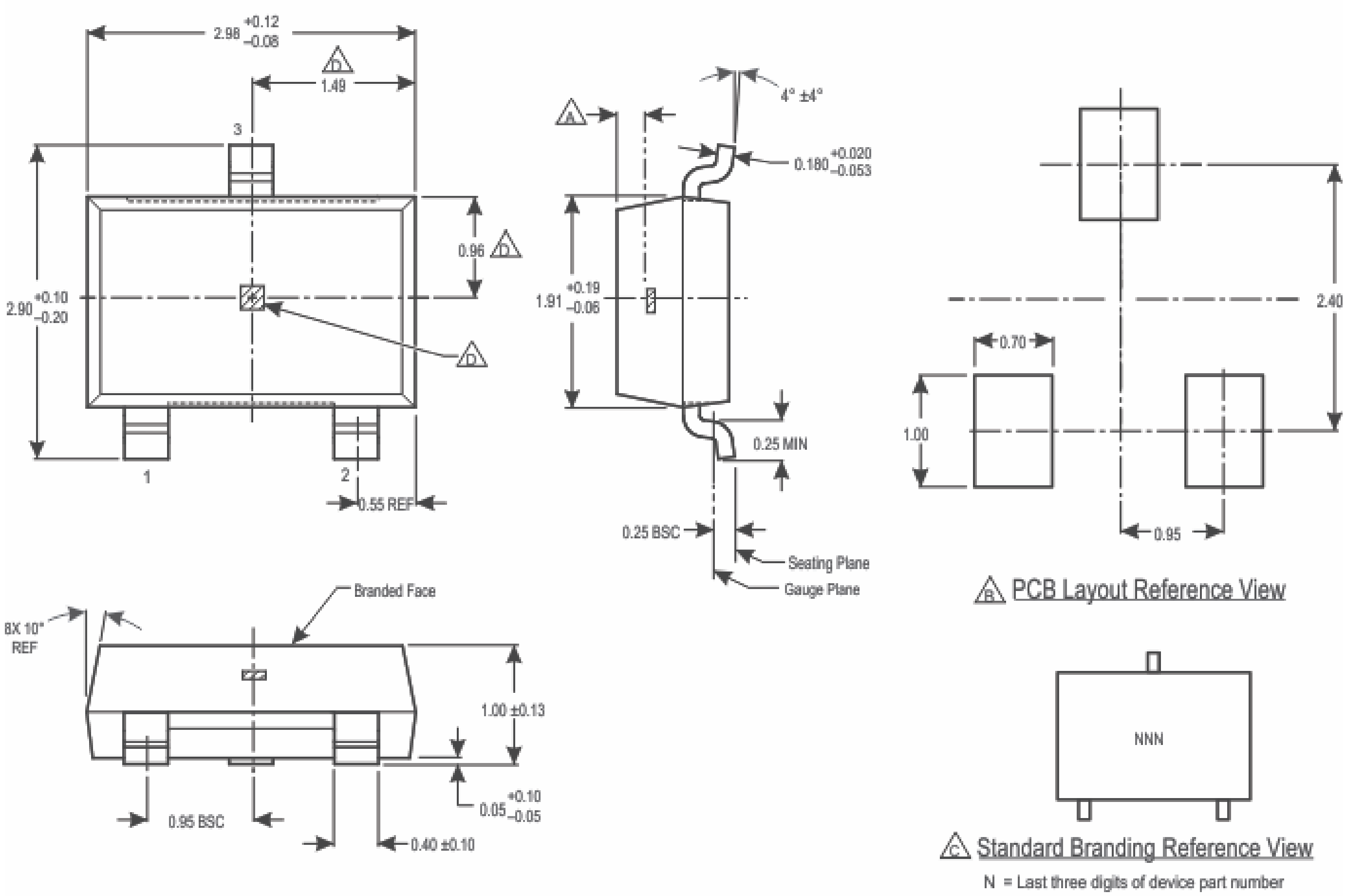


- A: Terminal #1 mark area
- B: Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)
- C: Reference land pattern layout (reference IPC7351); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)
- D: Coplanarity includes exposed thermal pad and terminals
- E: Hall element (not to scale); U.S. customary dimensions controlling
- F: Active area depth = 0.18

Package EL, 3-Pin DFN

For Reference Only – Not for Tooling Use

(Reference DWG-2840)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



A Active Area Depth, 0.43 mm

B Reference land pattern layout; all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances

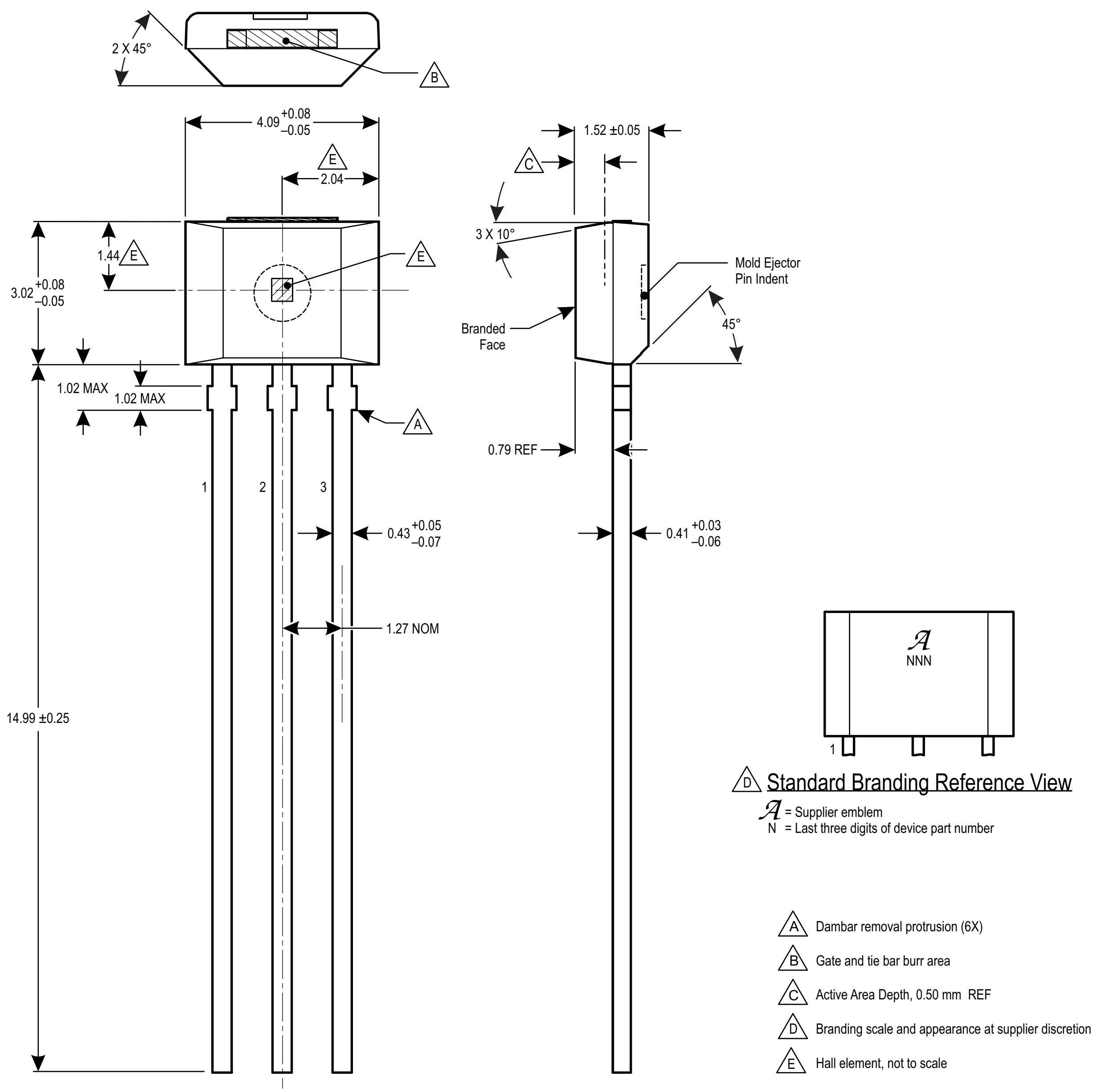
C Branding scale and appearance at supplier discretion

D Hall elements, not to scale

Package LH, 3-Pin SOT-23W

For Reference Only – Not for Tooling Use

(Reference DWG-9065)
Dimensions in millimeters – NOT TO SCALE
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown



Package UA, 3-Pin SIP

Revision History

Revision	Revision Date	Description of Revision
18	December 11, 2013	Update application note references
19	August 1, 2014	Revised footnote on Selection Guide
20	January 1, 2015	Added LX option to Selection Guide

For the latest version of this document, visit our website:

www.allegromicro.com

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