DRV8711 Stepper Motor Controller IC

1 Features

- Pulse width modulation (PWM) microstepping motor driver
  - Built-In 1/256-Step microstepping indexer
  - Drives external N-Channel MOSFETs
  - Optional STEP/DIR pins
  - Optional PWM control interface for DC motors
- Flexible decay modes, including automatic mixed decay mode
- Stall detection with optional BEMF output
- Highly configurable SPI serial interface
- Internal reference and torque DAC
- 8-V to 52-V Operating supply voltage range
- Scalable output current
- Thermally enhanced surface-mount package
- 5-V Regulator capable of 10-mA load
- Protection and diagnostic features
  - Overcurrent protection (OCP)
  - Overtemperature shutdown (OTS)
  - Undervoltage lockout (UVLO)
  - Individual fault condition indication bits
  - Fault condition indication pin

2 Applications

- Office Automation Machines
- Factory Automation
- Textile Machines
- Robotics

3 Description

The DRV8711 device is a stepper motor controller that uses external N-channel MOSFETs to drive a bipolar stepper motor or two brushed DC motors. A microstepping indexer is integrated, which is capable of step modes from full step to 1/256-step.

An ultra-smooth motion profile can be achieved using adaptive blanking time and various current decay modes, including an auto-mixed decay mode. Motor stall is reported with an optional back-EMF output.

A simple step/direction or PWM interface allows easy interfacing to controller circuits. A SPI serial interface is used to program the device operation. Output current (torque), step mode, decay mode, and stall detection functions are all programmable through a SPI serial interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature. Fault conditions are indicated through a FAULTn pin, and each fault condition is reported through a dedicated bit through SPI.

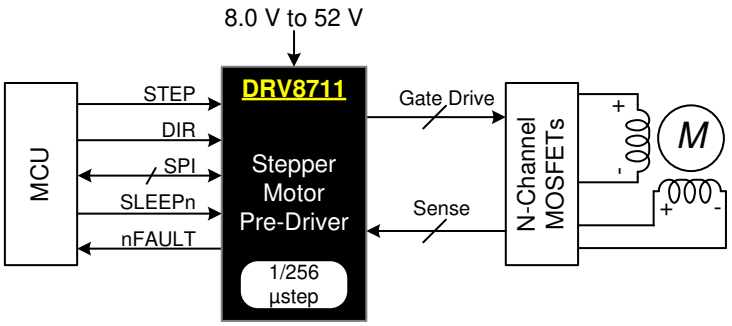
The DRV8711 is packaged in a PowerPAD™ 38-pin HTSSOP package with thermal pad (Eco-friendly: RoHS and no Sb/Br).

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DRV8711	HTSSOP (38)	9.70 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (May 2017) to Revision H — **Page**

- Added content to Overcurrent Protection (OCP) ... 25
- Added items to the Table 5 table ... 33
- Added Calculate Current Regulation section ... 35

Changes from Revision F (July 2016) to Revision G — **Page**

- Changed the description of the SCS pin in the *Pin Functions* table ... 4
- Changed the maximum voltages for the charge pump voltage, high-side gate drive pin voltage, and phase node pin voltage in the *Absolute Maximum Ratings* table ... 6
- Changed the OTS bit description in the STATUS register ... 30
- Clarified UVLO bit operation when device is sleep mode ... 31

Changes from Revision E (March 2015) to Revision F — **Page**

- Clarified that the SMPLTH bit 10 is a write-only bit in the TORQUE register ... 23
- Changed the default values for the OCPTH, OCPDEG, IDRIVEN, and IDRIVEP bits in the DRIVE register ... 30
- Added the *Receiving Notification of Documentation Updates* and *Community Resources* sections ... 43

Changes from Revision D (January 2014) to Revision E — **Page**

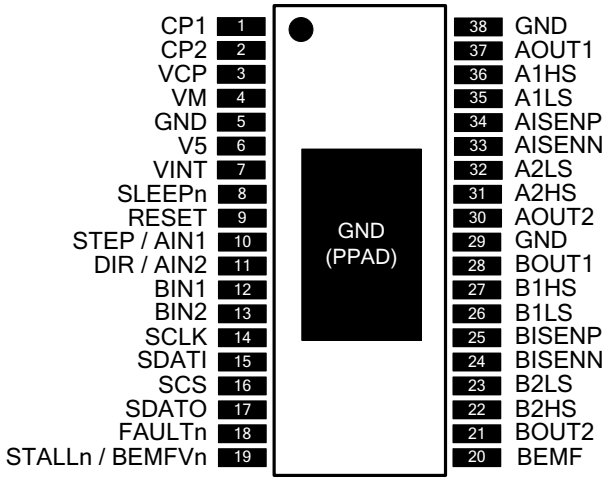
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision C (December 2013) to Revision D **Page**

- Changed STATUS Register bit descriptions 3 through 5 30

5 Pin Configuration and Functions

DCP PowerPAD™ Package
38-Pin HTSSOP
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
POWER AND GROUND				
GND	5, 29, 38, PPAD	—	Device ground	All pins must be connected to ground
VM	4	—	Bridge A power supply	Connect to motor supply voltage. Bypass to GND with a 0.01-μF ceramic capacitor plus a 100-μF electrolytic capacitor.
VINT	7	—	Internal logic supply voltage	Logic supply voltage. Bypass to GND with a 1-μF 6.3-V X7R ceramic capacitor.
V5	6	O	5-V regulator output	5-V linear regulator output. Bypass to GND with a 0.1-μF 10-V X7R ceramic capacitor.
CP1	1	IO	Charge pump flying capacitor	Connect a 0.1-μF X7R capacitor between CP1 and CP2. Voltage rating must be greater than applied VM voltage.
CP2	2	IO	Charge pump flying capacitor	
VCP	3	IO	High-side gate drive voltage	Connect a 1-μF 16-V X7R ceramic capacitor to VM
CONTROL				
SLEEPn	8	I	Sleep mode input	Logic high to enable device, logic low to enter low-power sleep mode
STEP/AIN1	10	I	Step input/Bridge A IN1	Indexer mode: Rising edge causes the indexer to move one step. External PWM mode: controls bridge A OUT1 Internal pulldown.
DIR/AIN2	11	I	Direction input/Bridge A IN2	Indexer mode: Level sets the direction of stepping. External PWM mode: controls bridge A OUT2 Internal pulldown.
BIN1	12	I	Bridge B IN1	Indexer mode: No function External PWM mode: controls bridge B OUT1 Internal pulldown.
BIN2	13	I	Bridge B IN2	Indexer mode: No function External PWM mode: controls bridge B OUT2 Internal pulldown.
RESET	9	I	Reset input	Active-high reset input initializes all internal logic and disables the H-bridge outputs. Internal pulldown.
SERIAL INTERFACE				
SCS	16	I	Serial chip select input	Active high to enable serial data transfer. Active low to complete the transaction. Internal pulldown.
SCLK	14	I	Serial clock input	Rising edge clocks data into part for write operations. Falling edge clocks data out of part for read operations. Internal pulldown.

(1) Directions: I = input, O = output, OZ = 3-state output, OD = open-drain output, IO = input/output

Pin Functions (continued)

PIN		I/O(1)	DESCRIPTION	EXTERNAL COMPONENTS OR CONNECTIONS
NAME	NO.			
SDATI	15	I	Serial data input	Serial data input from controller. Internal pulldown.
SDATO	17	OD	Serial data output	Serial data output to controller. Open-drain output requires external pullup.
STATUS				
STALLn/ BEMFVn	19	OD	Stall/Back EMF valid	Internal stall detect mode: logic low when motor stall detected. External stall detect mode: Active low when valid back EMF measurement is ready. Open-drain output requires external pullup.
FAULTn	18	OD	Fault	Logic low when in fault condition. Open-drain output requires external pullup. Faults: OCP, PDF, OTS, UVLO
BEMF	20	O	Back EMF	Analog output voltage represents motor back EMF. Place a 1-nF low-leakage capacitor to ground on this pin.
OUTPUTS				
A1HS	36	O	Bridge A out 1 HS gate	Connect to gate of HS FET for bridge A out 1
AOUT1	37	I	Bridge A output 1	Connect to output node of external FETs of bridge A out 1
A1LS	35	O	Bridge A out 1 LS gate	Connect to gate of LS FET for bridge A out 1
A2HS	31	O	Bridge A out 2 HS gate	Connect to gate of HS FET for bridge A out 2
AOUT2	30	I	Bridge A output 2	Connect to output node of external FETs of bridge A out 2
A2LS	32	O	Bridge A out 2 LS gate	Connect to gate of LS FET for bridge A out 2
AISENP	34	I	Bridge A Isense + in	Connect to current sense resistor for bridge A
AISENN	33	I	Bridge A Isense – in	Connect to ground at current sense resistor for bridge A
B1HS	27	O	Bridge B out 1 HS gate	Connect to gate of HS FET for bridge B out 1
BOUT1	28	I	Bridge B output 1	Connect to output node of external FETs of bridge B out 1
B1LS	26	O	Bridge B out 1 LS gate	Connect to gate of LS FET for bridge B out 1
B2HS	22	O	Bridge B out 2 HS gate	Connect to gate of HS FET for bridge B out 2
BOUT2	21	I	Bridge B output 2	Connect to output node of external FETs of bridge B out 2
B2LS	23	O	Bridge B out 2 LS gate	Connect to gate of LS FET for bridge B out 2
BISENP	25	I	Bridge B Isense + in	Connect to current sense resistor for bridge B
BISENN	24	I	Bridge B Isense – in	Connect to ground at current sense resistor for bridge B

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1][2][3]

	MIN	MAX	UNIT
Power supply voltage	–0.6	60	V
Charge pump voltage (CP2, VCP)	–0.6	VM + 12	V
Charge pump voltage (CP1)	–0.6	VM + 0.6	V
5-V regulator voltage (V5)	–0.6	5.5	V
Internal regulator voltage (VINT)	–0.6	2	V
Digital pin voltage (SLEEPn, RESET, STEP/AIN1, DIR/AIN2, BIN1, BIN2, SCS, SCLK, SDATI, SDATO, FAULTn, STALLn/BEMFVn)	–0.6	5.5	V
High-side gate drive pin voltage (A1HS, A2HS, B1HS, B2HS)	–0.6	VM + 12	V
Low-side gate drive pin voltage (A1LS, A2LS, B1LS, B2LS)	–0.6	12	V
Phase node pin voltage (AOUT1, AOUT2, BOUT1, BOUT2)	–0.6	VM + 0.6	V
ISENSEx pin voltage (AISENP, AISENN, BISENP, BISENN)	–0.7	0.7	V
BEMF pin voltage (BEMF)	–0.6	5.5	V
Operating virtual junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–60	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.
(3) Power dissipation and thermal limits must be observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±4000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101[2]	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_M	Motor power supply voltage	8		52	V
I_{VS}	V5 external load current	0		10	mA
T_A	Operating ambient temperature	-40		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		DRV8711 DCP (HTSSOP) 38 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	17.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.9	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VM}	VM operating supply current	VM = 24 V		17	20	mA
I_{VMQ}	VM sleep mode supply current	VM = 24 V, SLEEPn = 0, T_A = 25°C		65	98	µA
V_{UVLO}	VM undervoltage lockout voltage	VM rising		7.1	8	V
		VM falling		6.3		
INTERNAL LINEAR REGULATORS						
V_5	V5 output voltage	VM ≥ 12 V, I_{OUT} = 1 mA – 10 mA	4.8	5	5.2	V
V_{INT}	VINT voltage	No external load – reference only	1.7	1.8	1.9	V
LOGIC-LEVEL INPUTS						
V_{IL}	Input low voltage				0.8	V
V_{IH}	Input high voltage		1.5			V
V_{HYS}	Input hysteresis voltage			300		mV
I_{IL}	Input low current	V_{IN} = 0 V	–5		5	µA
I_{IH}	Input high current	V_{IN} = 5 V	30	50	70	µA
SDATAO, STALLn, FAULTn OUTPUTS (OPEN-DRAIN OUTPUTS)						
V_{OL}	Output low voltage	I_O = 5 mA			0.5	V
I_{OH}	Output high leakage current	V_O = 3.3 V			1	µA
MOSFET DRIVERS						
V_{OUTH}	High-side gate drive output voltage	VM = 24 V, I_O = 100 µA		VM+10		V
V_{OUTL}	Low-side gate drive output voltage	VM = 24 V, I_O = 100 µA		10		V
t_{DEAD}	Output dead time digital delay (dead time is enforced in analog circuits)	DTIME = 00		400		ns
		DTIME = 01		450		
		DTIME = 10		650		
		DTIME = 11		850		
I_{OUTH}	Peak output current gate drive (source)	IDRIVEP = 00		50		mA
		IDRIVEP = 01		100		
		IDRIVEP = 10		150		
		IDRIVEP = 11		200		
I_{OUTI}	Peak output current gate drive (sink)	IDRIVEN = 00		100		mA
		IDRIVEN = 01		150		
		IDRIVEN = 10		200		
		IDRIVEN = 11		400		
t_{DRIVE}	Peak current drive time (source)	TDRIVEP = 00		250		ns
		TDRIVEP = 01		500		
		TDRIVEP = 10		1000		
		TDRIVEP = 11		2000		
t_{DRIVE}	Peak current drive time (sink)	TDRIVEN = 00		250		ns
		TDRIVEN = 01		500		
		TDRIVEN = 10		1000		
		TDRIVEN = 11		2000		
MOTOR DRIVER						
t_{OFF}	PWM off time adjustment range	Set by TOFF register	0.5		128	µs
t_{BLANK}	Current sense blanking time	Set by TBLANK register	0.5		5.12	µs

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PROTECTION CIRCUITS						
V_{OCP}	Overcurrent protection trip level (Voltage drop across external FET)	OCPTH = 00	160	250	320	mV
		OCPTH = 01	380	500	580	
		OCPTH = 10	620	750	850	
		OCPTH = 11	840	1000	1200	
t_{TSD}	Thermal shutdown temperature(1)	Die temperature	150	160	180	°C
t_{HYS}	Thermal shutdown hysteresis			20		°C
CURRENT SENSE AMPLIFIERS						
A_V	Gain	ISGAIN = 00		5		V/V
		ISGAIN = 01		10		
		ISGAIN = 10		20		
		ISGAIN = 11		40		
t_{SET}	Settling time (to ±1%)	ISGAIN = 00, ΔVIN = 400 mV		150		ns
		ISGAIN = 01, ΔVIN = 200 mV		300		
		ISGAIN = 10, ΔVIN = 100 mV		600		
		ISGAIN = 11, ΔVIN = 50 mV		1.2		µs
V_{OFS}	Offset voltage	ISGAIN = 00, input shorted			4	mV
V_{IN}	Input differential voltage range		–600		600	mV
CURRENT CONTROL DACs						
	Resolution			256		steps
	Full-scale step response	10% to 90%			5	µs
V_{REF}	Full-scale (reference) voltage		2.50	2.75	3	V

(1) Not tested in production; ensured by design.

6.6 SPI Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 1)

NO.			MIN	NOM	MAX	UNIT
1	t_{CYC}	Clock cycle time	250			ns
2	t_{CLKH}	Clock high time	25			ns
3	t_{CLKL}	Clock low time	25			ns
4	$t_{SU(SDATI)}$	Setup time, SDATI to SCLK	5			ns
5	$t_{H(SDATI)}$	Hold time, SDATI to SCLK	1			ns
6	$t_{SU(SCS)}$	Setup time, SCS to SCLK	5			ns
7	$t_{H(SCS)}$	Hold time, SCS to SCLK	1			ns
8	$t_{L(SCS)}$	Inactive time, SCS (between writes and reads)	100			ns
9	$t_{D(SDATO)}$	Delay time, SCLK to SDATO (during read)			10	ns
	t_{SLEEP}	Wake time (SLEEPn inactive to high-side gate drive enabled)			1	ms
	t_{RESET}	Delay from power up or RESETn high until serial interface functional			10	µs

6.7 Indexer Timing Requirements

over operating free-air temperature range (unless otherwise noted) (see Figure 2)

NO.			MIN	NOM	MAX	UNIT
1	f_{STEP}	Step frequency			250	kHz
2	$t_{WH(STEP)}$	Pulse duration, STEP high	1.9			µs
3	$t_{WL(STEP)}$	Pulse duration, STEP low	1.9			µs
4	$t_{SU(STEP)}$	Setup time, command to STEP rising	200			ns
5	$t_{H(STEP)}$	Hold time, command to STEP rising	200			ns

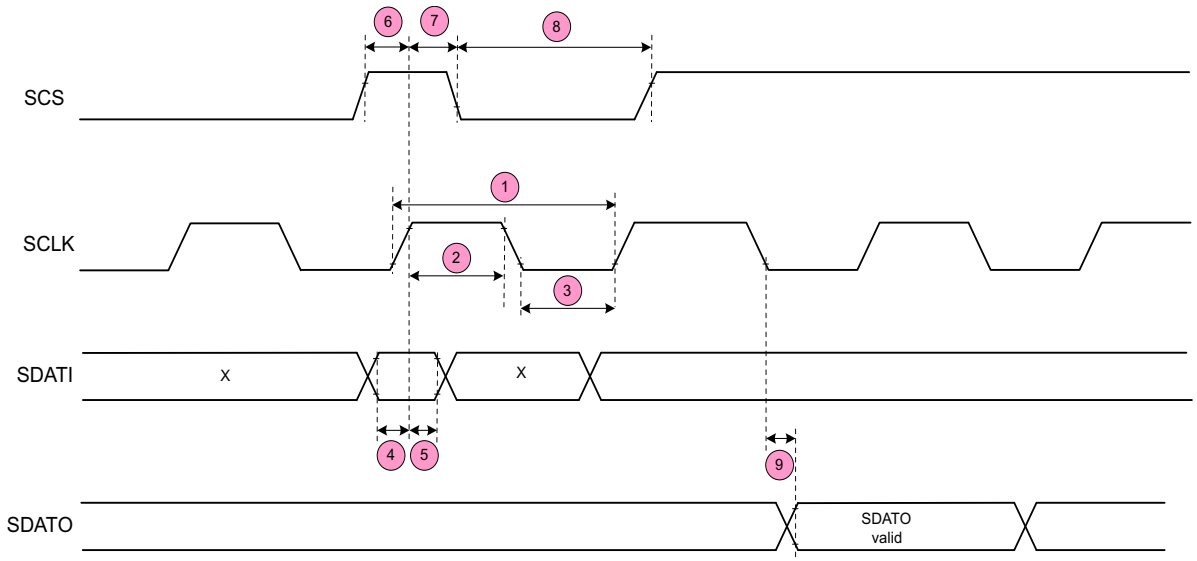


Figure 1. SPI Timing

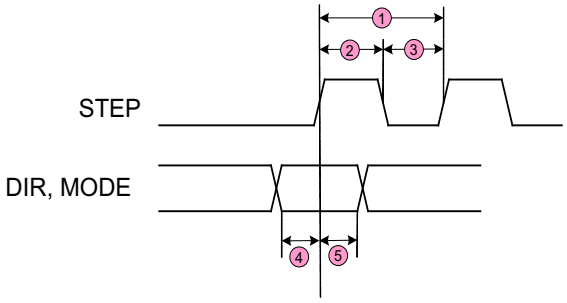


Figure 2. Indexer Timing

6.8 Typical Characteristics

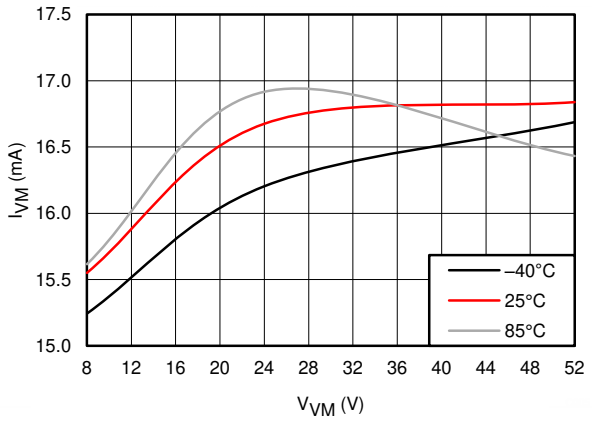


Figure 3. Operating Current

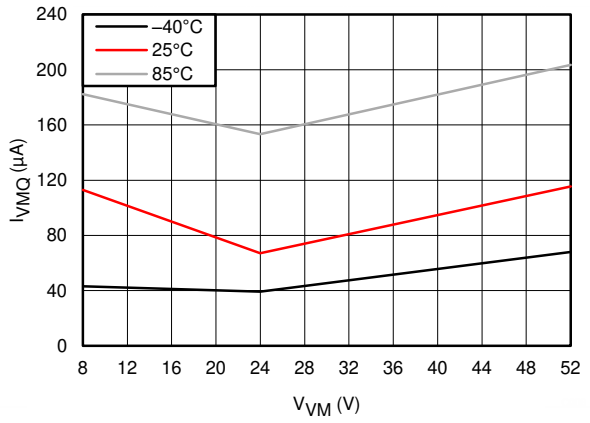


Figure 4. Sleep Current

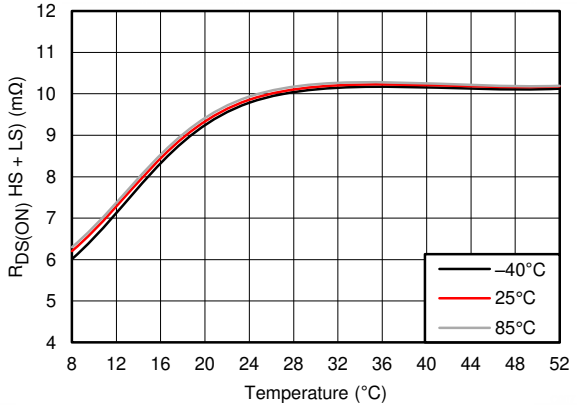


Figure 5. VCP Minus VM

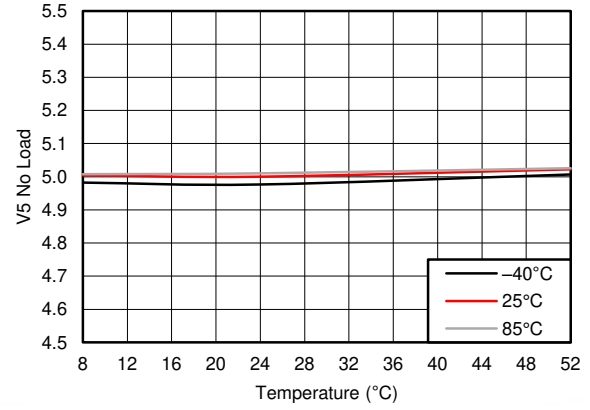


Figure 6. V5 No Load

7 Detailed Description

7.1 Overview

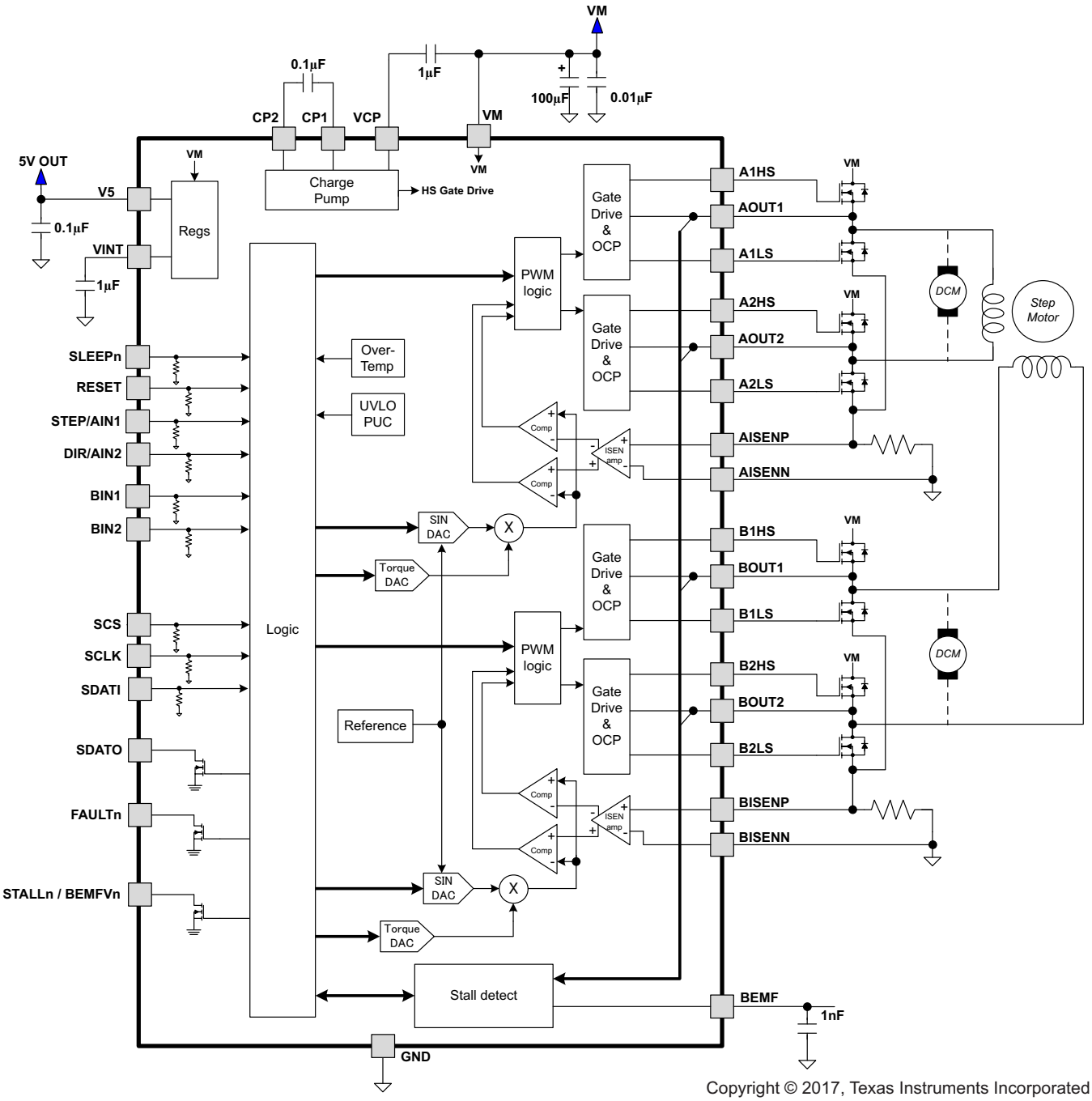
The DRV8711 device is a stepper motor controller that uses external N-channel MOSFETs to drive a bipolar stepper motor or two brushed DC motors. A microstepping indexer is integrated, which is capable of step modes from full step to 1/256-step.

An ultra-smooth motion profile can be achieved using adaptive blanking time, adjustable decay times, and various current decay modes, including an auto-mixed decay mode. When microstepping, motor stall can be reported with an optional back-EMF output.

A simple step/direction or PWM interface allows easy interfacing to controller circuits. A SPI serial interface is used to program the device operation. Output current (torque), step mode, decay mode, and stall detection functions are all programmable through a SPI serial interface.

Internal shutdown functions are provided for overcurrent protection, short-circuit protection, undervoltage lockout, and overtemperature. Fault conditions are indicated through a FAULTn pin, and each fault condition is reported through a dedicated bit through SPI.

7.2 Functional Block Diagram



7.3 Feature Description

Table 1 lists the critical components for the device.

Table 1. Critical Components

PIN	NAME	COMPONENT
4	VM	100-µF electrolytic rated for VM voltage to GND 0.01-µF ceramic rated for VM voltage to GND
3	VCP	1-µF ceramic X7R rated 16 V to VCP
1, 2	CP1, CP2	0.1-µF rated for VM + 12 V between these pins
6	V5	0.1-µF ceramic X7R rated 6.3 V to GND
7	VINT	1-µF ceramic X7R rated 6.3 V to GND
17	SDATO	Requires external pullup to logic supply
18	FAULTn	Requires external pullup to logic supply
19	STALLn/BEMFVn	Requires external pullup to logic supply
20	BEMF	1-nF low-leakage capacitor to GND

7.3.1 PWM Motor Drivers

The DRV8711 contains two H-bridge motor predrivers with current control PWM circuitry. More detailed descriptions of the subblocks are described in the following sections.

7.3.2 Direct PWM Input Mode

Direct PWM mode is selected by setting the PWMMODE bit in the OFF register. In direct PWM input mode, the AIN1, AIN2, BIN1, and BIN2 directly control the state of the output drivers. This allows for driving up to two brushed DC motors. The logic is shown in Table 2:

Table 2. Direct PWM Input Mode Logic

xIN1	xIN2	xOUT1	xOUT2	OPERATION
0	0	Z	Z	Asynchronous Fast Decay
0	1	L	H	Reverse Drive
1	0	H	L	Forward Drive
1	1	L	L	Slow Decay

If mixed or auto-mixed decay modes are used, they will apply to every cycle, because current change information is not available.

In direct PWM mode, the current control circuitry is still active. The full-scale VREF is set to 2.75 V. The TORQUE register may be used to scale this value, and the ISEN sense amp gain may still be set using the ISGAIN bits of the CTRL register.

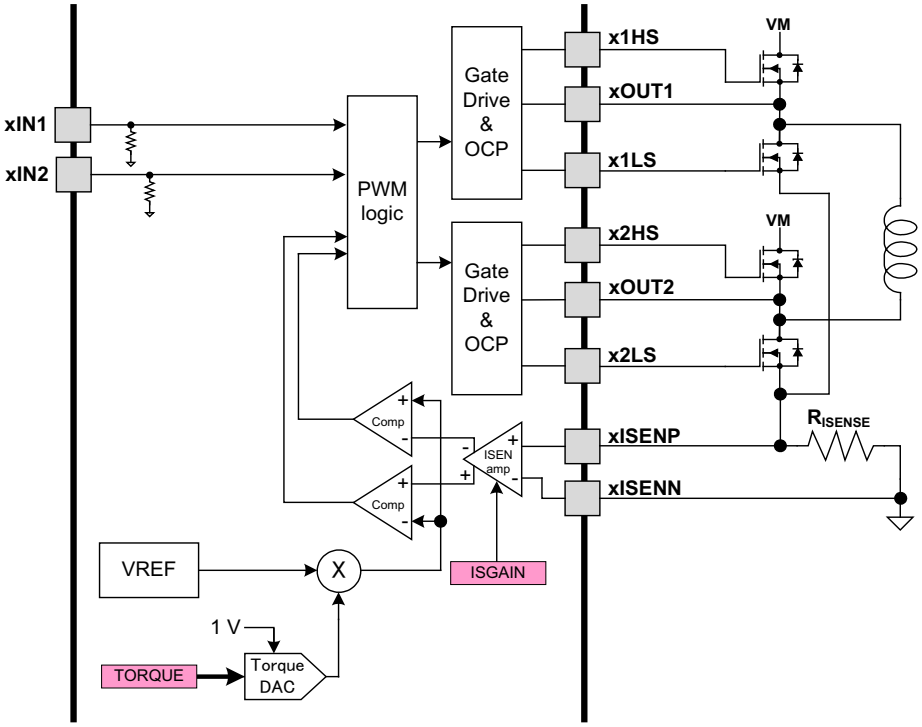


Figure 7. Direct PWM Input Mode

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding and the magnitude of the back EMF present. Once the current hits the current chopping threshold, the bridge disables the current for a fixed period of time, which is programmable between 500 ns and 128 µs by writing to the TOFF bits in the OFF register. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

The chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISENx pins, multiplied by the gain of the current sense amplifier, with a reference voltage. The current sense amplifier is programmable in the CTRL register. When driving in PWM mode, the chopping current is calculated as follows:

$$I_{CHOP} = \frac{2.75V \bullet TORQUE}{256 \bullet ISGAIN \bullet R_{ISENSE}} \quad (1)$$

Where TORQUE is the setting of the TORQUE bits, and ISGAIN is the programmed gain of the ISENSE amplifiers (5, 10, 20, or 40).

7.3.3 Microstepping Indexer

Built-in indexer logic in the DRV8711 allows a number of different stepping configurations. The MODE bits in the CTRL register are used to configure the stepping format as shown in Table 3.

Table 3. Microstepping Indexer Logic

MODE3	MODE2	MODE1	MODE0	STEP MODE
0	0	0	0	Full-step (2-phase excitation) with 71% current
0	0	0	1	1/2 step
0	0	1	0	1/4 step
0	0	1	1	1/8 step
0	1	0	0	1/16 step
0	1	0	1	1/32 step
0	1	1	0	1/64 step
0	1	1	1	1/128 step
1	0	0	0	1/256 step

Table 4 shows the relative current and step directions for full-step through 1/8-step operation. Higher microstepping resolutions follow the same pattern. The AOUT current is the sine of the electrical angle; BOUT current is the cosine of the electrical angle.

The reset state is 45°. This state is entered at power up or application of RESETn. This is shown in Table 4 by cells shaded in yellow.

Table 4. Step Directions

FULL STEP	1/2 STEP	1/4 STEP	1/8 STEP	AOUT CURRENT (% FULL-SCALE)	BOUT CURRENT (% FULL-SCALE)	ELECTRICAL ANGLE (DEGREES)
	1	1	1	0	100	0
			2	20	98	11.325
		2	3	38	92	22.5
			4	56	83	33.75
1	2	3	5	71	71	45 (home state)
			6	83	56	56.25
		4	7	92	38	67.5
			8	98	20	78.75
	3	5	9	100	0	90
			10	98	–20	101.25
		6	11	92	–38	112.5
			12	83	–56	123.75
2	4	7	13	71	–71	135
			14	56	–83	146.25
		8	15	38	–92	157.5
			16	20	–98	168.75
	5	9	17	0	–100	180
			18	–20	–98	191.25
		10	19	–38	–92	202.5
			20	–56	–83	213.75
3	6	11	21	–71	–71	225
			22	–83	–56	236.25
		12	23	–92	–38	247.5
			24	–98	–20	258.75
	7	13	25	–100	0	270
			26	–98	20	281.25
		14	27	–92	38	292.5
			28	–83	56	303.75
4	8	15	29	–71	71	315
			30	–56	83	326.25
		16	31	–38	92	337.5
			32	–20	98	348.75

At each rising edge of the STEP input, or each time a 1 is written to the RSTEP bit in the CTRL register, the indexer travels to the next state in the table. The direction is shown with the DIR pin high and the RDIR bit in the CTRL register set to 0, or the DIR pin low and the RDIR bit set to 1. If the DIR pin is low with the RDIR bit 0, or the DIR pin is high with the RDIR bit 1, the sequence is reversed. Positive current is defined as xOUT1 = positive with respect to xOUT2.

If the step mode is changed while stepping, the indexer will advance to the next valid state for the new MODE setting at the rising edge of STEP.

7.3.4 Current Regulation

The current through the motor windings is regulated by an adjustable fixed-off-time PWM current regulation circuit. When an H-bridge is enabled, current rises through the winding at a rate dependent on the DC voltage and inductance of the winding and the magnitude of the back EMF present. Once the current hits the current chopping threshold, the bridge disables the current for a fixed period of time, which is programmable between 500 nS and 128 µS by writing to the TOFF bits in the OFF register. After the off time expires, the bridge is re-enabled, starting another PWM cycle.

In stepping motors, current regulation is used to vary the current in the two windings in a sinusoidal fashion to provide smooth motion.

The PWM chopping current is set by a comparator which compares the voltage across a current sense resistor connected to the xISENx pins, multiplied by the gain of the current sense amplifier, with a reference voltage. The current sense amplifier is programmable in the CTRL register.

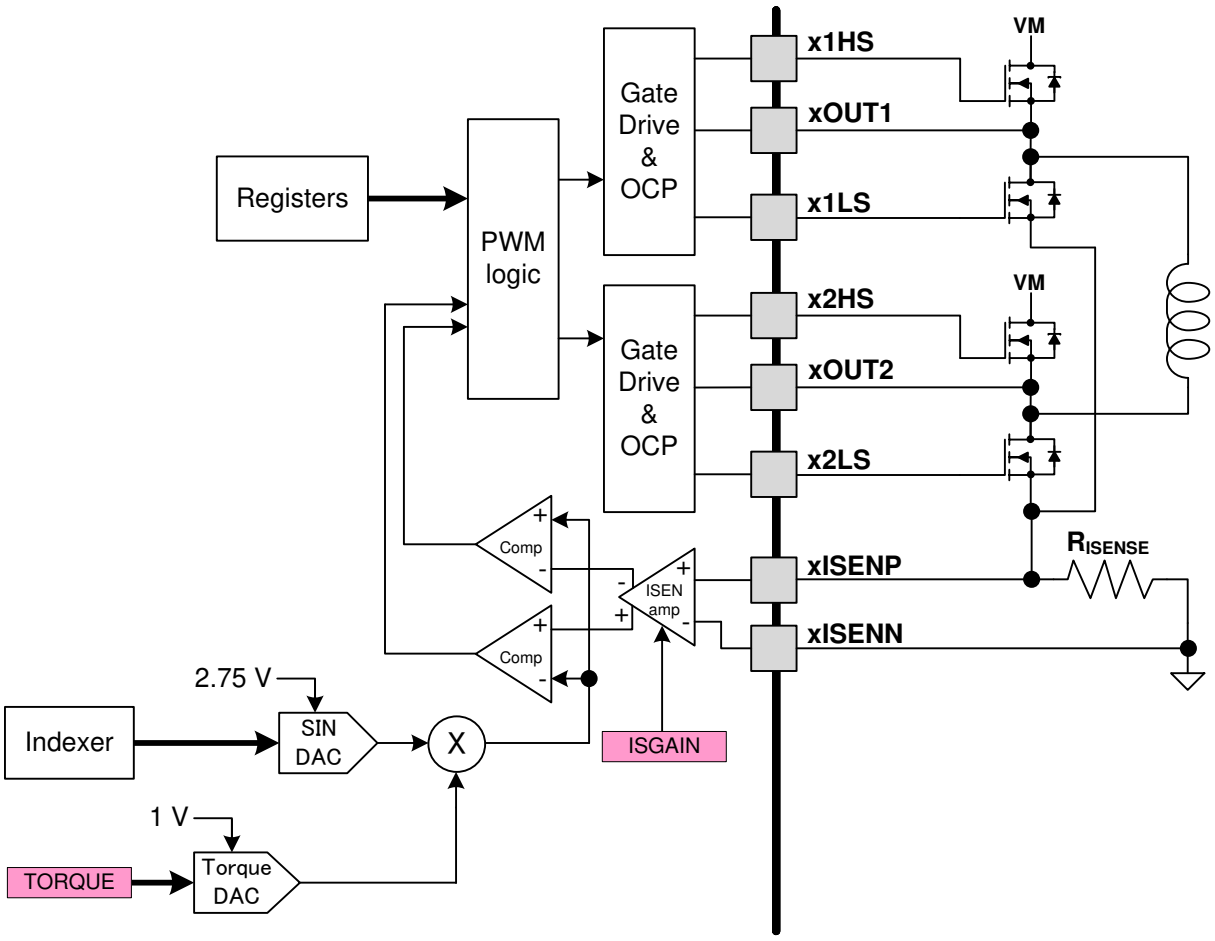


Figure 8. PWM Chopping Current

To generate the reference voltage for the current chopping comparator, the output of a sine lookup table is multiplied by the value of the bits in the TORQUE register. This result is applied to a sine-weighted DAC, whose full-scale output voltage is 2.75 V.

Therefore, the full-scale (100%) chopping current is calculated as follows:

$$I_{FS} = \frac{2.75V \bullet TORQUE}{256 \bullet ISGAIN \bullet R_{ISENSE}} \quad (2)$$

where

- TORQUE is the setting of the TORQUE bits
- ISGAIN is the programmed gain of the ISENSE amplifiers (5, 10, 20, or 40)

Example:

If a 0.1-Ω sense resistor is used, ISGAIN is set to 0 (gain of 5), and TORQUE is set to 255, the full-scale (100%) chopping current will be (2.75 V * 255) / (256 * 5 * 0.1 Ω) = 5.5 A.

7.3.5 Decay Modes

During PWM current chopping, the H-bridge is enabled to drive through the motor winding until the PWM current chopping threshold is reached. This is shown in Figure 9, Item 1. The current flow direction shown indicates positive current flow in the step table below.

Once the chopping current threshold is reached, the H-bridge can operate in two different states, fast decay or slow decay.

In fast decay mode, once the PWM chopping current level has been reached, the H-bridge reverses state to allow winding current to flow in a reverse direction. The opposite FETs are turned on; as the winding current approaches zero, the bridge is disabled to prevent any reverse current flow. Fast decay mode is shown in Figure 9, item 2.

In slow decay mode, winding current is recirculated by enabling both of the low-side FETs in the bridge. This is shown in Figure 9, Item 3.

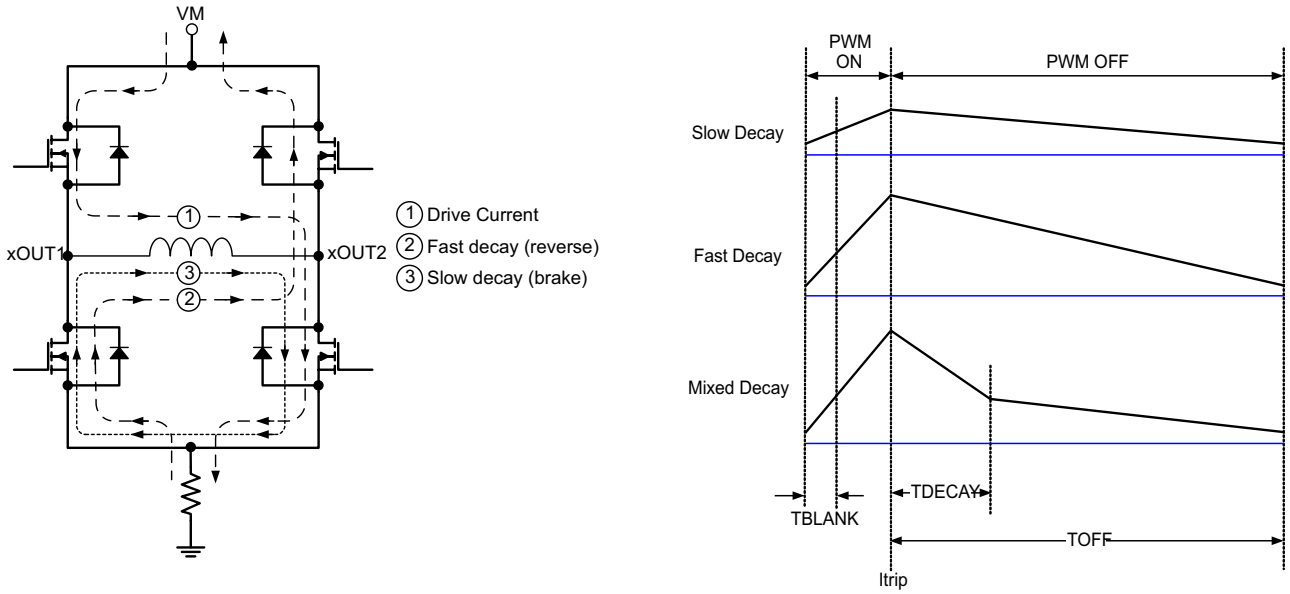


Figure 9. Decay Modes

The DRV8711 supports fast decay and slow decay modes in both indexer and direct PWM modes. In addition, in indexer mode only, it supports fixed mixed decay and auto-mixed decay modes. Decay mode is selected by the DECMOD bits in the DECAY register.

Mixed decay mode begins as fast decay, but after a programmable period of time (set by the TDECAY bits in the DECAY register) switches to slow decay mode for the remainder of the fixed off time. Even if mixed decay is selected, if the current is increasing or remaining the same (per the step table), then slow decay is used.

Auto-mixed decay mode samples the current level at the end of the blanking time, and if the current is above the Itrip threshold, immediately changes the H-bridge to fast decay. During fast decay, the (negative) current is monitored, and when it falls below the Itrip threshold (and another blanking time has passed), the bridge is switched to slow decay. Once the fixed off time expires, a new cycle is started.

If the bridge is turned on and at the end of TBLANK the current is below the Itrip threshold, the bridge remains on until the current reaches Itrip. Then slow decay is entered for the fixed off time, and a new cycle begins.

See Figure 10 and Figure 11.

The upper waveform shows the behavior if I < Itrip at the end of tBLANK. At slow motor speeds, where back EMF is not significant, the current increase during the ON phase is the same magnitude as the current decrease in fast decay, because both times are controlled by tBLANK, and the rate of change is the same (full VM is applied to the load inductance in both cases, but in opposite directions). In this case, the current will gradually be driven down until the peak current is just hitting Itrip at the end of the blanking time, after which some cycles will be slow decay, and some will be mixed decay.

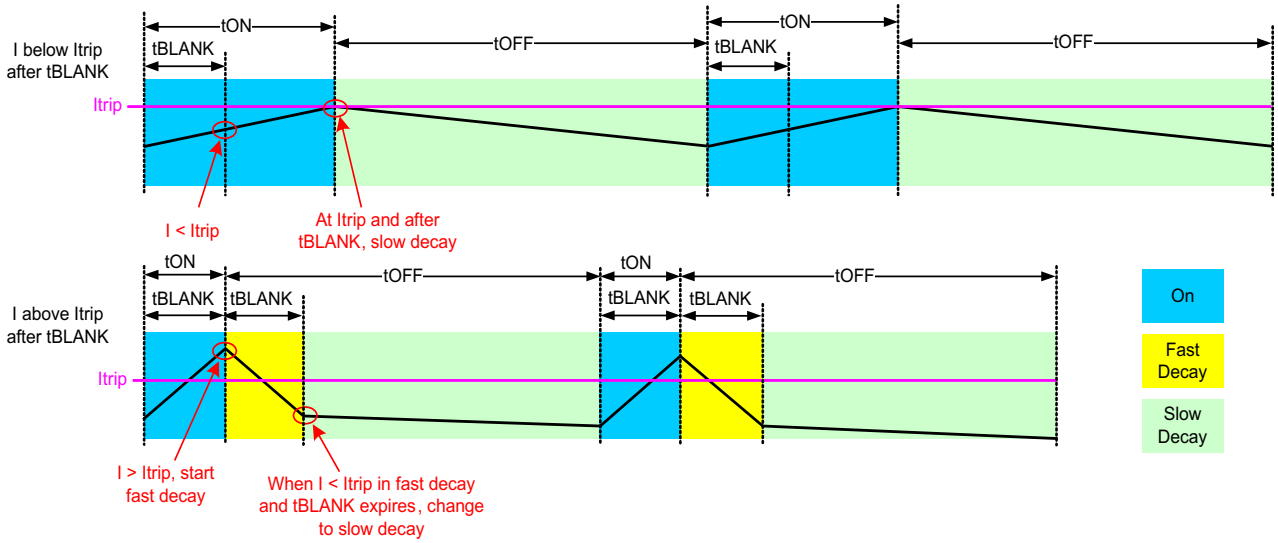


Figure 10. I < Itrip at the End of tBLANK

If the Itrip level changes during a PWM cycle (in response to a step command to the indexer), the current cycle is immediately terminated, and a new cycle is begun. Refer to the drawing below.

If the Itrip level has increased, the H-bridge will immediately turn on; if the Itrip level has decreased, fast decay mode is begun immediately. The top waveform shows what happens when the Itrip threshold decreases during a PWM cycle. The lower Itrip level results in the current being above the Itrip threshold at the end of tBLANK on the following cycle. Fast decay is entered until the current is driven below the Itrip threshold.

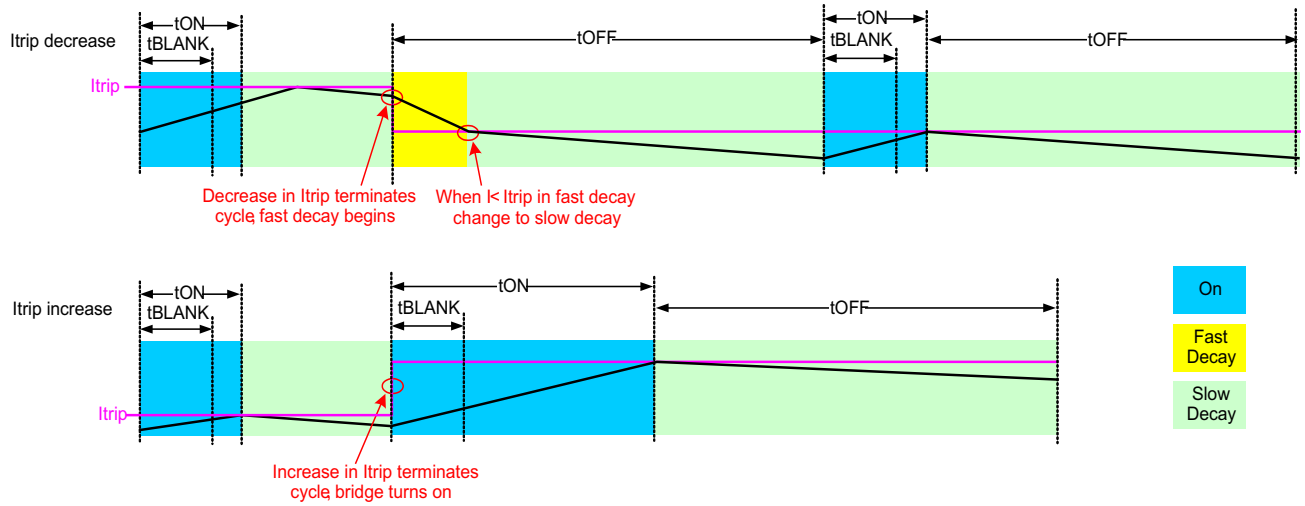


Figure 11. Itrip Level Changing During a PWM Cycle

To accurately detect zero current, an internal offset has been intentionally placed in the zero current detection circuit. If an external filter is placed on the current sense resistor to the xISENN and xISENP pins, symmetry must be maintained. This means that any resistance between the bottom of the R_{ISENSE} resistor and xISENN must be matched by the same resistor value (1% tolerance) between the top of the R_{ISENSE} resistor and xISENP. Ensure a maximum resistance of 500 Ω. The capacitor value should be chosen such that the RC time constant is between 50 ns and 60 ns. Any external filtering on these pins is optional and not required for operation.

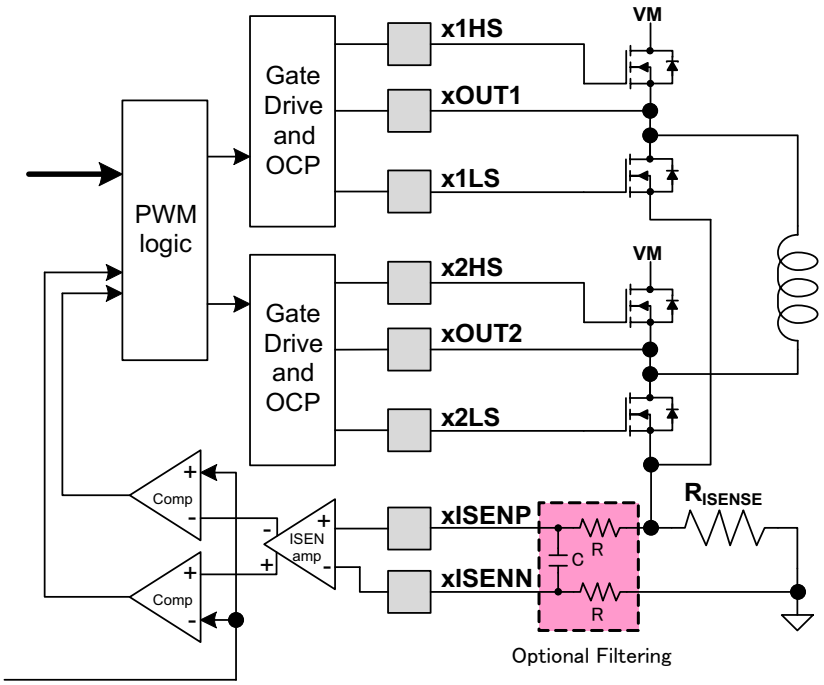


Figure 12. Optional Filtering Between R_{ISENSE} and xINSENx

7.3.6 Blanking Time

After the current is enabled in an H-bridge, the voltage on the ISEN pin is ignored for a period of time before enabling the current sense circuitry. This blanking time is adjustable from 1 µS to 5.12 µs, in 20 ns increments, by setting the TBLANK bits in the BLANK register. Note that the blanking time also sets the minimum on time of the PWM.

The same blanking time is applied to the fast decay period in auto decay mode. The PWM will ignore any transitions on Itrip after entering fast decay mode, until the blanking time has expired.

To provide better current control at very low current steps, an adaptive blanking time mode can be enabled by setting the ABT bit in the BLANK register. If ABT is set, at current levels below 30% of full scale current (as determined by the step table), the blanking time (so also the minimum on time) is cut in half, to 50% of the value programmed by the TBLANK bits.

For higher degrees of micro-stepping, TI recommends enabling ABT bit for better current regulation.

7.3.7 Predrivers

An internal charge pump circuit and predrivers inside the DRV8711 directly drive N-channel MOSFETs, which drive the motor current.

The peak drive current of the predrivers is adjustable by setting the bits in the DRIVE register. Peak source currents may be set to 50 mA, 100 mA, 150 mA, or 200 mA. The peak sink current is approximately 2x the peak source current. Adjusting the peak current will change the output slew rate, which also depends on the FET input capacitance and gate charge.

When changing the state of the output, the peak current is applied for a short period of time (tDRIVE), to charge the gate capacitance. After this time, a weak current source is used to keep the gate at the desired state. When selecting the gate drive strength for a given external FET, the selected current must be high enough to fully charge and discharge the gate during the time when driven at full current, or excessive power will be dissipated in the FET.

During high-side turnon, the low-side gate is pulled low. This prevents the gate-source capacitance of the low-side FET from inducing turnon.

The predriver circuits include enforcement of a dead time in analog circuitry, which prevents the high-side and low-side FETs from conducting at the same time. Additional dead time is added with digital delays. This delay can be selected by setting the DTIME bits in the CTRL register.

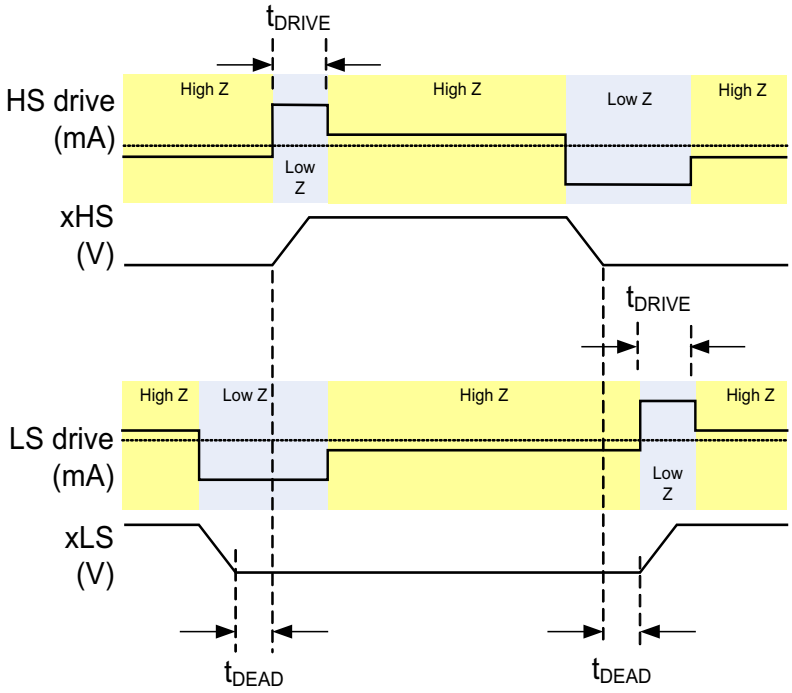


Figure 13. Predrivers

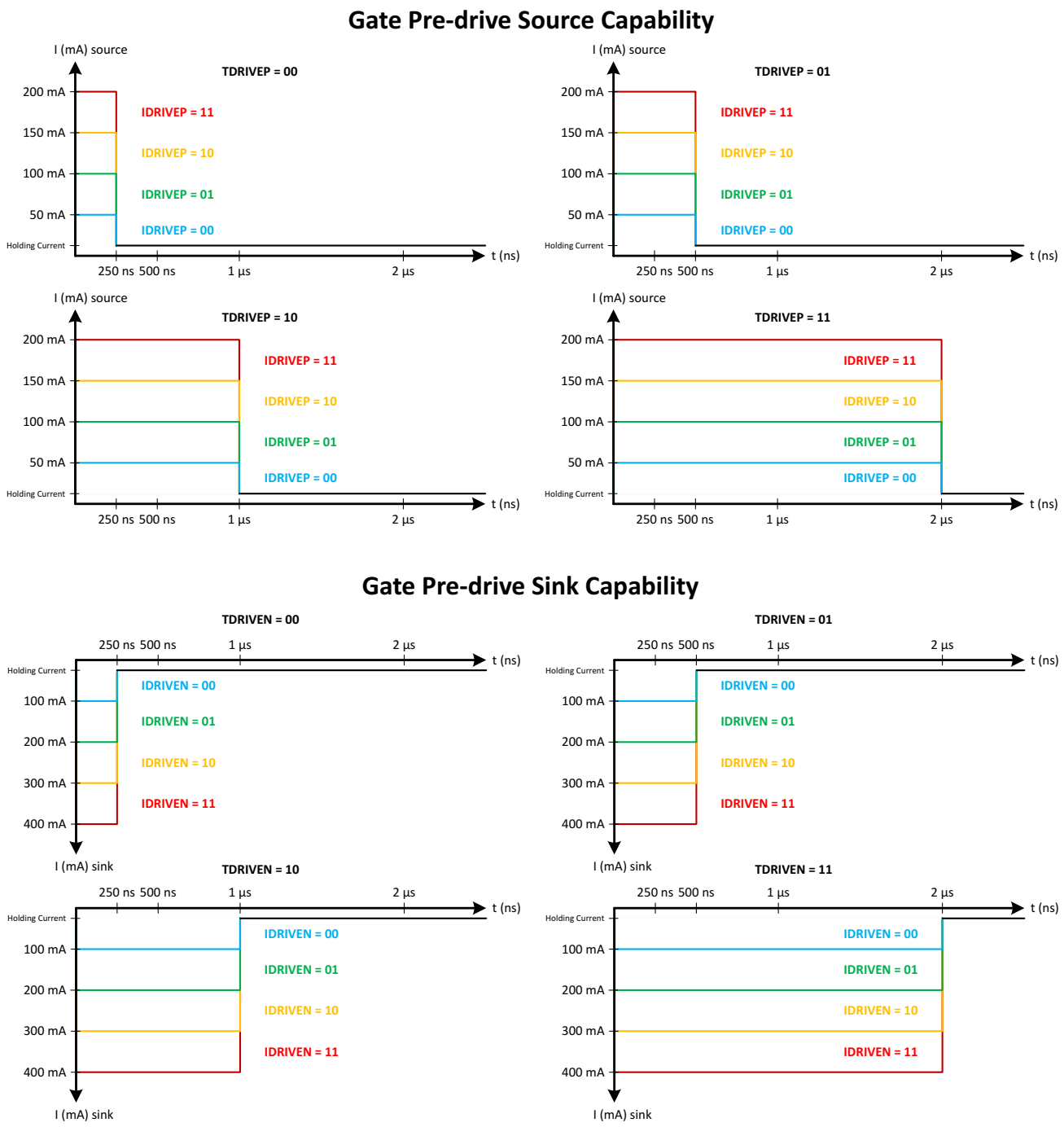


Figure 14. Gate Pre-Drive Source/Sink Capability

7.3.8 Configuring Predrivers

IDRIVE and TDRIVE are selected based on the size of external FETs used. These registers need to be configured so that the FET gates are charged completely during TDRIVE. If IDRIVE and TDRIVE are chosen to be too low for a given FET, then the FET may not turn on completely. TI suggests adjusting these values in-system with the required external FETs and stepper motor to determine the best possible setting for any application.

TDRIVE will not increase the PWM time or change the PWM chopping frequency.

In a system with capacitor charge Q and desired rise time RT, IDRIVE and TDRIVE can be initially selected based on:

IDRIVE > Q / RT

TDRIVE > 2 × RT

For best results, select the smallest IDRIVE and TDRIVE that meet the above conditions.

Example:

If the gate charge is 15 nC and the desired rise time is 400 ns, then select:

IDRIVEP = 50 mA, IDRIVEN = 100 mA

TDRIVEP = TDRIVEN = 1 µs

7.3.9 External FET Selection

In a typical setup, the DRV8711 can support external FETs over 50 nC each. However, this capacity can be lower or higher based on the device operation. For an accurate calculation of FET driving capacity, use the following equation.

$$Q < \frac{20mA \bullet (2 \bullet DTIME + TBLANK + TOFF)}{4} \quad (3)$$

Example:

If a DTIME is set to 0 (400 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0 (500 ns), then the DRV8711 will support Q < 11.5 nC FETs (this is an absolute worst-case scenario with a PWM frequency approximately 430 kHz).

If a DTIME is set to 0 (400 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0x14 (10 µs), then the DRV8711 will support Q < 59 nC FETs (PWM frequency approximately 85 kHz).

If a DTIME is set to 0 (400 ns), TBLANK is set to 0 (1 µs), and TOFF is set to 0x60 (48 µs), then the DRV8711 will support Q < 249 nC FETs (PWM frequency approximately 20 kHz).

7.3.10 Stall Detection

The DRV8711 implements a back EMF monitoring scheme that is capable of detecting a stall during stepper motor motion. This stall detection is intended to be used to get an indication when a motor is run into a mechanical stop, or when an increased torque load on the motor causes it to stall.

To determine that a stall has occurred, a drop in motor back EMF is detected. The DRV8711 supports two methods of this detection: an automatic internal stall detection circuit, or the ability to use an external microcontroller to monitor back EMF.

During a zero-current step, one side of the H-bridge is placed in a high impedance state, and the opposite low-side FET is turned on for a brief duration defined by TORQUE register SMPLTH bit [10:8]. This allows the current to decay quickly through the low-side FET and the opposite body diode. Which side of the bridge is tri-state and which one is driven low depends on the current direction on the previous step. The bridge with the high side that has been actively PWMed (at the beginning of the PWM cycle during blank time) before entering the zero-current step will be held low and the opposite side will be tri-stated.

Back EMF is sampled on the tri-stated output pin at the end of SMPLTH time (TORQUE register bit [10:8]). The back EMF from the selected pin is divided by 4, 8, 16, or 32, depending on the setting of the VDIV bits in the STALL register. The voltage is buffered and held on an external capacitor placed on the BEMF pin. The signal on the BEMF output pin can be further processed by a microcontroller to implement more advanced control and stall detection algorithms.

The SMPLTH bit [10] is a write-only bit. When read, the bit always reads 0. TI recommends to maintain the value of the bit locally. When a change in the TORQUE register is desired, the bit can be read locally and added to the other bits to complete the value.

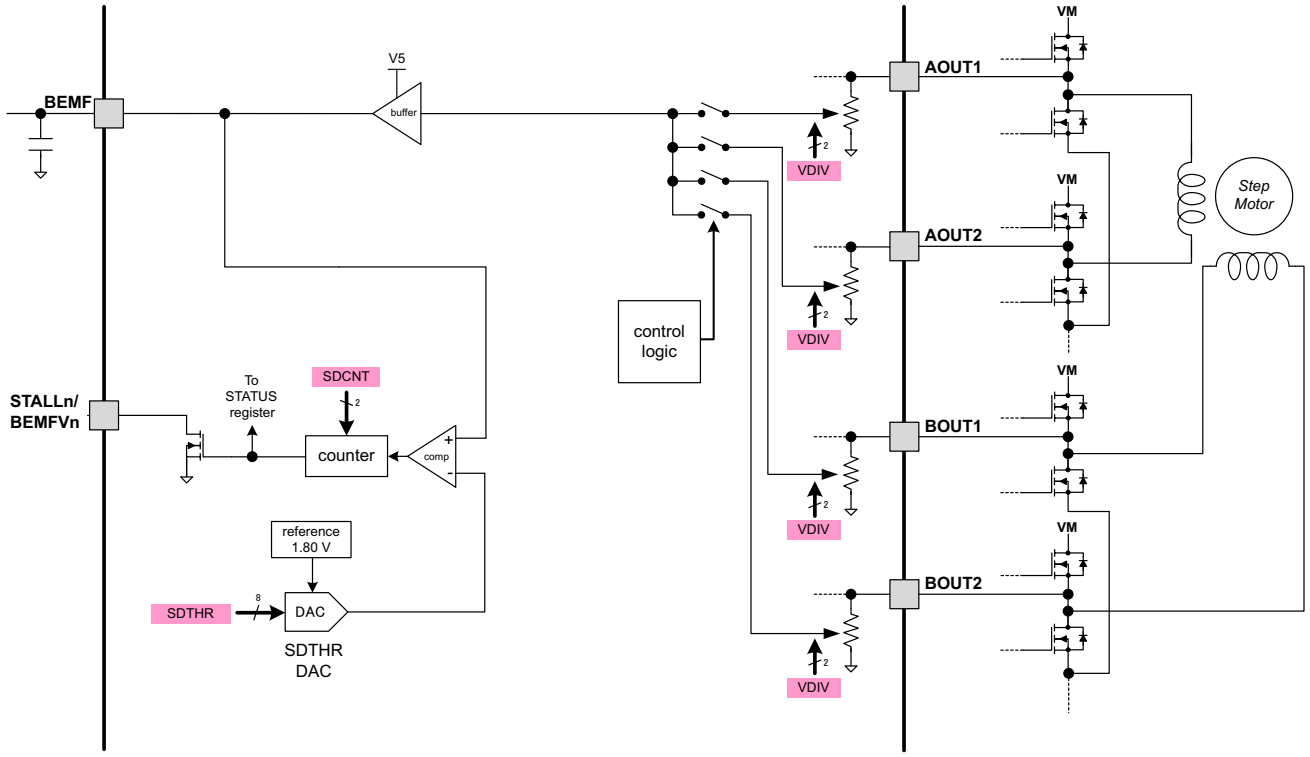


Figure 15. Stall Detection

7.3.10.1 Internal Stall Detection

To use internal stall detection, the EXSTALL bit in the CTRL register is set to 0. In this mode, the STALLn/BEMFVn output pin is used to signal a valid stall condition.

The time between step inputs must be greater than SMPLTH time for back EMF sampling.

Using internal stall detection, a stall is detected when the sampled back EMF drops below the value set by the SDTHR bits in the STALL register. A programmable counter circuit allows the assertion of the STALLn output to be delayed until the back EMF has been sampled below the SDTHR value for more than one zero-current step. The counter is programmed by the SDCNT bits in the STALL register, and provides selections of 1, 2, 4, or 8 steps.

When the stall is detected (at the end of a SMPLTH interval), the STALLn/BEMFVn pin is driven active low, and the STD bit and the STDLAT bit in the STATUS register are set. The STALLn/BEMFVn pin will deassert and the STD bit will automatically clear at the next zero-current step if a stall condition is not detected, while the STDLAT bit will remain set until a 0 is written to it. The STDLAT is reset when the STD bit clears after the first zero-cross step that does not detect a stall condition.

This stall detection scheme is only effective when the motor is stalled while running at or above some minimum speed. Because it relies on detecting a drop in motor back EMF, the motor must be rotating with sufficient speed to generate a detectable back EMF. During motor start-up, and at very slow step rates, the stall detection is not reliable.

Because back EMF can only be sampled during a zero-current state, stall detection is not possible in full step mode. During full-step operation, the stall detect circuit is gated off to prevent false signaling of a stall.

The correct setting of the SDTHR bits needs to be determined experimentally. It is dependent on many factors, including the electrical and mechanical characteristics of the load, the peak current setting, and the supply voltage.

7.3.10.2 External Stall Detection

To use an external microcontroller to manage stall detection, the EXSTALL bit in the CTRL register is set to 1. In this mode, the STALLn / BEMFVn output pin is used to signal a valid back EMF measurement is ready. In addition, the SDT and SDTLAT bits are also set at this time.

BEMFVn and BEMF are still valid outputs in this mode even if the step time is smaller than SMPLTH time.

When the BEMFVn pin goes active low, it is an indication that a valid back EMF voltage measurement is available. This signal could be used, for example, to trigger an interrupt on a microcontroller. The microcontroller can then sample the voltage present (using an A/D converter) on the BEMF pin.

After sampling the back EMF voltage, the microcontroller writes a 0 to the SDTLAT bit to clear the SDT bit and BEMFVn pin, in preparation for the next back EMF sample. If the SDTLAT bit is not cleared by the microcontroller, it will automatically be cleared in the next zero-current step.

For either internal or external stall detection, at very high motor speeds when the PWM duty cycle approaches 100%, the inductance of the motor and the short duration of each step may cause the time required for current recirculation to exceed the step time. In this case, back EMF will not be correctly sampled, and stall detection cannot function. This condition occurs most at high degrees of micro-stepping, because the zero current step lasts for a shorter duration. It is advisable to run the motor at lower degrees of micro-stepping at higher speeds to allow time for current recirculation if stall detection is needed in this condition.

7.3.11 Protection Circuits

The DRV8711 is fully protected against undervoltage, overcurrent and overtemperature events.

7.3.11.1 Overcurrent Protection (OCP)

Overcurrent is sensed by monitoring the voltage drop across the external FETs. If the voltage across a driven FET exceeds the value programmed by the OCPTH bits in the DRIVE register for more than the time period specified by the OCPDEG bits in the DRIVE register, an OCP event is recognized. When operating in direct PWM mode, during an OCP event, the H-bridge experiencing the OCP event is disabled; if operating in indexer mode, both H-bridges will be disabled. In addition, the corresponding xOCP bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridge(s) will remain off, and the xOCP bit will remain set, until it is written to 0, or the device is reset.

In order to calculate the current needed to trip OCP, use the OCPTH value and the FET $R_{DS(ON)}$:

$$I_{OCP} = \frac{OCPTH}{R_{DS(ON)}(\Omega)} \quad (4)$$

If the motor winding parasitic capacitance, C_L, is very large (on the order of 1 µF), then it may be required to increase OCPDEG to account for the large inrush current. For C_L less than 10 nF, the default value for this register should be sufficient.

7.3.11.2 Predriver Fault

In PWM mode, if excessive current is detected on the gate drive outputs (which would be indicative of a failed/shorted output FET or PCB fault), the H-bridge experiencing the fault is disabled, the xPDF bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridge will remain off, and the xPDF bit will remain set until it is written to 0 or the device is reset.

When in indexer mode, both H-bridges are disabled, the xPDF bit in the STATUS register is set, and the FAULTn pin is driven low. The H-bridges will remain off, and the xPDF bit will remain set until it is written to 0 or the device is reset.

7.3.11.3 Thermal Shutdown (TSD)

If the die temperature exceeds safe limits, all FETs in the H-bridge will be disabled, the OTS bit in the STATUS register will be set, and the FAULTn pin will be driven low. Once the die temperature has fallen to a safe level operation will automatically resume and the OTS bit will reset. The FAULTn pin will be released after operation has resumed.

7.3.11.4 Undervoltage Lockout (UVLO)

If at any time the voltage on the VM pin falls below the undervoltage lockout threshold voltage, all FETs in the H-bridge will be disabled, the UVLO bit in the STATUS register will be set, and the FAULTn pin will be driven low. Operation will resume when VM rises above the UVLO threshold. The UVLO bit will remain set until it is written to 0. The FAULTn pin will be released after operation has resumed.

During any of these fault conditions, the STEP input pin will be ignored.

7.4 Device Functional Modes

7.4.1 RESET and SLEEPn Operation

An internal power-up reset circuit monitors the voltage applied to the VM pin. If VM falls below the VM undervoltage lockout voltage, the part is reset, as described below for the case of asserting the RESET pin.

If the RESET pin is asserted, all internal logic including the indexer is reset. All registers are returned to their initial default conditions. The power stage will be disabled, and all inputs, including STEP and the serial interface, are ignored when RESET is active.

On exiting reset state, some time (approximately 1 mS) needs to pass before the part is fully functional.

Applying an active low input to the SLEEPn input pin will place the device into a low power state. In sleep mode, the motor driver circuitry is disabled, the gate drive regulator and charge pump are disabled, and all analog circuitry is placed into a low power state. The digital circuitry in the device still operates, so the device registers can still be accessed via the serial interface.

When SLEEPn is active, the RESET pin does not function. SLEEPn must be exited before RESET will take effect. SLEEPn must also be exited to clear the UVLO bit in the status register.

When exiting from sleep mode, some time (approximately 1 mS) needs to pass before applying a STEP input, to allow the internal circuitry to stabilize.

7.4.2 Microstepping Drive Current

Figure 16 shows examples of stepper motor current in one of the windings. Because these waveforms are dependent on DRV8711 register settings as well as the external FETs, sense resistor, and stepper motor, they should only be used as a reference.

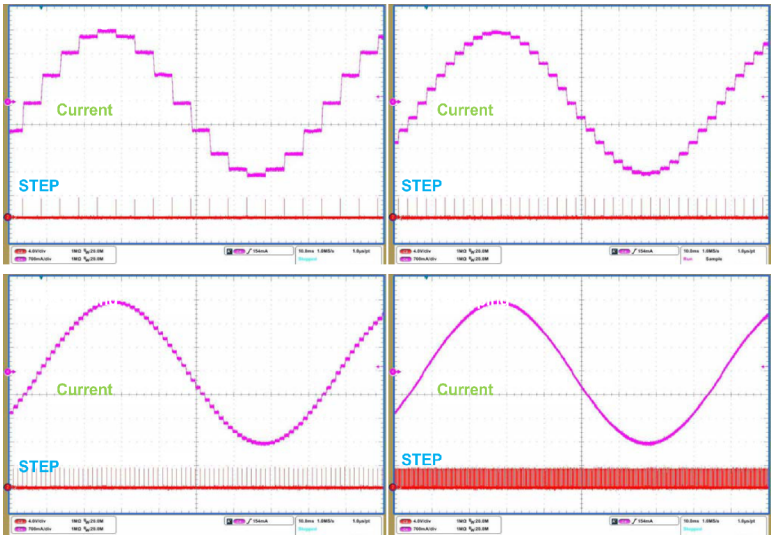


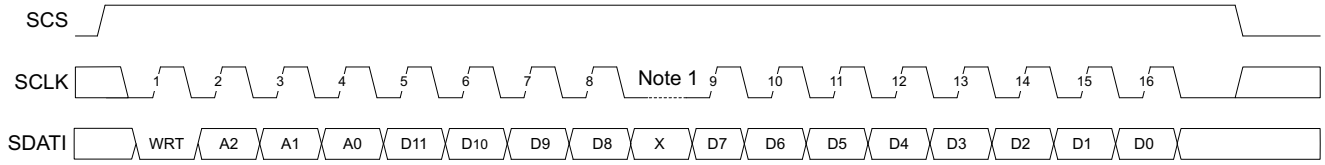
Figure 16. Microstepping Drive Current

7.5 Programming

7.5.1 Serial Data Format

The serial data consists of a 16-bit serial write, with a read/write bit, 3 address bits and 12 data bits. The 3 address bits identify one of the registers defined in the register section above. To complete the read or write transaction, SCS must be set to a logic 0.

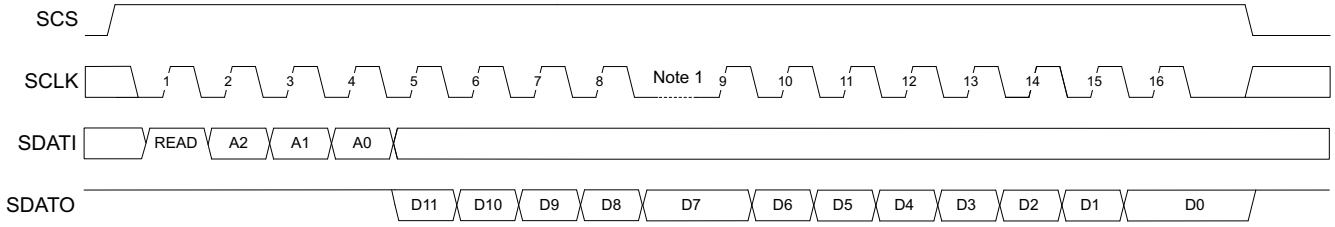
To write to a register, data is shifted in after the address as shown in the timing diagram below. The first bit at the beginning of the access must be logic low for a write operation.



A. Any amount of time may pass between bits, as long as SCS stays active high. This allows two 8-bit writes to be used.

Figure 17. Write Operation

Data may be read from the registers through the SDATO pin. During a read operation, only the address is used form the SDATI pin; the data bits following are ignored. The first bit at the beginning of the access must be logic high for a read operation.



(1) Any amount of time may pass between bits, as long as SCS stays active high. This allows two 8-bit writes to be used.

Figure 18. Read Operation

7.6 Register Maps

7.6.1 Control Registers

The DRV8711 uses internal registers to control the operation of the motor. The registers are programmed through a serial SPI communications interface. At power up or reset, the registers will be preloaded with default values as shown in *CTRL Register (Address = 0x00)* to *STATUS Register (Address = 0x07)*.

Figure 19 is a map of the DRV8711 registers.

Individual register contents are defined in *CTRL Register (Address = 0x00)* to *STATUS Register (Address = 0x07)*.

Register Maps (continued)

DRV8711 REGISTER MAP

Name	11	10	9	8	7	6	5	4	3	2	1	0		Address Hex
CTRL	DTIME		ISGAIN		EXSTALL	MODE				RSTEP	RDIR	ENBL	RW	00
TORQUE	Reserved	SMPLTH			TORQUE								RW	01
OFF	Reserved			PWMMODE	TOFF								RW	02
BLANK	Reserved			ABT	TBLANK								RW	03
DECAY	Reserved	DECMOD			TDECAY								RW	04
STALL	VDIV		SDCNT		SDTHR								RW	05
DRIVE	IDRIVEP		IDRIVEN		TDRIVEP		TDRIVEN		OCPDEG		OCPTH		RW	06
STATUS	Reserved				STDLAT	STD	UVLO	BPDF	APDF	BOCP	AOCP	OTS	RW	07
Name	11	10	9	8	7	6	5	4	3	2	1	0		Address Hex

Figure 19. DRV8711 Register Map

7.6.2 CTRL Register (Address = 0x00)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
0	ENBL	1	R/W	0	**0: Disable motor** 1: Enable motor
1	RDIR	1	R/W	0	**0: Direction set by DIR pin** 1: Direction set by inverse of DIR pin
2	RSTEP	1	W	0	0: No action 1: Indexer will advance one step; automatically cleared after write
6-3	MODE	4	R/W	0010	0000: Full-step, 71% current 0001: Half step **0010: 1/4 step** 0011: 1/8 step 0100: 1/16 step 0101: 1/32 step 0110: 1/64 step 0111: 1/128 step 1000: 1/256 step 1001 – 1111: Reserved
7	EXSTALL	1	R/W	0	**0: Internal stall detect** 1: External stall detect
9-8	ISGAIN	2	R/W	00	ISENSE amplifier gain set **00: Gain of 5** 01: Gain of 10 10: Gain of 20 11: Gain of 40
11-10	DTIME	2	R/W	11	Dead time set 00: 400 ns dead time 01: 450 ns dead time 10: 650 ns dead time **11: 850 ns dead time**

7.6.3 TORQUE Register (Address = 0x01)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TORQUE	8	R/W	0xFF	Sets full-scale output current for both H-bridges

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
10-8	SMPLTH(1)	3	R/W	001	Back EMF sample threshold 000: 50 µs **001: 100 µs** 010: 200 µs 011: 300 µs 100: 400 µs 101: 600 µs 110: 800 µs 111: 1000 µs
11	Reserved	1	-	-	Reserved

(1) Bit 10 is a write only bit. When read, bit 10 will always return 0.

7.6.4 OFF Register (Address = 0x02)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TOFF	8	R/W	0x30	Sets fixed off time, in increments of 500 ns 0x00: 500 ns 0xFF: 128 µs
8	PWMMODE	1	R/W	0	**0: Use internal indexer** 1: Bypass indexer, use xINx inputs to control outputs
11-9	Reserved	3	-	-	Reserved

7.6.5 BLANK Register (Address = 0x03)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TBLANK	8	R/W	0x80	Sets current trip blanking time, in increments of 20 ns 0x00: 1 µs … 0x32: 1 µs 0x33: 1.02 µs … 0xFE: 5.10 µs 0xFF: 5.12 µs Also sets minimum on-time of PWM
8	ABT	1	R/W	0	**0: Disable adaptive blanking time** 1: Enable adaptive blanking time
11-9	Reserved	3	-	-	Reserved

7.6.6 DECAY Register (Address = 0x04)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	TDECAY	8	R/W	0x10	Sets mixed decay transition time, in increments of 500 ns
10-8	DECMOD	3	R/W	001	000: Force slow decay at all times **001: Slow decay for increasing current, mixed decay for decreasing current (indexer mode only)** 010: Force fast decay at all times 011: Use mixed decay at all times 100: Slow decay for increasing current, auto mixed decay for decreasing current (indexer mode only) 101: Use auto mixed decay at all times 110 – 111: Reserved
11	Reserved	1	-	-	Reserved

7.6.7 STALL Register (Address = 0x05)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
7-0	SDTHR	8	R/W	0x40	Sets stall detect threshold The correct setting needs to be determined experimentally

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
9-8	SDCNT	2	R/W	00	**00: STALLn asserted on first step with back EMF below SDTHR** 01: STALLn asserted after 2 steps 10: STALLn asserted after 4 steps 11: STALLn asserted after 8 steps
11-10	VDIV	2	R/W	00	**00: Back EMF is divided by 32** 01: Back EMF is divided by 16 10: Back EMF is divided by 8 11: Back EMF is divided by 4

7.6.8 DRIVE Register (Address = 0x06)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
1-0	OCPTH	2	R/W	01	OCP threshold 00: 250 mV **01: 500 mV** 10: 750 mV 11: 1000 mV
3-2	OCPDEG	2	R/W	10	OCP deglitch time 00: 1 µs 01: 2 µs **10: 4 µs** 11: 8 µs
5-4	TDRIVEN	2	R/W	01	Low-side gate drive time 00: 250 ns **01: 500 ns** 10: 1 µs 11: 2 µs
7-6	TDRIVEP	2	R/W	01	High-side gate drive time 00: 250 ns **01: 500 ns** 10: 1 µs 11: 2 µs
9-8	IDRIVEN	2	R/W	10	Low-side gate drive peak current 00: 100 mA peak (sink) 01: 200 mA peak (sink) **10: 300 mA peak (sink)** 11: 400 mA peak (sink)
11-10	IDRIVEP	2	R/W	10	High-side gate drive peak current 00: 50 mA peak (source) 01: 100 mA peak (source) **10: 150 mA peak (source)** 11: 200 mA peak (source)

7.6.9 STATUS Register (Address = 0x07)

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
0	OTS	1	R/W	0	0: Normal operation 1: Device has entered overtemperature shutdown Write a 0 to this bit to clear the fault. Operation automatically resumes when the temperature has fallen to safe levels.
1	AOCP	1	R/W	0	0: Normal operation 1: Channel A overcurrent shutdown Write a 0 to this bit to clear the fault and resume operation
2	BOCP	1	R/W	0	0: Normal operation 1: Channel B overcurrent shutdown Write a 0 to this bit to clear the fault and resume operation
3	APDF	1	R/W	0	0: Normal operation 1: Channel A predriver fault Write a 0 to this bit to clear the fault and resume operation.
4	BPDF	1	R/W	0	0: Normal operation 1: Channel B predriver fault Write a 0 to this bit to clear the fault and resume operation

BIT	NAME	SIZE	R/W	DEFAULT	DESCRIPTION
5	UVLO	1	R/W	0	0: Normal operation 1: Undervoltage lockout Write a 0 to this bit to clear the fault. The UVLO bit cannot be cleared in sleep mode. Operation automatically resumes when VM has increased above V_{UVLO}
6	STD	1	R	0	0: Normal operation 1: Stall detected
7	STDLAT	1	R/W	0	0: Normal operation 1: Latched stall detect Write a 0 to this bit to clear the fault and resume operation
11-8	Reserved	4	-	-	Reserved

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DRV8711 is used in bipolar stepper control. The microstepping motor predriver provides additional precision and a smooth rotation from the stepper motor.

8.1.1 Sense Resistor

For optimal performance, it is important for the sense resistor to be:

- Surface-mount
- Low inductance
- Rated for high enough power
- Placed closely to the motor driver

The power dissipated by the sense resistor equals $I_{RMS}^2 \times R$. For example, if peak motor current is 3 A, RMS motor current is 2 A, and a 0.05-Ω sense resistor is used, the resistor will dissipate $2\ A^2 \times 0.05\ \Omega = 0.2$ W. The power quickly increases with higher current levels.

Resistors typically have a rated power within some ambient temperature range, along with a derated power curve for high ambient temperatures. When a PCB is shared with other components generating heat, margin should be added. It is always best to measure the actual sense resistor temperature in a final system, along with the power MOSFETs, as those are often the hottest components.

Because power resistors are larger and more expensive than standard resistors, it is common practice to use multiple standard resistors in parallel, between the sense node and ground. This distributes the current and heat dissipation.

8.1.2 Optional Series Gate Resistor

In high current or high voltage applications, the low side predriver fault may assert due to noise in the system. In this application, TI recommends placing a 47 to 120-Ω resistor in series with the low side output and the gate of the low side FET. TI also recommends setting the dead time to 850 ns when adding a series resistor.

8.2 Typical Application

The following design is a common application of the DRV8711.

Typical Application (continued)

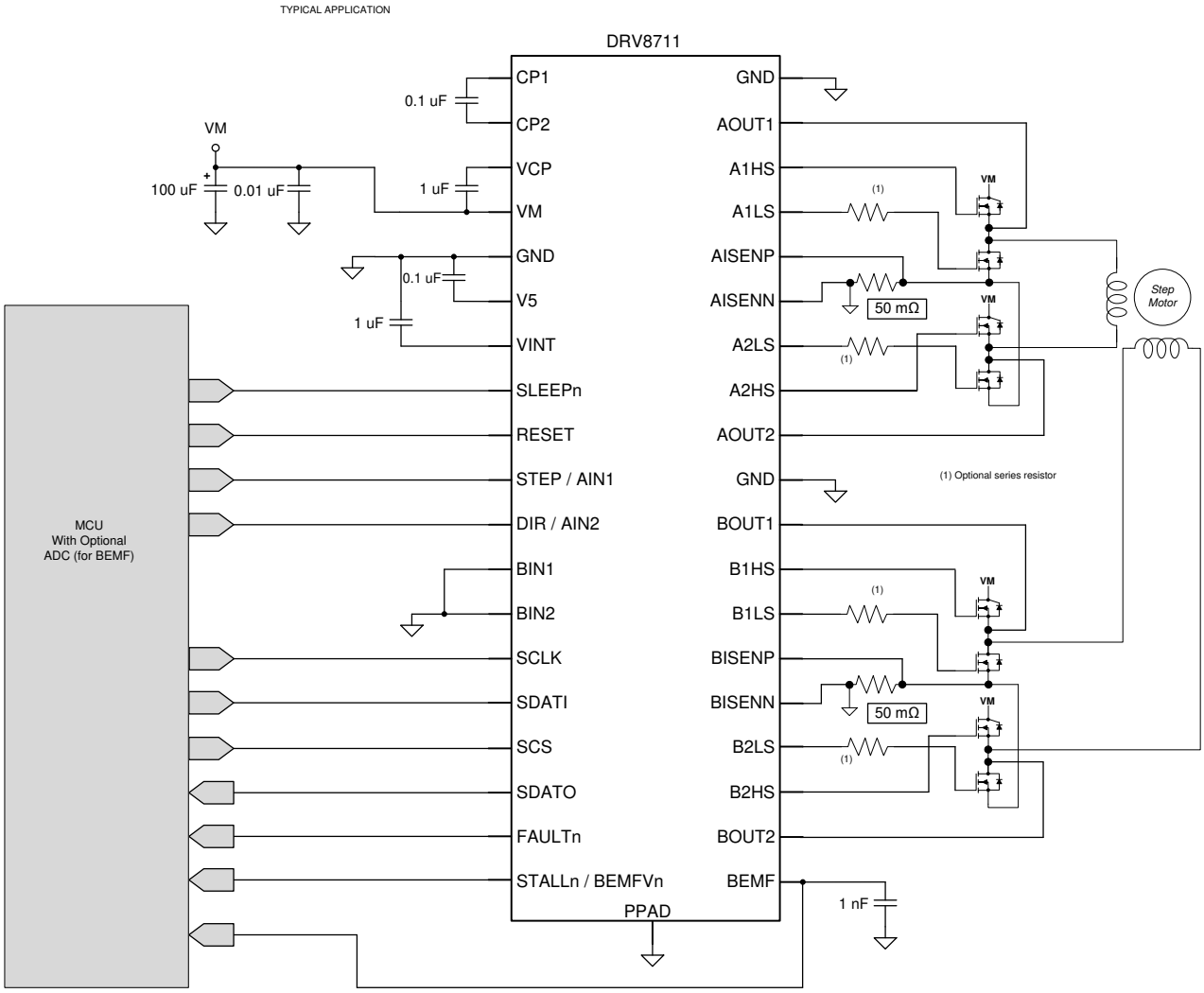


Figure 20. Typical Application Schematic

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 5 as the input parameters.

Table 5. Design Parameter

	Item	Reference	Example
1	Supply voltage	VM	24 V
2	MOSFET gate charge	Q_g	18 nC
3	MOSFET drain to source resistance	$R_{DS(ON)}$	3.5 mΩ
4	Motor winding resistance	R_L	1.0 Ω/phase
5	Motor winding inductance	L_L	3.5 mH/phase
6	Motor winding parasitic capacitance	C_L	10 nF
7	Motor full step angle	θ_{step}	1.8°/step
8	Motor current	I_L	3.0 A/phase
9	Sense resistor	R_{SENSE}	0.033 Ω
10	Target microstepping level	n_m	16 steps

Typical Application (continued)

Table 5. Design Parameter (continued)

Item		Reference	Example
12	Target motor speed	v	120 rpm
13	Target full-scale current	I_{FS}	1.25 A
14	Target MOSFET rise time	RT	600 ns
15	Target pulse-width modulation (PWM) chopping frequency	f_{PWM}	40 kHz
16	Target stall detect stepping speed	f_{stall}	60 rpm
17	Target overcurrent protection level	I_{OCP}	2 A

8.2.2 Detailed Design Procedure

8.2.2.1 Set Step Rate

The first step in configuring the DRV8711 requires the desired motor speed and microstepping level. If the target application requires a constant speed, then a square wave with frequency f_{step} must be applied to the STEP pin.

If the target motor start-up speed is too high, the motor will not spin. Make sure that the motor can support the target speed or implement an acceleration profile to bring the motor up to speed.

For a desired motor speed (V), microstepping level (n_m), and motor full step angle (θ_{step}),

$$f_{step}\left(\mu steps/second\right) = \frac{v\left(\frac{rotations}{minute}\right) \times 360\left(\frac{^\circ}{rotation}\right) \times n_m\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times \theta_{step}\left(\frac{^\circ}{step}\right)} \quad (5)$$

$$f_{step}\left(\mu steps/second\right) = \frac{120\left(\frac{rotations}{minute}\right) \times 360\left(\frac{^\circ}{rotation}\right) \times 8\left(\frac{\mu steps}{step}\right)}{60\left(\frac{seconds}{minute}\right) \times 1.8\left(\frac{^\circ}{step}\right)} \quad (6)$$

θ_{step} can be found in the stepper motor data sheet or written on the motor itself.

For the DRV8711, the microstepping level is set by the MODE bits in the CTRL register. Higher microstepping will mean a smoother motor motion and less audible noise, but will increase switching losses and require a higher f_{step} to achieve the same motor speed.

NOTE

All register defaults shown in the following **CTRL Register** table are examples and subject to change. Refer to the datasheet to ensure the correct default settings are used.

CTRL Register **Address = 0x00h**

Bit	Name	Size	R/W	Default	Description
6-3	MODE	4	R/W	0110	0000: Full-step, 71% current (n_m = 1) 0001: Half step (n_m = 2) *0010: 1/4 step (n_m = 4)* 0011: 1/8 step (n_m = 8) 0100: 1/16 step (n_m = 16) 0101: 1/32 step (n_m = 32) 0110: 1/64 step (n_m = 64) 0111: 1/128 step (n_m = 128) 1000: 1/256 step (n_m = 256)

8.2.2.2 Calculate Current Regulation

In a stepper motor, the set full-scale current (I_{FS}) is the maximum current driven through either winding. For the DRV8711, this quantity will depend on the analog voltage, the programmed torque and gain values, and the sense resistor value (R_{SENSE}). During stepping, IFS defines the current chopping threshold (I_{TRIP}) for the maximum current step. The gain of DRV8711 is set for 5 V/V.

$$I_{FS}(A) = \frac{2.75\,(V) \times TORQUE}{256 \times ISGAIN \times R_{SENSE}\,(\Omega)} \quad (7)$$

To achieve I_{FS} = 1.25 A with R_{SENSE} of 0.2 Ω with a gain of 5, TORQUE should be set to 116(dec).

I_{FS} is set by a comparator which compares the voltage across R_{SENSE} to a reference voltage. There is a current sense amplifier built in with programmable gain through ISGAIN. Note that I_{FS} must also follow Equation 8 in order to avoid saturating the motor. VM is the motor supply voltage, and R_L is the motor winding resistance.

$$I_{FS}\,(A) < \frac{VM(V)}{R_L\,(\Omega) + 2 \times R_{DS(ON)}\,(\Omega) + R_{SENSE}\,(\Omega)} \quad (8)$$

TORQUE is a register used to scale the output. If TORQUE = 0xFF, then the SIN DAC is scaled by 1. As TORQUE is decreased, the reference is decreased as well.

As an example, the torque register can be reduced when the motor has been stopped. Reducing torque at this point could reduce the current required to hold the motor.

TORQUE Register Address = 0x01h

Bit	Name	Size	R/W	Default	Description
7-0	TORQUE	8	R/W	0xFFh	Sets full-scale output current for both H-bridges

ISGAIN controls the gain of the current sense amplifier. Note that from Equation 7, increasing this gain will decrease I_{FS} since it is used in the feedback path.

CTRL Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
9-8	ISGAIN	2	R/W	00	ISENSE amplifier gain set *00: Gain of 5* 01: Gain of 10 10: Gain of 20 11: Gain of 40

8.2.2.3 Support External FETs

It is critical to ensure that any external FETs used can support the PWM current chopping frequency desired. Equation 3 is used to calculate the maximum FET driving capability of the DRV8711:

$$Q_g\,(nC) < \frac{20mA \times (2 \times DTIME + TBLANK + TOFF)}{4} \approx \frac{20mA}{4 \times f_{PWM}(Hz)} \quad (9)$$

In Equation 3, 2 × DTIME + TBLANK + TOFF is the worst-case scenario (smallest time period) for PWM current chopping ($1/f_{PWM}$). Since the PWM current chopping frequency is not fixed, the desired f_{PWM} only gives an estimate on the worst-case FET driving capacity.

DTIME is the dead-time inserted between turning off a low-side FET and turning on a high-side FET, or vice versa. During this time, both FETs are in High-Z, and current is conducted through the body diodes in asynchronous decay. It is recommended to leave DTIME as its default value unless the stepping speed is very high.

CTRL Register **Address = 0x00h**

Bit	Name	Size	R/W	Default	Description
11-10	DTIME	2	R/W	11	Dead time set 00: 400 ns dead time 01: 450 ns dead time 10: 650 ns dead time *11: 850 ns dead time*

TBLANK is the blanking time during PWM current chopping. This sets the minimum drive time (current is increasing) during the PWM cycle. At the beginning of the PWM cycle, the current trip value is ignored for TBLANK. In auto mixed decay mode, TBLANK is also the fast decay time if the current is higher than the current chopping level after the drive time. This value is explained more in the Blanking time section.

BLANK Register **Address = 0x03h**

Bit	Name	Size	R/W	Default	Description
7-0	TBLANK	8	R/W	0x80h	Sets current trip blanking time, in increments of 20 ns 0x00h: 1.00 µs … 0x32h: 1.00 µs 0x33h: 1.02 µs … 0xFEh: 5.10 µs 0xFFh: 5.12 µs Also sets minimum on-time of PWM

TOFF sets the time that the driver is in a decay mode after the drive phase of PWM current chopping. This value is explained more in the Decay Modes section.

OFF Register **Address = 0x02h**

Bit	Name	Size	R/W	Default	Description
7-0	TOFF	8	R/W	0x30H	Sets fixed off time, in increments of 500 ns 0x00h: 500 ns 0xFFh: 128 µs

The registers IDRIVEP, IDRIVEN, TDRIVEP, and TDRIVEN are set based on the gate charge of the external FETs used (Q_g), and the desired rise time (RT). RT is the time it will take to charge the FET gate and turn on.

$$\text{IDRIVE} > Q / RT \quad (10)$$

$$\text{TDRIVE} > 2 \times RT \quad (11)$$

IDRIVEN / IDRIVEP and TDRIVEN / TDRIVEP should be selected to be the smallest settings that meet the requirements in Equation 10 and Equation 11.

DRIVE Register Address = 0x06h

Bit	Name	Size	R/W	Default	Description
5-4	TDRIVEN	2	R/W	01	Gate drive sink time 00: 250 ns *01: 500 ns* 10: 1 µs 11: 2 µs
7-6	TDRIVEP	2	R/W	01	Gate drive source time 00: 250 ns *01: 500 ns* 10: 1 µs 11: 2 µs
9-8	IDRIVEN	2	R/W	00	Gate drive peak sink current *00: 100 mA peak (sink)* 01: 200 mA peak (sink) 10: 300 mA peak (sink) 11: 400 mA peak (sink)
11-10	IDRIVEP	2	R/W	00	Gate drive peak source current *00: 50 mA peak (source)* 01: 100 mA peak (source) 10: 150 mA peak (source) 11: 200 mA peak (source)

8.2.2.4 Pick Decay Mode

The DRV8711 supports three different decay modes: slow decay, fast decay, and mixed decay. The DRV8711 also supports automatic mixed decay mode, which minimizes current ripple. The current through the motor windings is regulated using programmable settings for blanking, decay and off time. This means that after any drive phase, when a motor winding current has hit the current chopping threshold (I_{TRIP}), the DRV8711 will place the winding in the programmed decay modes until the cycle has expired. Afterward, a new drive phase starts.

If there is a desired PWM chopping frequency, f_{PWM}, use Equation 12. Note that this will only ensure that the minimum PWM frequency is f_{PWM}, since the drive time may be longer than TBLANK.

$$\text{TBLANK} + \text{TOFF} + (2 \times \text{DTIME}) \approx 1/f_{PWM} \text{ (Hz)} \quad (12)$$

If there is no target f_{PWM}, the best way to choose TBLANK and TOFF is to tune the DRV8711 in-system based on the chosen decay mode.

In most applications, it is recommended to use auto mixed decay. This decay mode eliminates some of the disadvantages of the other decay modes when the motor is stopped.

TOFF defines the time that the device is in the defined decay mode.

OFF Register Address = 0x02h

Bit	Name	Size	R/W	Default	Description
7-0	TOFF	8	R/W	0x30h	Sets fixed off time, in increments of 500 ns 0x00h: 500 ns 0xFFh: 128 µs

TBLANK defines the minimum drive time for the PWM current chopping. I_{TRIP} is ignored during TBLANK, so the winding current may overshoot the trip level. In auto mixed decay, TBLANK also sets the fast decay time.

BLANK Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
7-0	TBLANK	8	R/W	0x80h	Sets current trip blanking time, in increments of 20ns 0x00h: 1.00 µs … 0x32h: 1.00 µs 0x33h: 1.02 µs … 0xFEh: 5.10 µs 0xFFh: 5.12 µs

If the application requires a high degree of microstepping (n_m = 64, 128, or 256), it is recommended to set the ABT bit. This enables adaptive blanking time, which will cut the blanking time in half for small current steps. Adaptive blanking time allows for more accurate current control at these lower current steps.

BLANK Register Address = 0x03h

Bit	Name	Size	R/W	Default	Description
8	ABT	1	R/W	0	*0: Disable adaptive blanking time* 1: Enable adaptive blanking time

During microstepping, current can be either increasing or decreasing from one step to the next. Fast decay can be very useful when I_{TRIP} is decreasing, because it allows the winding current to decay very rapidly and settle at the next step. Slow decay is used often because the current decays slowly and results in a lower current ripple versus fast decay. Mixed decay and auto mixed decay allow flexibility to have the advantages of both fast decay and slow decay in the same mode.

DECAY Register Address = 0x04h

Bit	Name	Size	R/W	Default	Description
10-8	DECMOD	3	R/W	001	000: Force slow decay at all times *001: Slow decay for increasing current, mixed decay for decreasing current (indexer mode only)* 010: Force fast decay at all times 011: Use mixed decay at all times 100: Slow decay for increasing current, auto mixed decay for decreasing current (indexer mode only) 101: Use auto mixed decay at all times

8.2.2.5 Config Stall Detection

The best way to configure internal stall detect is by selecting a desired stall speed (in rpm). Set both SDTHR and VDIV to their minimum values. Next, decrease the motor speed to the desired stall detect speed. Use Equation 13 to determine the necessary stepping frequency:

$$f_{step}(steps/sec) = \frac{v(rpm) \times n_m(steps) \times 6}{\theta_{step}(^\circ/step)} \quad (13)$$

Now that the motor is spinning more slowly, increase SDTHR, or VDIV, or both SDTHR and VDIV until STALLn/BEMFn are asserted. Increasing either SDTHR or VDIV will make the stall detect trip at higher speeds. Set SDCNT so that the stall detect will trip after the desired number of steps.

CTRL Register Address = 0x00h

Bit	Name	Size	R/W	Default	Description
7	EXSTALL	1	R/W	0	*0: Internal stall detect* 1: External stall detect

TORQUE Register Address = 0x01h

Bit	Name	Size	R/W	Default	Description
10-8	SMPLTH	3	R/W	001	Back EMF sample threshold 000: 50 µs *001: 100 µs* 010: 200 µs 011: 300 µs 100: 400 µs 101: 600 µs 110: 800 µs 111: 1000 µs

STALL Register **Address = 0x05h**

Bit	Name	Size	R/W	Default	Description
7-0	SDTHR	8	R/W	0x40h	Sets stall detect threshold The correct setting needs to be determined experimentally
9-8	SDCNT	2	R/W	00	*00: STALLn asserted on first step with back EMF below SDTHR* 01: STALLn asserted after 2 steps 10: STALLn asserted after 4 steps 11: STALLn asserted after 8 steps
11-10	VDIV	2	R/W	00	*00: Back EMF is divided by 32* 01: Back EMF is divided by 16 10: Back EMF is divided by 8 11: Back EMF is divided by 4

8.2.2.6 Application Curves

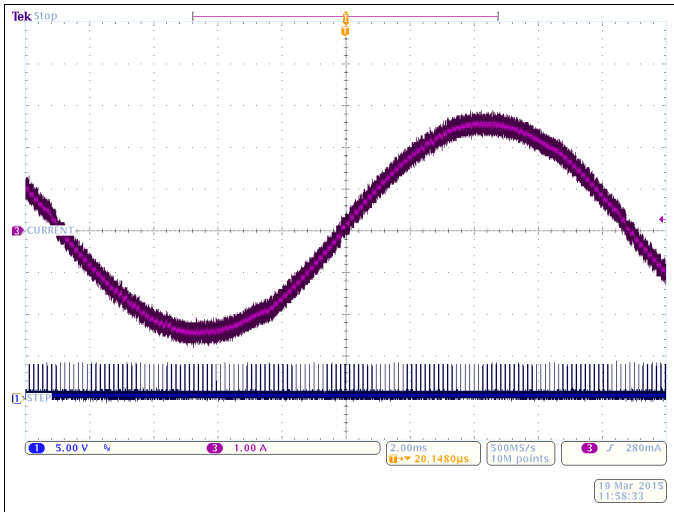


Figure 21. 1/32 Microstepping Drive Current

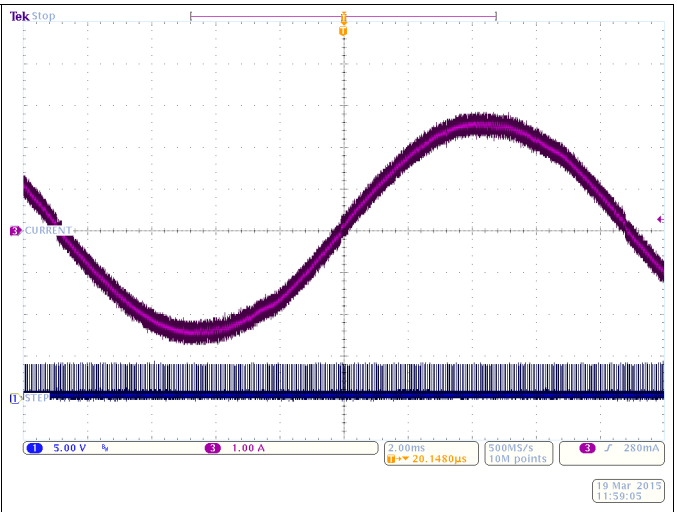


Figure 22. 1/64 Microstepping Drive Current

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The power supply's capacitance and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (Brushed DC, Brushless DC, Stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

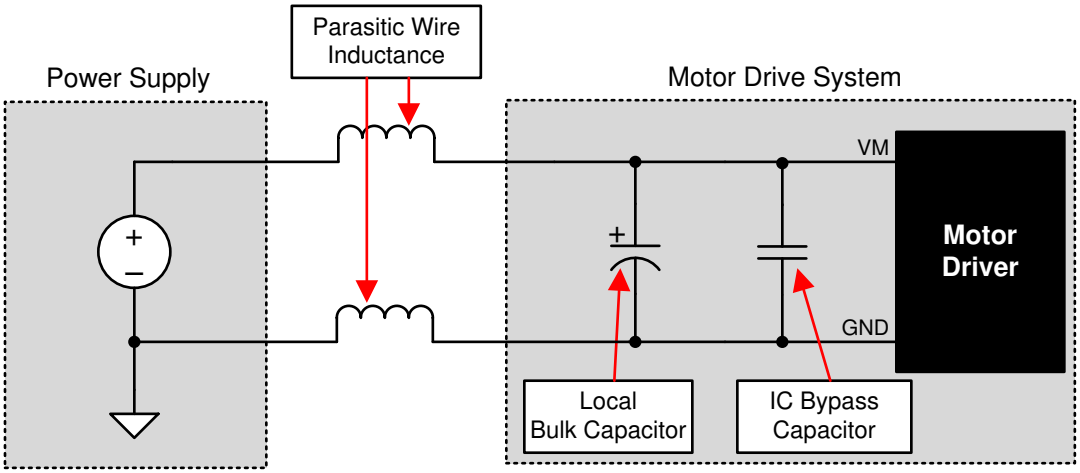


Figure 23. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

10 Layout

10.1 Layout Guidelines

The VM pin should be bypassed to GND using low-ESR ceramic bypass capacitors with a recommended value of 0.01-μF rated for VM. This capacitor should be placed as close to the VM pin as possible with a thick trace or ground plane connection to the device GND pin. The VM pin must be bypassed to ground using an appropriate bulk capacitor. This component may be an electrolytic and should be located close to the DRV8711.

A low-ESR ceramic capacitor must be placed in between the VM and VCP pins. TI recommends a value of 1 μF rated for 16 V. Place this component as close to the pins as possible.

A low-ESR ceramic capacitor must be placed in between the CP1 and CP2 pins. TI recommends a value of 0.1 μF rated for VM. Place this component as close to the pins as possible.

Bypass VINT to ground with a 1-μF ceramic capacitor rated 6.3 V. Place this bypass capacitor as close to the pin as possible.

Bypass V5 to ground with a 1-μF ceramic capacitor rated 10 V. Place this bypass capacitor as close to the pin as possible.

10.2 Layout Example

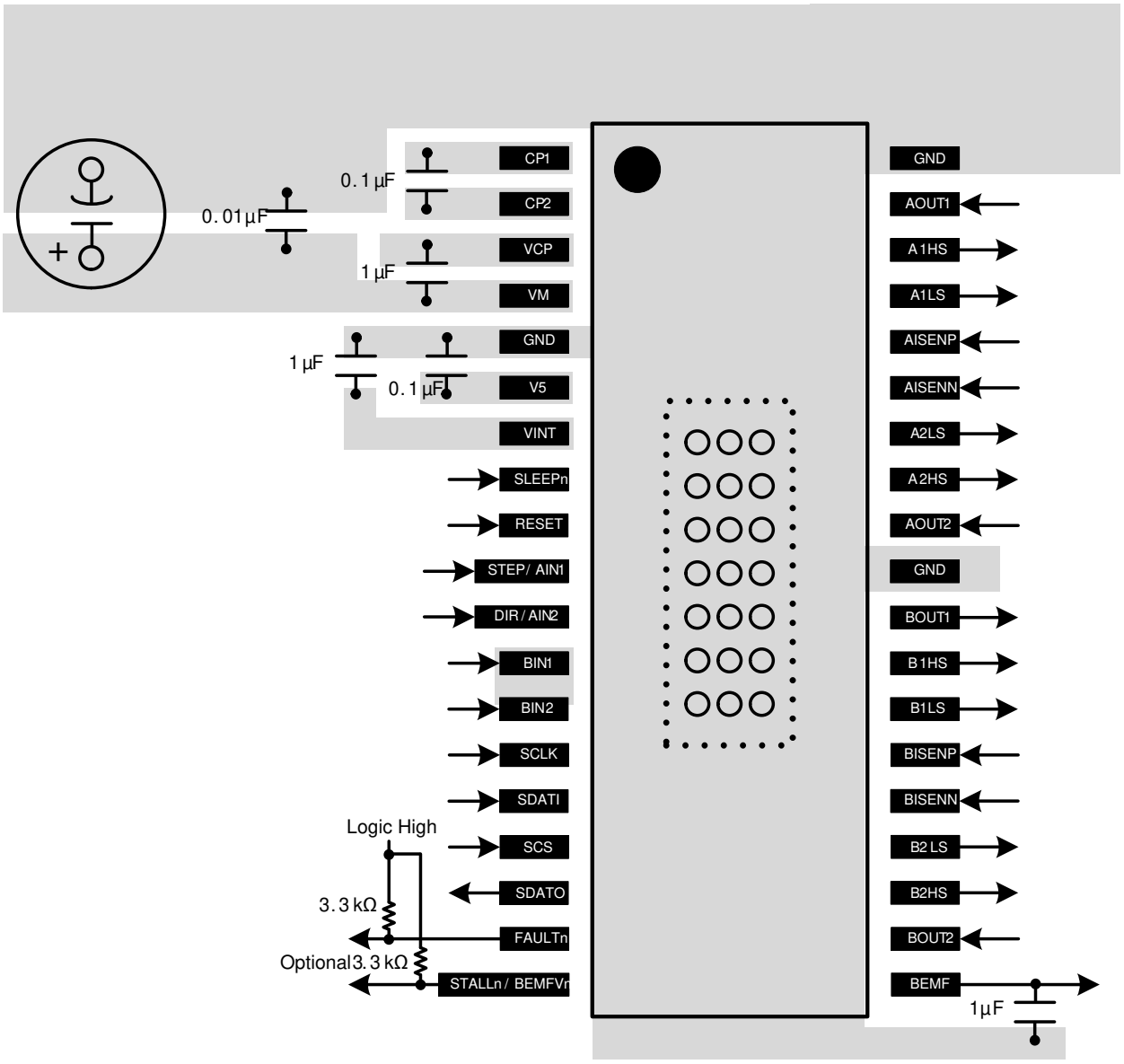


Figure 24. Recommended Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *DRV8711 Decay Mode Setting Optimization*
- *PowerPAD™ Thermally Enhanced Package*
- *PowerPAD™ Made Easy*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8711DCP	ACTIVE	HTSSOP	DCP	38	50	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8711	Samples
DRV8711DCPR	ACTIVE	HTSSOP	DCP	38	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	DRV8711	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

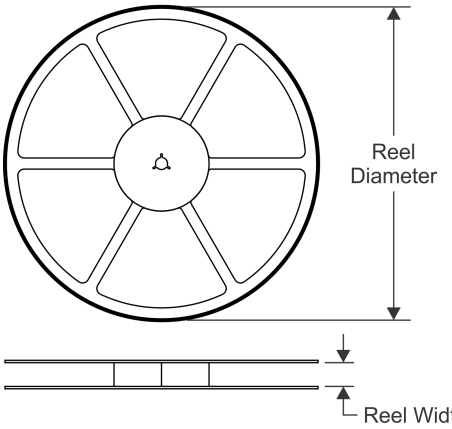
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

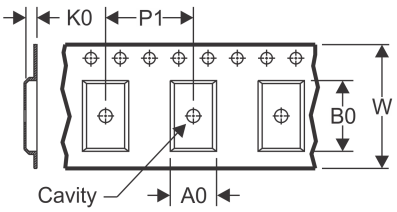
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

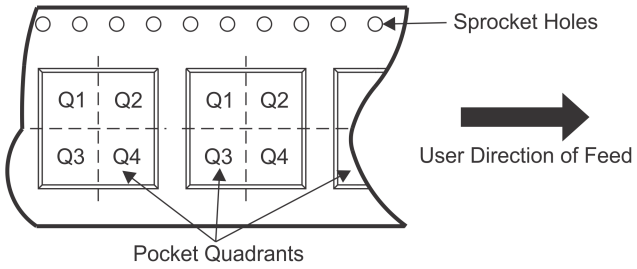


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

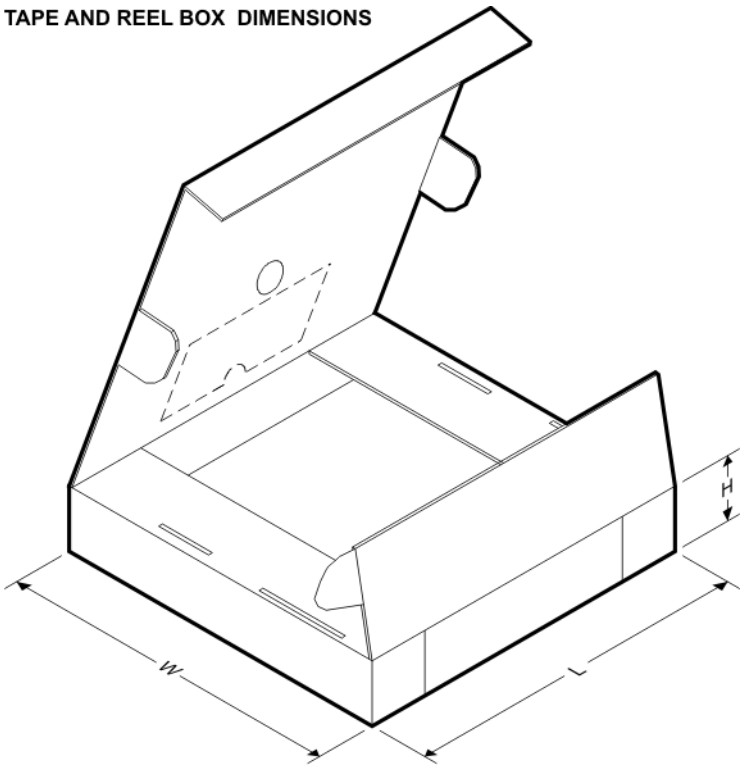
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8711DCPR	HTSSOP	DCP	38	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8711DCPR	HTSSOP	DCP	38	2000	350.0	350.0	43.0

GENERIC PACKAGE VIEW

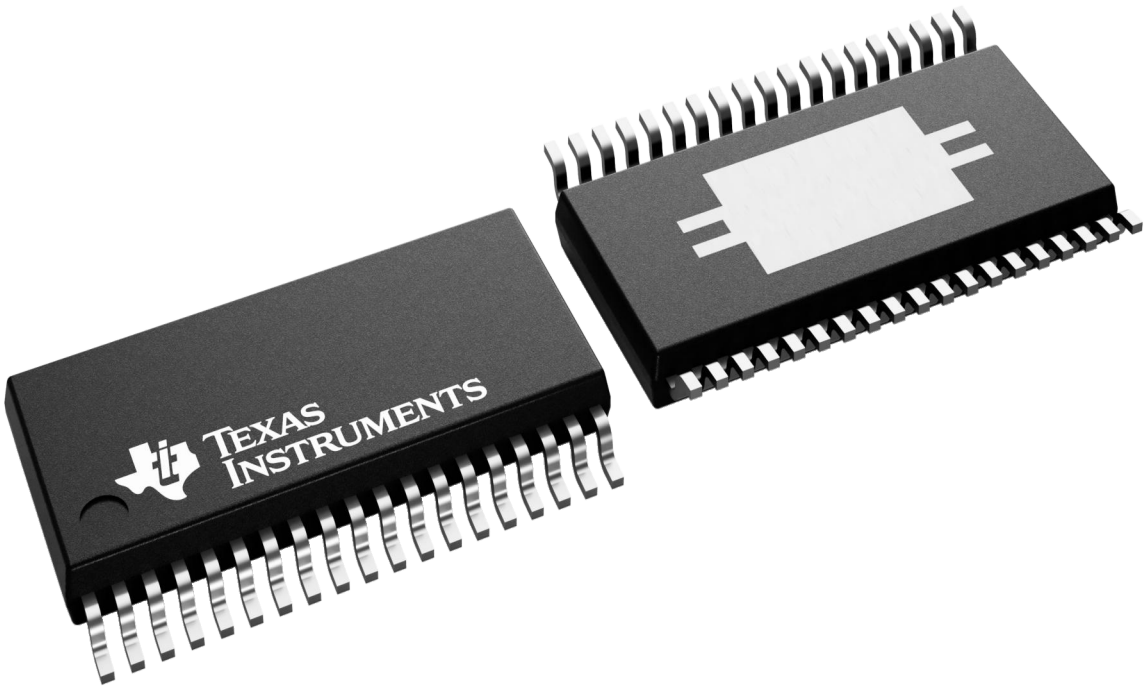
DCP 38

PowerPAD TSSOP - 1.2 mm max height

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

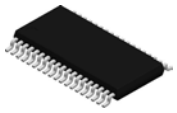
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224560/B

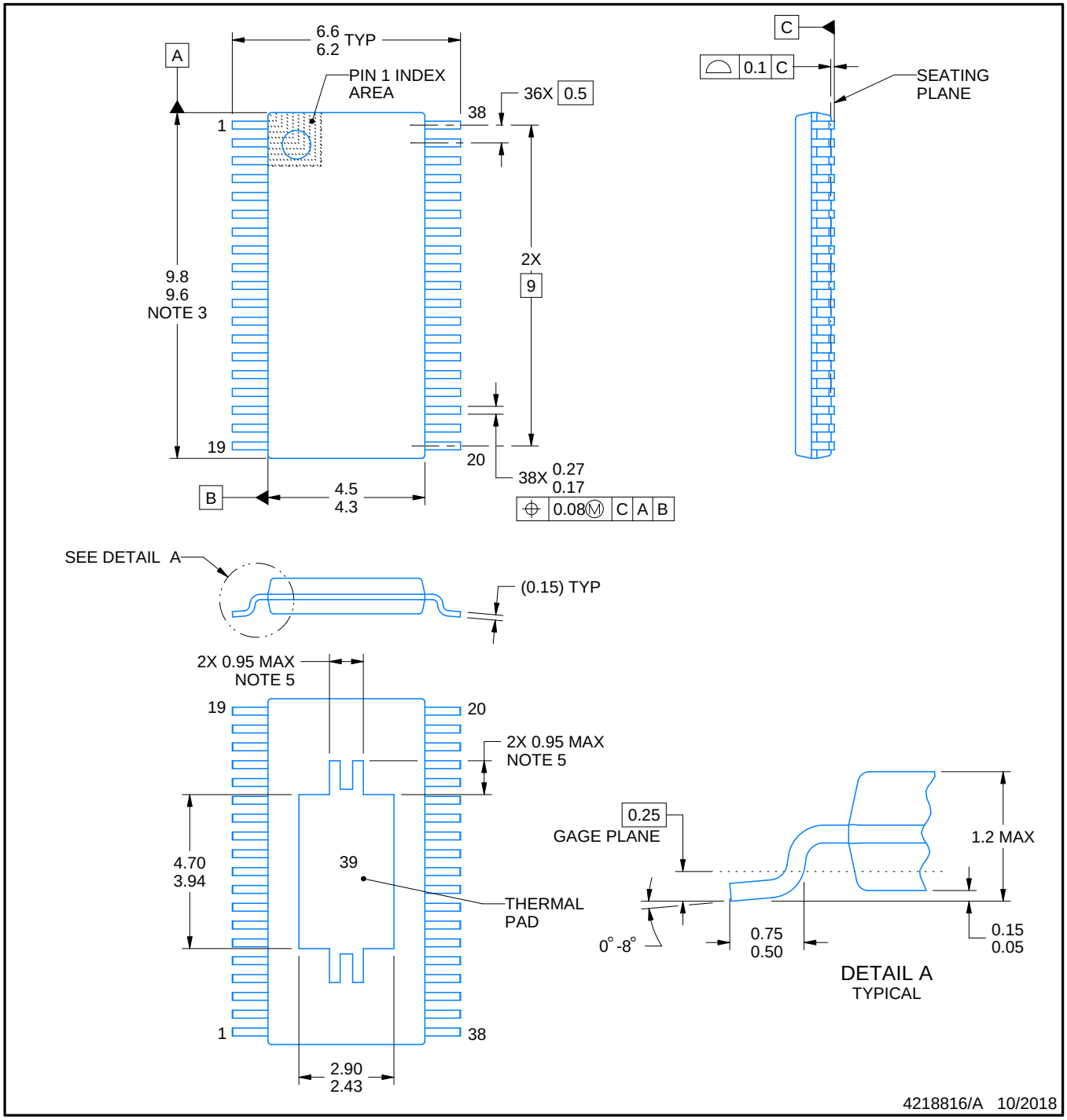
PACKAGE OUTLINE

DCP0038A



PowerPAD™ TSSOP - 1.2 mm max height

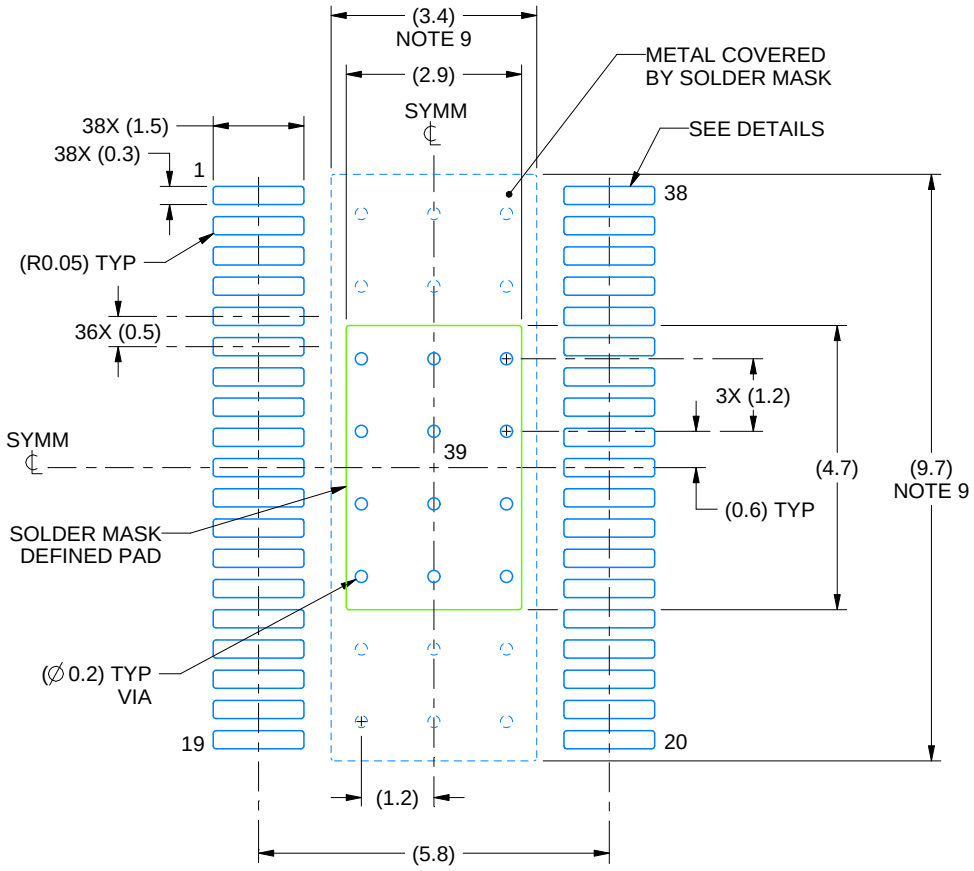
SMALL OUTLINE PACKAGE



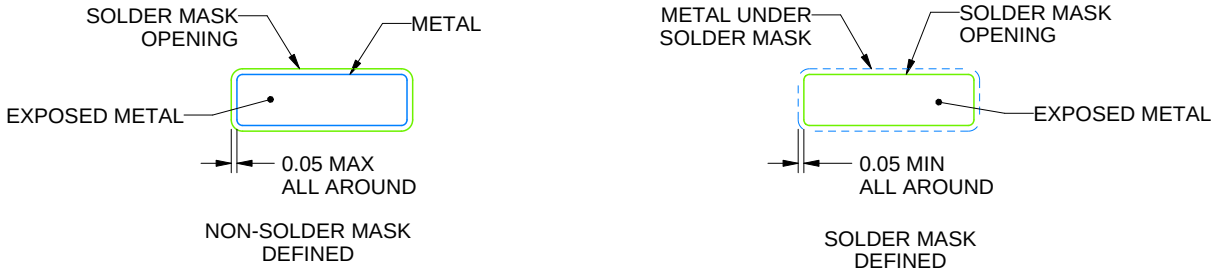
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

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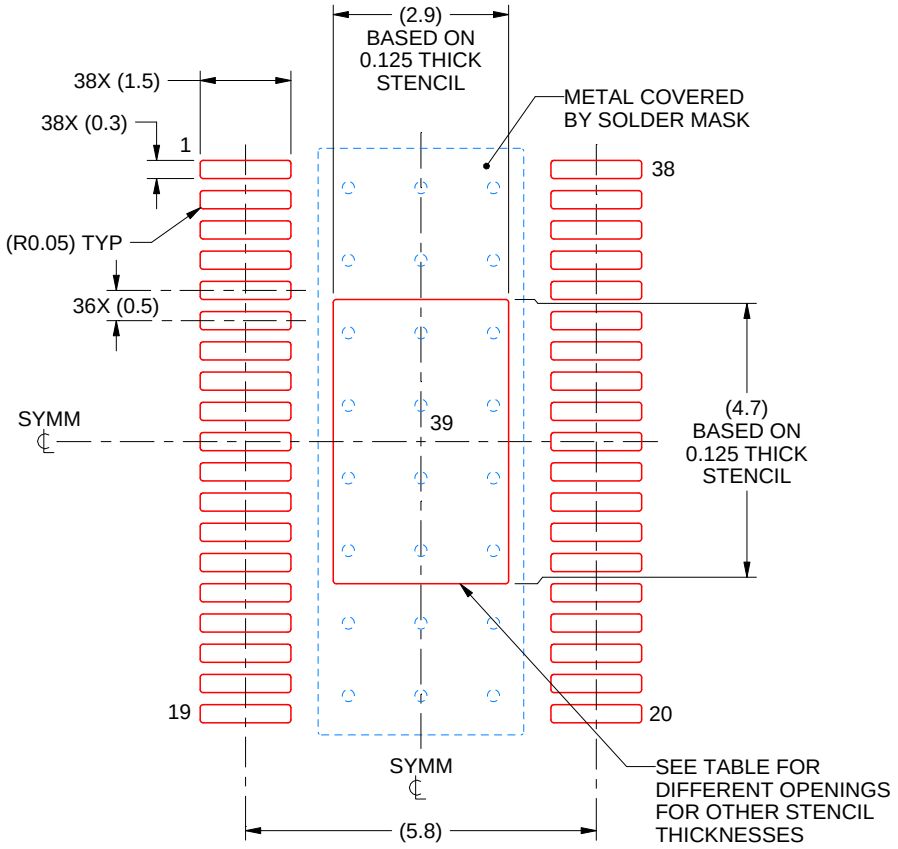
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.24 X 5.25
0.125	2.90 X 4.70 (SHOWN)
0.15	2.65 X 4.29
0.175	2.45 X 3.97

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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