MP2019

40V, 300mA, Low Quiescent Current Adjustable Output Linear Regulator

DESCRIPTION

The MP2019 is a low-power linear regulator that supplies power to systems with high-voltage batteries. It includes a wide 3V to 40V input range, low-dropout voltage, and a low quiescent-supply current. The low quiescent current and low dropout voltage allow operations at extremely low-power levels. Therefore, the MP2019 is ideal for low-power microcontrollers and battery-powered equipment.

The MP2019 provides a wide variety of fixed output-voltage options (if requested): 1.8V, 1.9V, 2.3V, 2.5V, 3.0V, 3.3V, 3.45V, and 5.0V; also, it provides the output-adjustable option (from 1.25V to 15V).

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions.

The MP2019 includes thermal shutdown (TSD), current-limiting fault protection, and is available in a SOIC-8 EP package.

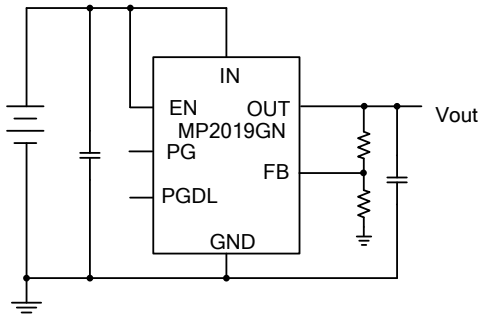
FEATURES

- 3V to 40V Input Range
- 10µA Quiescent Supply Current
- Stable with Low-Value Output Ceramic Capacitor (> 0.47µF)
- 300mA Specified Current
- Fixed 5V, 3.3V, and Adjustable Output (1.2 V to 15 V) Versions
- Output ±2% Accuracy Over Temperature
- Specified Current Limit
- Power Good
- Programmable Power Good Delay
- Thermal Shutdown and Short-Circuit Protection
- -40°C to +125°C Specified Junction-Temperature Range
- Available in a SOIC-8 EP Package

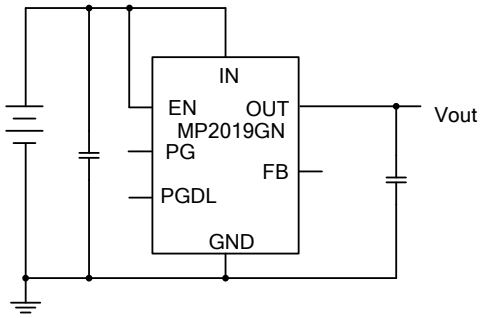
APPLICATIONS

- Industrial/Automotive Applications
- Portable/Battery-Powered Equipment
- Ultra-Low Power Microcontrollers
- Cellular Handsets
- Medical Imaging

TYPICAL APPLICATION



Output-Adjustable Version



Output-Fixed Version

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP2019GN	SOIC-8 EP	*See Below*
MP2019GN-33	SOIC-8 EP	
MP2019GN-5	SOIC-8 EP	

* For Tape & Reel, add suffix –Z (e.g. MP2019GN–Z);

TOP MARKING

MP2019
LLLLLLLL
MPSYWW

MP2019: part code of MP2019GN;
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

TOP MARKING

M2019-33
LLLLLLLL
MPSYWW

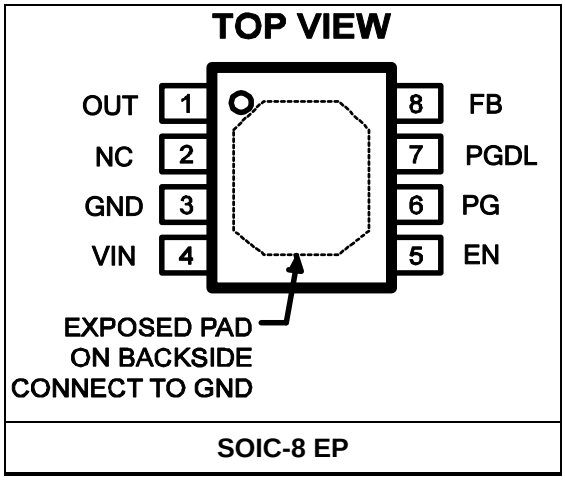
MP2019-33: part code of MP2019GN-33
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

TOP MARKING

MP2019-5
LLLLLLLL
MPSYWW

MP2019-5: part code of MP2019GN-5
LLLLLLLL: lot number;
MPS: MPS prefix:
Y: year code;
WW: week code:

PACKAGE REFERENCE



SOIC-8 EP

ABSOLUTE MAXIMUM RATINGS (1)

IN, EN ..... -0.3V to +42V
OUT ..... -0.3V to +17V
PG ..... -0.3V to +15V
PGDL, FB ..... -0.3V to +6V
Junction Temperature ..... +150°C
Lead Temperature ..... +260°C
Storage Temperature ..... -65°C to +150°C
Continuous Power Dissipation (T_A = +25°C) (2)
SOIC-8 EP 2.5W

ESD SUSCEPTIBILITY (3)

HBM (Human Body Mode) 4kV
MM (Machine Mode) 200V

Recommended Operating Conditions (4)

Supply Voltage V_{IN} ..... 3V to 40V
Output Voltage V_{OUT} ..... 1.25V to 15V
Operating Temperature ..... T_J=-40°C to +125°C

Thermal Resistance (5) θ_{JA} θ_{JC}

SOIC-8 EP ..... 50 ..... 10 ... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation produces an excessive die temperature, causing the regulator to go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) Devices are ESD sensitive. Handle with precaution.
4) The device is not guaranteed to function outside of its operating conditions.
5) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN} = V_{EN} = 13.5V, T_J =+25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Input Voltage	V_{IN}			3		40	V
Output-Voltage Range	V_{OUT}			1.25		15	V
GND Current	I_{GND}	MP2019GN	0<I_{LOAD}<1mA		10	15	µA
			1mA<I_{LOAD}<30mA		15	21	
			30mA<I_{LOAD}<300mA		65	95	
		MP2019GN-33	0<I_{LOAD}<1mA		12	16	µA
			1mA<I_{LOAD}<30mA		16	22	
			30mA<I_{LOAD}<300mA		65	95	
		MP2019GN-5	0<I_{LOAD}<1mA		12	16	µA
			1mA<I_{LOAD}<30mA		16	22	
			30mA<I_{LOAD}<300mA		65	95	
Shutdown Supply Current	I_S	V_{EN} =0V				1	µA
Load Current Limit	I_{LIMIT}	V_{IN}=7V, V_{OUT} = 0V		600	1000	1350	mA
FB Voltage	V_{FB}	MP2019GN, FB = OUT, I_{LOAD}=5mA		1.225	1.25	1.275	V
Output Voltage Accuracy		MP2019GN-33, I_{LOAD}=5mA		3.2	3.3	3.4	V
		MP2019GN-5, I_{LOAD}=5mA		4.85	5	5.15	
Dropout Voltage[6]	$V_{DROPOUT}$	MP2019GN	V_{OUT}=5V, I_{LOAD} = 150mA		200	400	mV
			V_{OUT}=5V, I_{LOAD} = 300mA		420	550	
		MP2019GN-33	V_{OUT}=3.3V, I_{LOAD} = 150mA		230	430	
			V_{OUT}=3.3V, I_{LOAD} = 300mA		480	640	
		MP2019GN-5	V_{OUT}=5V, I_{LOAD} = 150mA		230	430	
			V_{OUT}=5V, I_{LOAD} = 300mA		480	640	
FB Input Current	I_{FB}	MP2019GN	V_{FB} = 1.3V			50	nA
Line Regulation		MP2019GN	V_{IN} = 3V to 40V, I_{LOAD} = 5mA, V_{OUT} = V_{FB}	-10	1	10	mV
		MP2019GN-33	V_{IN} = 5V to 40V, I_{LOAD} = 5mA, V_{OUT} = 3.3V	-10	1	10	
		MP2019GN-5	V_{IN} = 6V to 40V, I_{LOAD} = 5mA, V_{OUT} = 6V	-10	1	10	

ELECTRICAL CHARACTERISTICS *(continued)*

V_{IN} = V_{EN} = 13.5V, T_J =+25°C, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Units
Load Regulation		MP2019GN	I_{LOAD} = 5mA to 300mA, V_{OUT} = 5V		1	15	mV
		MP2019GN-33	I_{LOAD} = 5mA to 300mA, V_{OUT} = 3.3V		1	15	
		MP2019GN-5	I_{LOAD} = 5mA to 300mA, V_{OUT} = 5V		1	15	
Output Voltage PSRR(7)		100Hz, C_{OUT} = 10µF, I_{LOAD}=10mA			57		dB
		1kHz, C_{OUT} = 10µF, I_{LOAD}=10mA			45		dB
		100kHz, C_{OUT} = 10µF, I_{LOAD}=10mA			51		dB
Start-Up Response Time		MP2019GN	R_{LOAD}=500Ω, V_{OUT} = 5V, C_{OUT}=22µF, V_{OUT} from 10% to 90%		0.9	1.5	ms
		MP2019GN-33	R_{LOAD}=500Ω,V_{OUT}=3.3V, C_{OUT}=22µF, V_{OUT} from 10% to 90%		0.5	1	
		MP2019GN-5	R_{LOAD}=500Ω,V_{OUT}=5V, C_{OUT}=22µF, V_{OUT} from 10% to 90%		0.9	1.5	
EN Threshold Voltage	V_{IL}					0.3	V
	V_{IH}			1.8			V
EN Input Current		EN = 0V or 15V			0.1	0.5	µA
PG Rising Threshold		MP2019GN		89%	93%	97%	V_{FB}
		MP2019GN-33		88%	92%	96%	
		MP2019GN-5		88%	92%	96%	
PG Rising Threshold Hysteresis					5%		V_{FB}
PG Low Voltage		Sink 1mA Current			0.1	0.4	V
PG Leakage Current		V_{PG}=5V				1	µA
PGDL Charging Current		V_{PGDL}=1V		3	5.5	9	µA
PGDL Rising Threshold				1.4	1.7	2	V
PGDL Falling Threshold				0.2	0.4	0.7	V
PG Delay Time		C_{PGDL}=47nF		5	10	15	ms
PG Reaction Time		C_{PGDL}=47nF			0.5	2	µs
Thermal Shutdown(7)	T_{SD}				165		°C
Thermal Shutdown Hysteresis(7)	ΔTSD				30		°C

Notes:

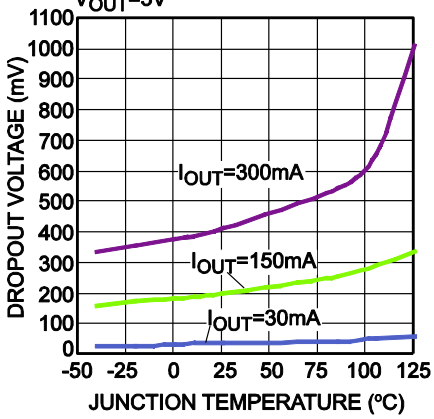
6) Dropout Voltage: Measured when the output voltage VOUT has dropped 100mV from the nominal value obtained at VIN=13.5V.
7) Derived from bench characterization. Not tested in production.

PIN FUNCTIONS

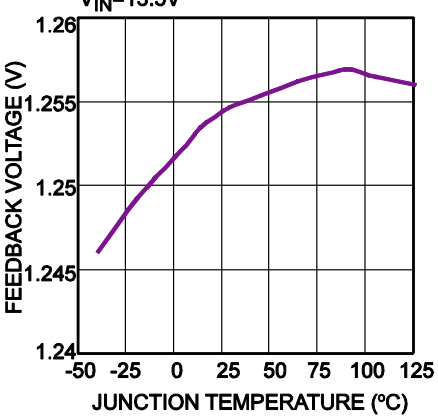
Pin #	Name	Description
1	OUT	Regulated Output Voltage. Only a low-value ceramic capacitor (≥ 0.47μF) on the output is required for stability.
2	NC	No Connection. Do NOT connect.
3	GND	Ground. Connect the exposed pad and GND to the same ground plane.
4	VIN	Input Voltage. Connect a 3V to 40V supply to VIN.
5	EN	Regulator On/Off Control Input. Logic low shuts down the IC; logic high starts up the IC. Connect EN to VIN for automatic start-up.
6	PG	Power Good. If not used, pin can be left floating.
7	PGDL	Programmable Power-Good Delay Time. If not used, pin can be left floating.
8	FB	Feedback Input for Output Adjustable Version. FB is regulated to 1.25V nominally. This terminal is used to set the output voltage.

TYPICAL PERFORMANCE CHARACTERISTICS

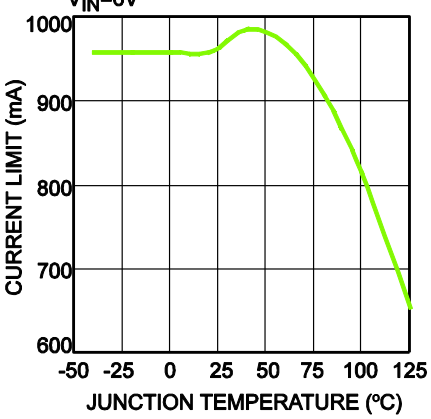
Dropout Voltage vs. Junction Temperature



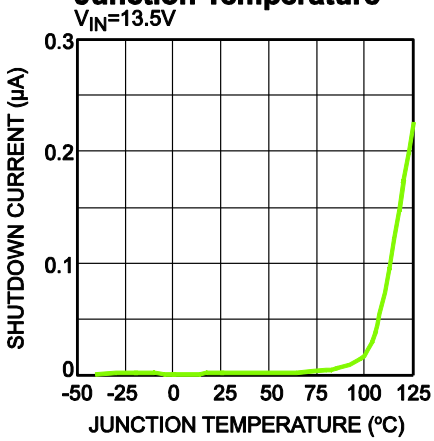
Feedback Voltage vs. Junction Temperature



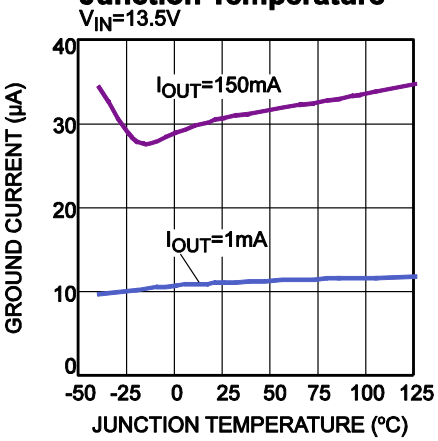
Current Limit vs. Junction Temperature



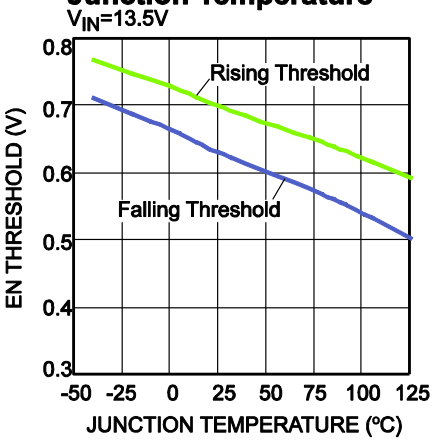
Shutdown Current vs. Junction Temperature



GND Current vs. Junction Temperature



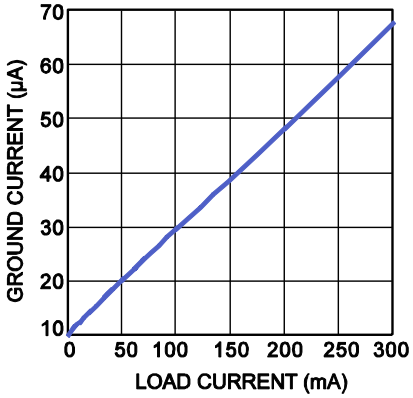
EN Threshold vs. Junction Temperature



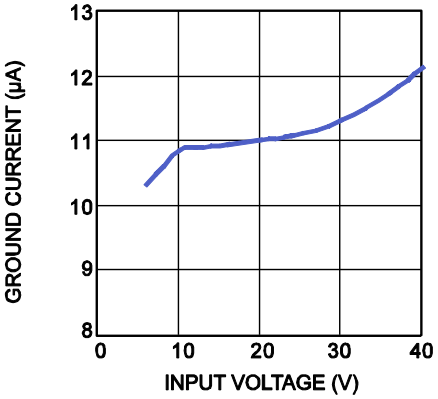
TYPICAL PERFORMANCE CHARACTERISTICS

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

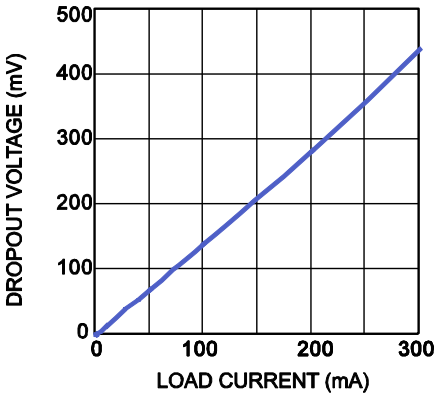
Ground Current vs. Load Current
V_{IN}=6V



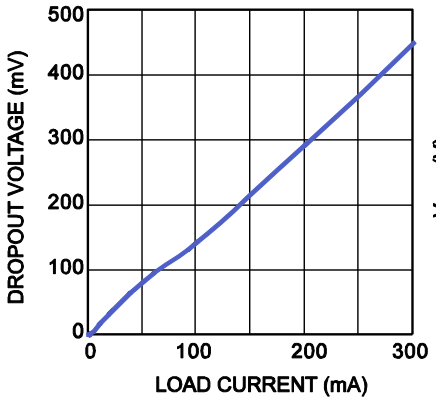
Ground Current vs. V_{IN}
I_{OUT}=0mA



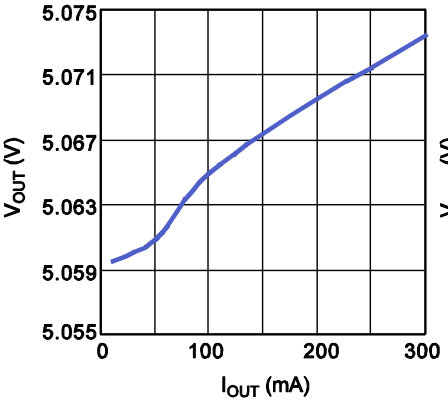
Dropout Voltage vs. Load Current
V_{OUT}=3.3V



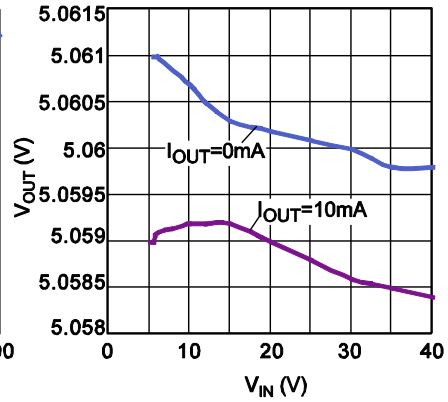
Dropout Voltage vs. Load Current



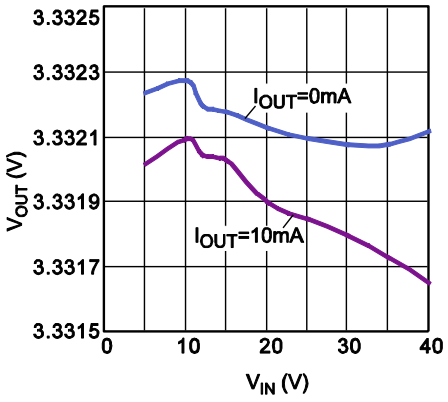
V_{OUT} vs. I_{OUT}
V_{IN}=6V



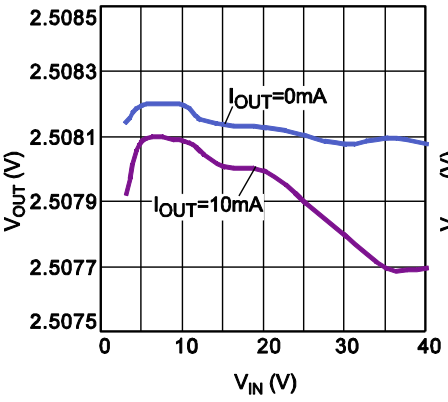
V_{OUT} vs. V_{IN}



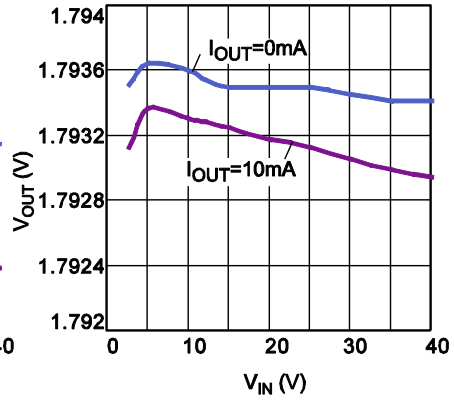
V_{OUT} vs. V_{IN}
V_{OUT}=3.3V



V_{OUT} vs. V_{IN}
V_{OUT}=2.5V



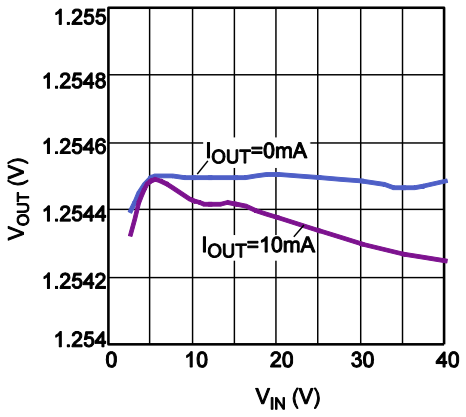
V_{OUT} vs. V_{IN}
V_{OUT}=1.8V



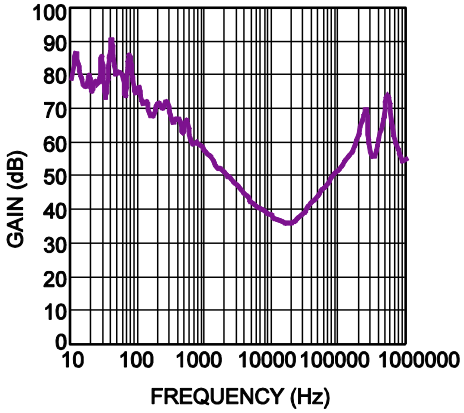
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

V_{OUT} vs. V_{IN}
V_{OUT}=1.25V



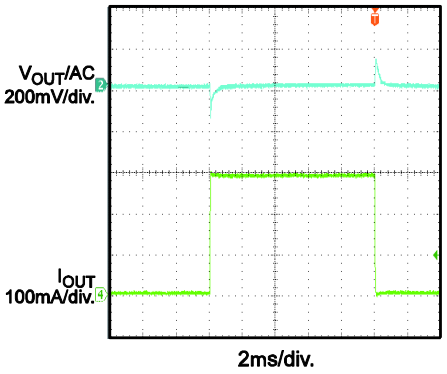
PSRR vs. Frequency



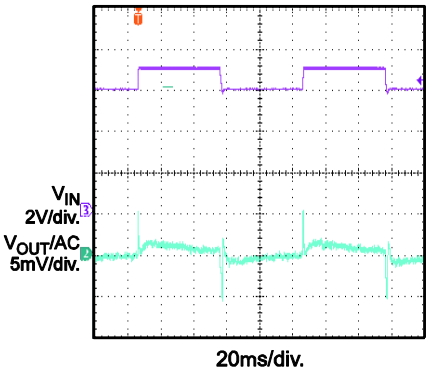
TYPICAL PERFORMANCE CHARACTERISTICS *(continued)*

C_{IN} = 1µF, C_{OUT} = 22µF, V_{OUT} = 5V, T_A = 25°C, unless otherwise noted.

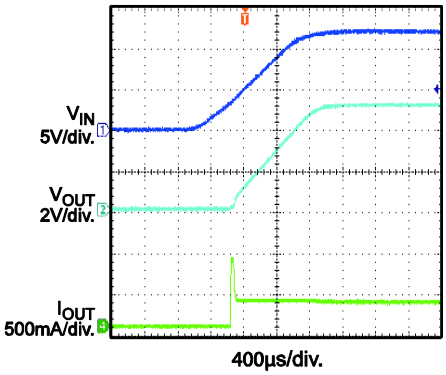
Load Transient
V_{IN} = 12V, I_{OUT} = 300mA



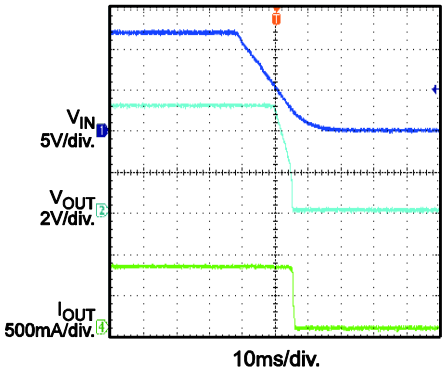
Line Transient
V_{IN} = 6V-7V, I_{OUT} = 300mA



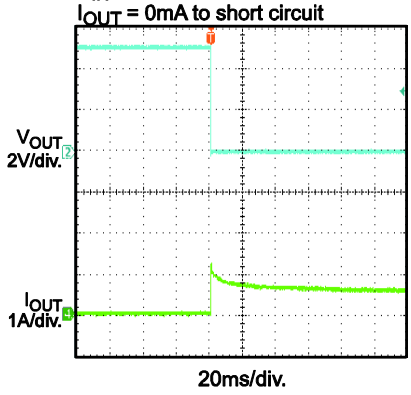
Start-Up through V_{IN}
V_{IN} = 12V, I_{OUT} = 300mA



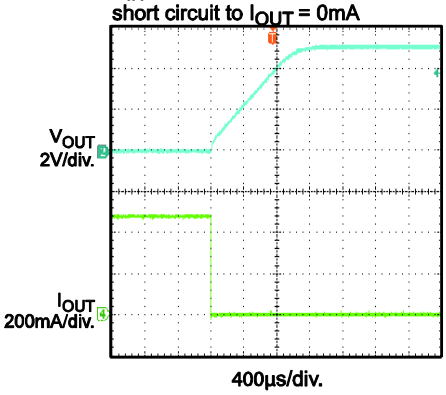
Shutdown through V_{IN}
V_{IN} = 12V, I_{OUT} = 300mA



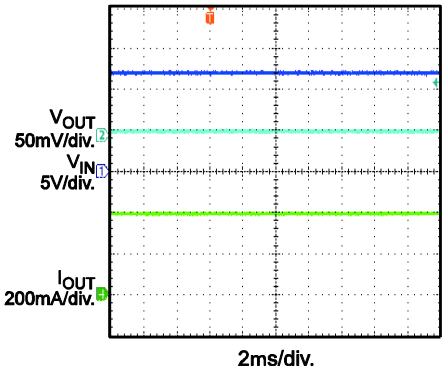
Short-Circuit Entry
V_{IN} = 12V,
I_{OUT} = 0mA to short circuit



Short-Circuit Recovery
V_{IN} = 12V,
short circuit to I_{OUT} = 0mA



Short-Circuit Steady State
V_{IN} = 12V



OPERATION

The MP2019 is a linear regulator that supplies power to systems with high-voltage batteries. It includes a wide 3V to 40V input range, low dropout voltage, and a low quiescent-supply current (see Fig. 1).

The MP2019 provides a wide variety of fixed output-voltage options: 1.8V, 1.9V, 2.3V, 2.5V, 3.0V, 3.3V, 3.45V, and 5.0V; also, it provides the output-adjustable option (from 1.25V to 15V).

The output-adjustable version has an output that is adjustable from 1.25V to 15V with a simple resistor divider. It uses external feedback, allowing the user to set the output voltage with an external resistor divider. The FB threshold is 1.25V, typically.

The IC enters shutdown mode when EN is low. In shutdown mode, the pass transistor, control circuitry, reference, and all biases turn off; this reduces the supply current to <1μA. Connect EN to VIN for automatic start-up.

The regulator output current is limited internally, and the device is protected against short-circuit, over-load, and over-temperature conditions (see Fig. 2).

The peak output current is limited to around 1000mA, which exceeds the 300mA recommended continuous output current.

When the junction temperature is too high, the thermal sensor sends a signal to the control logic which shuts down the IC. The IC will re-start when the temperature has cooled sufficiently.

The maximum power output current is a function of the package's maximum power dissipation for a given temperature.

The maximum power dissipation is dependent on the thermal resistance of the case and the circuit board, the temperature difference between the die junction and the ambient air, and the rate of air flow. GND and the exposed pad must be connected to the ground plane for proper dissipation.

MP2019 has one power good (PG) pin. The PG pin is the open drain of an internal MOSFET. It should be connected to V_{OUT} or external voltage source(<15V) through a resistor (i.e. 100kohm). After the V_{FB} reaches 93% of nominal value, the MOSFET turns off and PG pin is pulled to high by V_{OUT} or external voltage source. When the V_{FB} drops to 88% of nominal value, the PG voltage is pulled to GND.

There is a delay time when PG asserts high. The delay time can be programmed by adding a capacitor on PGDL. To select a capacitor for PGDL, use below equation:

$$C_{PGDL}(nF) = \frac{t_{PGDL}(ms) \times I_{PGDL}(\mu A)}{V_{th\_PGDL}(V)}$$

Where t_{PGDL} is the desired delay time for PG asserts high, I_{PGDL} is the PGDL charging current and V_{th_PGDL} is 1.7V.

Figure 2 shows the power good timing.

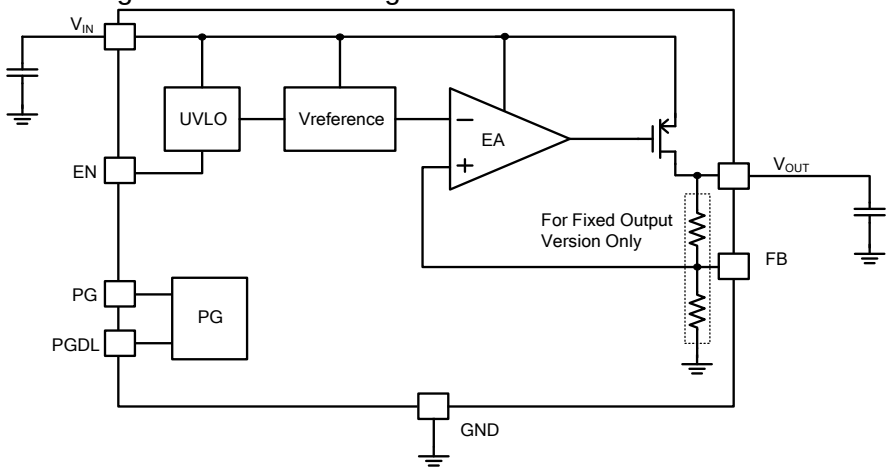


Figure 1. Functional Block Diagram

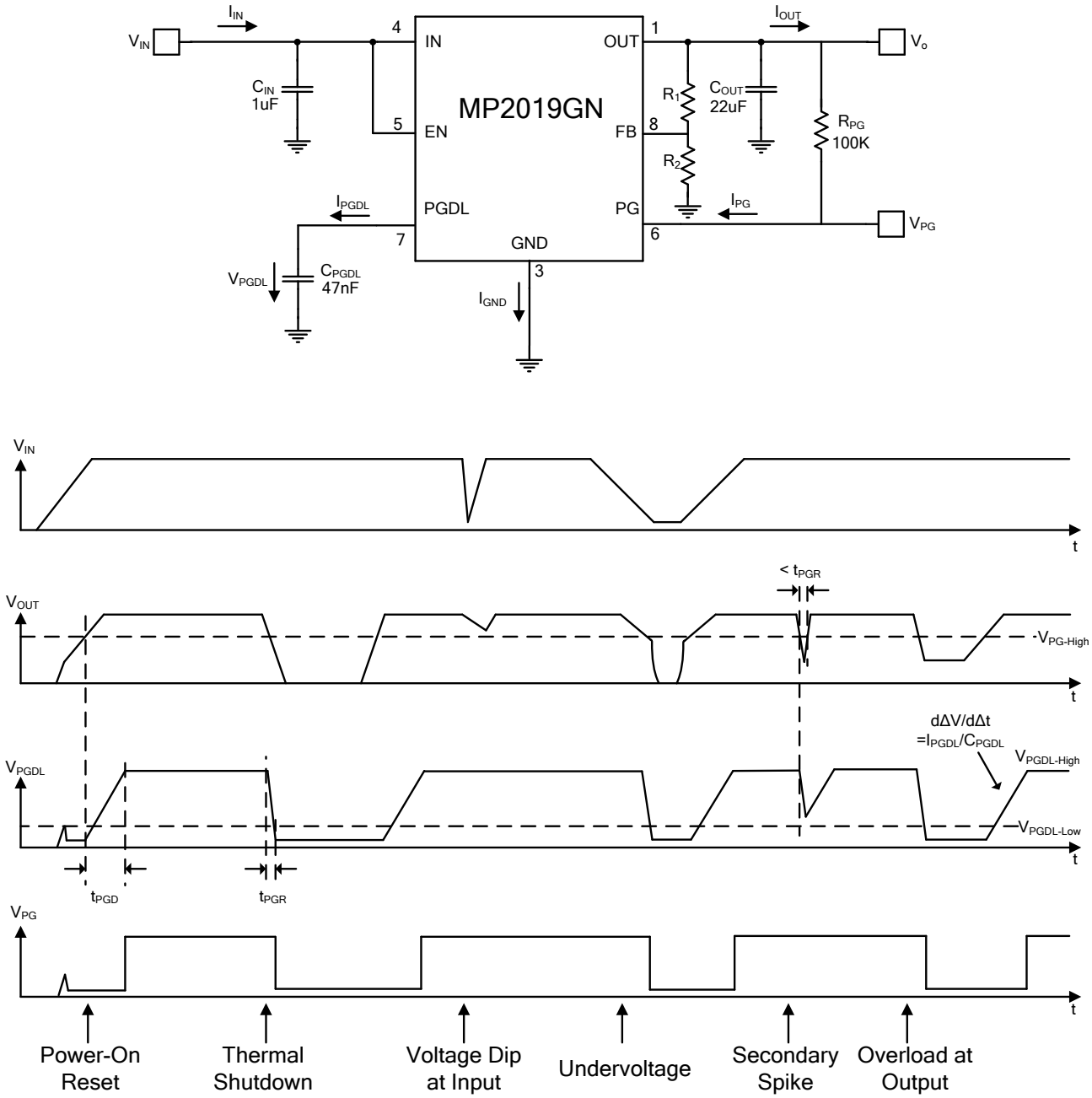


Figure 2. Power Good Timing

APPLICATION INFORMATION

COMPONENT SELECTION

Setting the Output Voltage

Set the output voltage of the MP2019 by using a resistor divider (see Fig. 3).

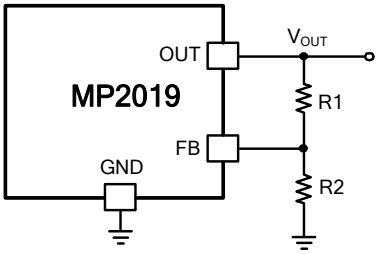


Figure 3. FB Resistor Divider to Set V_{OUT}

Choose R2=1MΩ to maintain a 1.215μA minimum load. Calculate the value for R1 using the following equation:

$$R1 = R2 \times \left(\frac{V_{OUT}}{1.25V} - 1 \right)$$

For a fixed-output version, VOUT can be adjusted by adding an external resistor divider (see Fig. 4). When choosing an external divider, take the internal FB resistor divider into consideration.

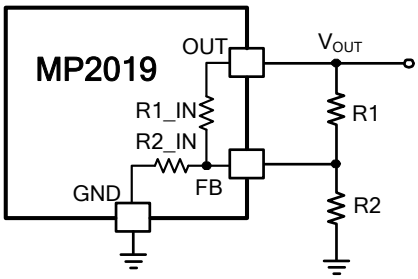


Figure 4. FB Divider for Fixed-Output Version

When R2 is selected, R1 can be calculated with the equation below:

$$R1 = \frac{R1\_IN}{\frac{1.25 \times R1\_IN \times (R2 + R2\_IN)}{(V_{OUT} - 1.25) \times R2 \times R2\_IN} - 1}$$

Table 1 below shows the internal FB resistor dividers for different fixed-output versions.

Table 1. Internal FB Resistor Divider

Fixed-Output Voltage	R1_IN	R2_IN
3.3V	1.64MΩ	1MΩ
5V	3MΩ	1MΩ

Table 2 below shows various output voltages for a fixed-output version with an external FB divider..

Table 2. 3.3V Fixed-Output Version with External FB Divider

V_{OUT}(V)	R1 (kΩ)	R2 (kΩ)
11	80.6	10
8.5	59	10
8	54.9	10
6.5	43	10
5	30.1	10

Enable Control (EA)

EN is a digital control pin that turns the regulator on and off. When EN is pulled below 0.3V, the chip shuts down. When EN is pulled above 1.8V, the chip starts up. If this function is not used, EN can be connected to VIN directly.

Input Capacitor

For efficient operation, place a ceramic capacitor, (C1) between 1μF and 10μF of dielectric type (X5R or X7R) between the input pin and ground. Larger values in this range improve line transient response.

Output Capacitor

For stable operation, use a ceramic capacitor (C2) of type X5R or X7R between 1μF and 22μF. Larger values in this range improve load transient response and reduce noise. Output capacitors of other dielectric types may be used, but they are not recommended as their capacitance can deviate greatly from their rated value over temperature.

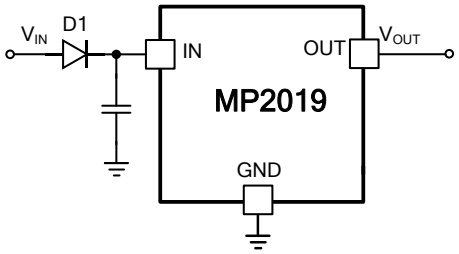
To improve load transient response, add a small ceramic (X5R, X7R, or Y5V dielectric) 2.2nF feed-forward capacitor in parallel with R1. The feed-forward capacitor is not required for stable operation.

Output Noise

The MP2019 exhibits noise on the output during normal operation. This noise is negligible for most applications. However, in applications that include analog-to-digital converters (ADCs) of more than 12 bits, consider the ADC's power supply rejection specifications. The feed-forward capacitor C2 across R1 reduces significantly the output noise.

External Reverse Voltage Protection

In some situations, e.g. a backup battery is connected as MP2019 load, the output voltage may be held up while the input is either pulled to ground, pulled to some intermediate voltage or is floating. Thus, the output voltage is higher than input voltage. Since the MP2019 PMOS pass element has a body diode, a current will conduct from the output to input and is not internally limited. It's possible that the IC will be damaged by this unlimited reverse current. To avoid this, it's recommended to place an external diode at input like below.

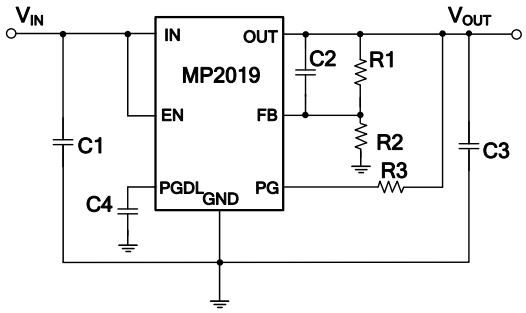


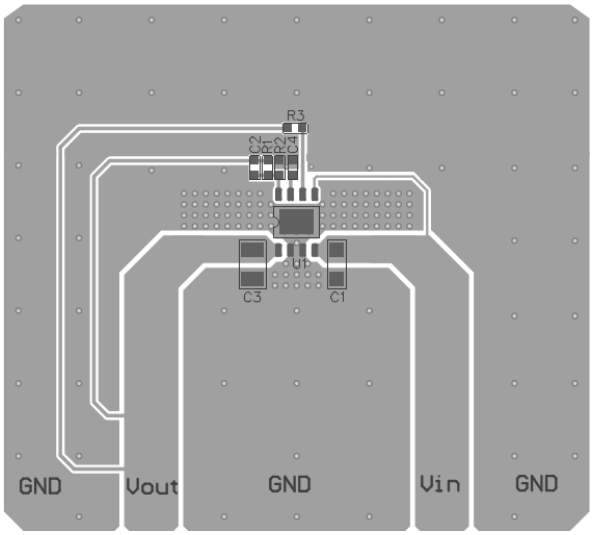
PCB Layout Guidelines

Efficient PCB layout is critical to achieve good regulation, ripple rejection, transient response, and thermal performance. It is recommended highly to duplicate the EVB layout for optimum performance.

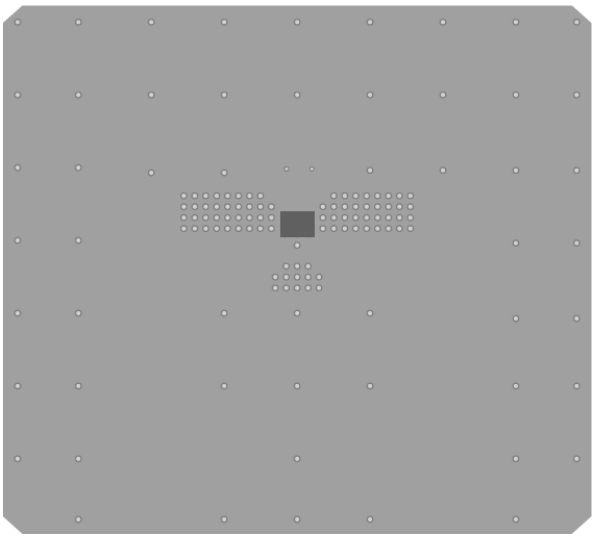
If changes are necessary, refer to Fig. 5 and follow the guidelines below:

1) Place input and output bypass ceramic capacitors close to IN and OUT, respectively.
2) Ensure all feedback connections are short and direct. Place the feedback resistors and compensation components as close to the chip as possible.
3) Connect IN, OUT, and especially, GND, respectively, to a large copper area to cool the chip. This improves thermal performance and long-term reliability.





Top Layer



Bottom Layer

Figure 5. Recommended PCB Layout

DESIGN EXAMPLE

Fig. 6 is a design example following the application guidelines for V_{OUT}=3.3V with a feed-forward cap:

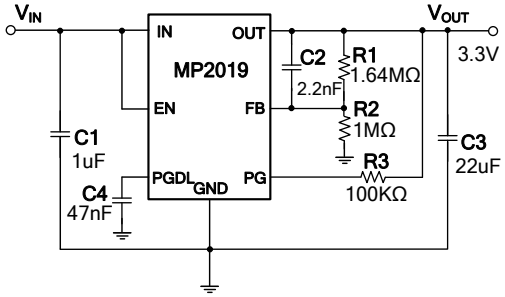


Figure 6. Design Example

TYPICAL APPLICATION CIRCUITS

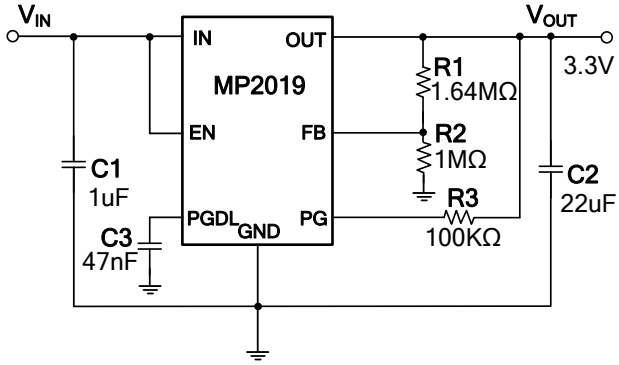


Figure 7. 3.3V Output Typical Application Circuit

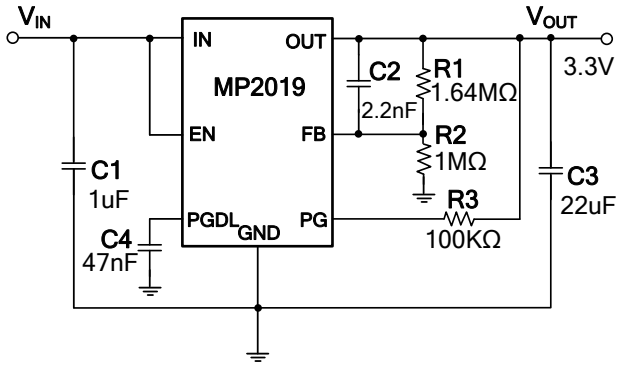
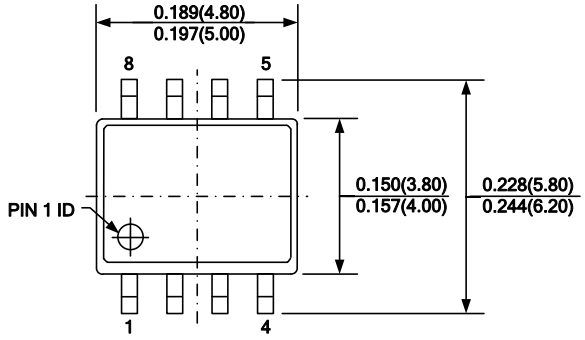


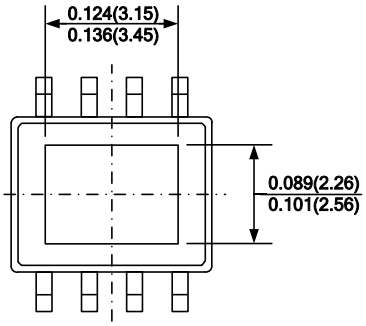
Figure 8. 3.3V Output with Feed-Forward Capacitor

PACKAGE INFORMATION

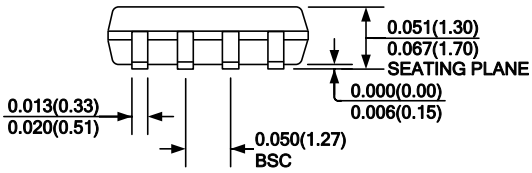
SOIC-8 EP



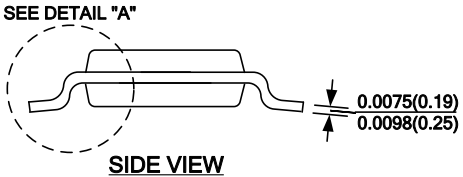
TOP VIEW



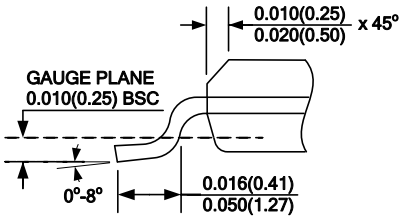
BOTTOM VIEW



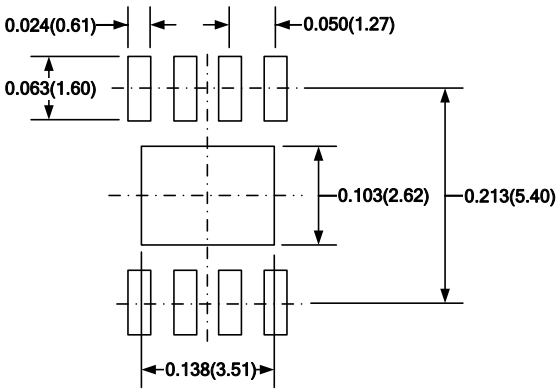
FRONT VIEW



SIDE VIEW



DETAIL "A"



RECOMMENDED LAND PATTERN

NOTE:

1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKETS IS IN MILLIMETERS.
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
6) DRAWING IS NOT TO SCALE.