PCF8579

LCD column driver for dot matrix graphic displays

Rev. 05 — 11 May 2009   **Product data sheet**

1. General description

The PCF8579 is a low power CMOS[1] LCD column driver, designed to drive dot matrix graphic displays at multiplex rates of 1:8, 1:16, 1:24 or 1:32. The device has 40 outputs and can drive 32×40 dots in a 32 row multiplexed LCD. Up to 16 PCF8579s can be cascaded and up to 32 devices may be used on the same I²C-bus (using the two slave addresses). The device is optimized for use with the PCF8578 LCD row/column driver. Together these devices form a general purpose LCD dot matrix driver chip set, capable of driving displays of up to 40960 dots. The PCF8579 is compatible with most microcontrollers and communicates via a two-line bidirectional bus (I²C-bus). To allow partial V_{DD} shutdown the ESD protection system of the SCL and SDA pins does not use a diode connected to V_{DD}. Communication overhead is minimized by a display RAM with auto-incremented addressing and display bank switching.

2. Features

- LCD column driver
- Used in conjunction with the PCF8578, this device forms part of a chip set capable of driving up to 40960 dots
- 40 column outputs
- Selectable multiplex rates; 1:8, 1:16, 1:24 or 1:32
- Externally selectable bias configuration, 5 or 6 levels
- Easily cascadable for large applications (up to 32 devices)
- 1280-bit RAM for display data storage
- Display memory bank switching
- Auto-incremented data loading across hardware subaddress boundaries (with PCF8578)
- Power-On Reset (POR) blanks display
- Logic voltage supply range 2.5 V to 6 V
- Maximum LCD supply voltage 9 V
- Low power consumption
- I²C-bus interface
- Compatible with most microcontrollers
- Optimized pinning for single plane wiring in multiple device applications (with PCF8578)
- Space saving 56-lead small outline package and 64-pin quad flat pack

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 15.

3. Applications

■ Automotive information systems
■ Telecommunication systems
■ Point-of-sale terminals
■ Industrial computer terminals
■ Instrumentation

4. Ordering information

Table 1. Ordering information

Type number	Package			Version
	Name	**Description**		
PCF8579T/1	VSO56	plastic very small outline package; 56 leads		SOT190-1
PCF8579H/1	LQFP64	plastic low profile quad flat package; 64 leads; body $10 \times 10 \times 1.4$ mm[1]		SOT314-2
PCF8579HT/1	TQFP64	plastic thin quad flat package; 64 leads; body $10 \times 10 \times 1.0$ mm		SOT357-1

[1] Should not be used for new designs.

5. Marking

Table 2. Marking codes

Type number	Marking code
PCF8579T/1	PCF8579T
PCF8579H/1	PCF8579H
PCF8579HT/1	PCF8579HT

PCF8579_5

Product data sheet **Rev. 05 — 11 May 2009** 2 of 41
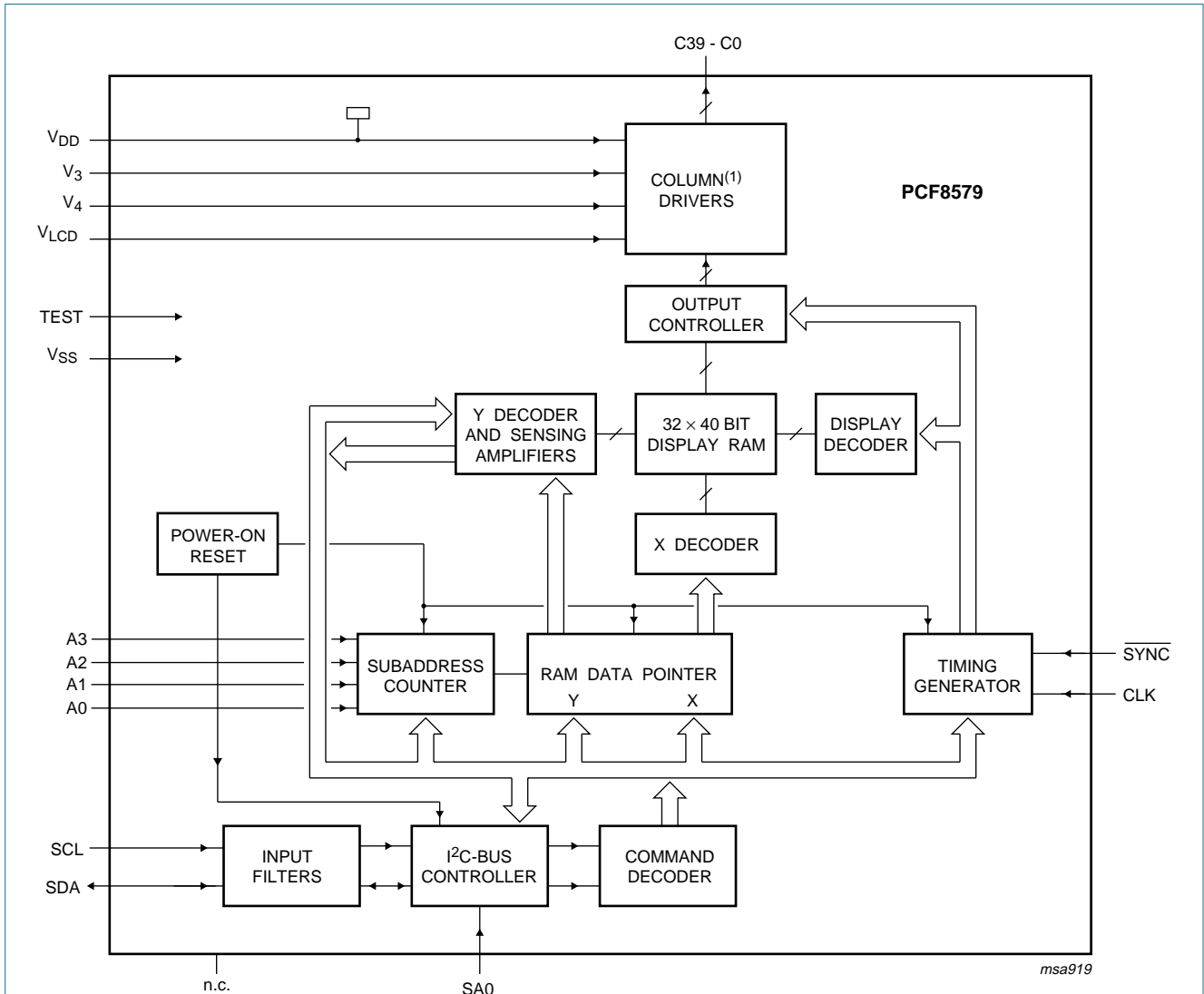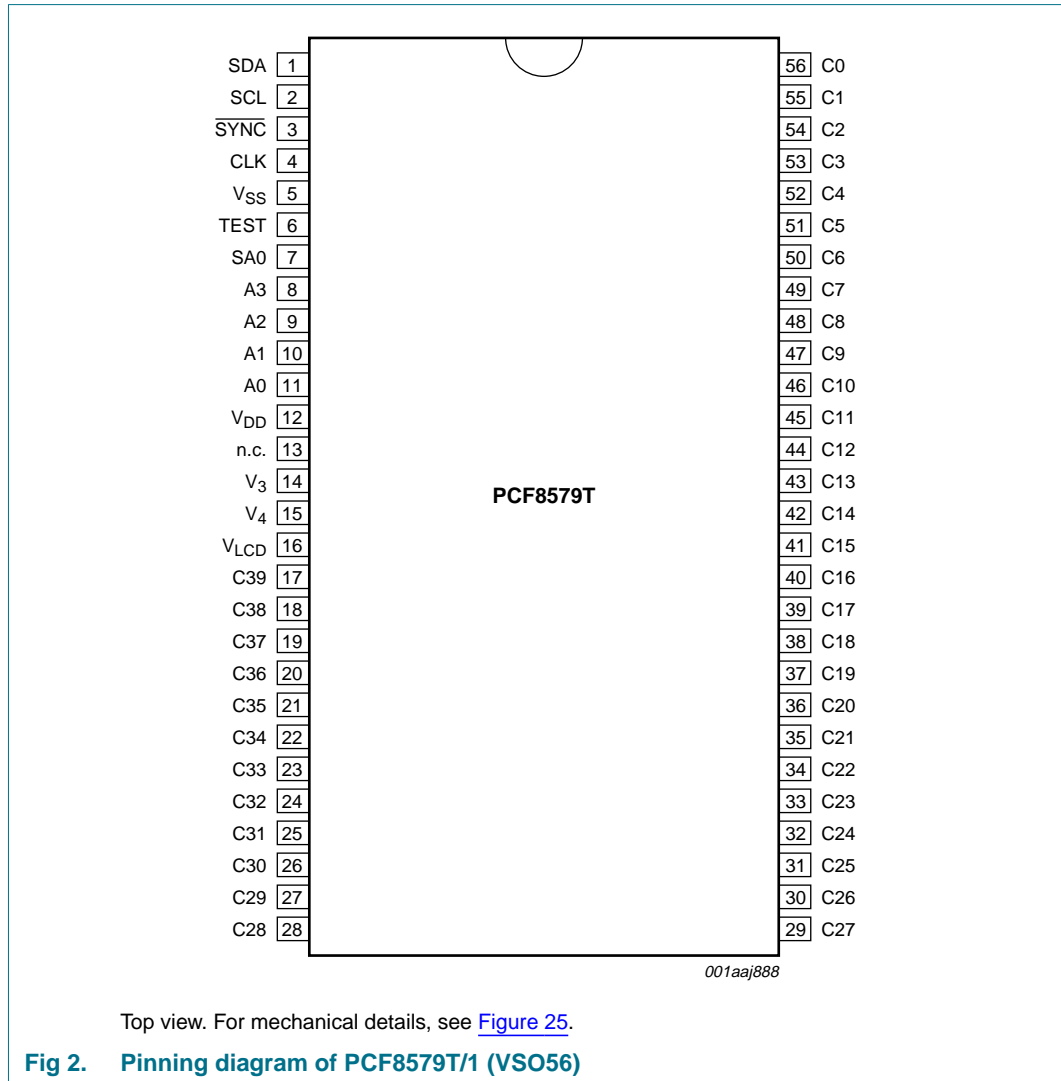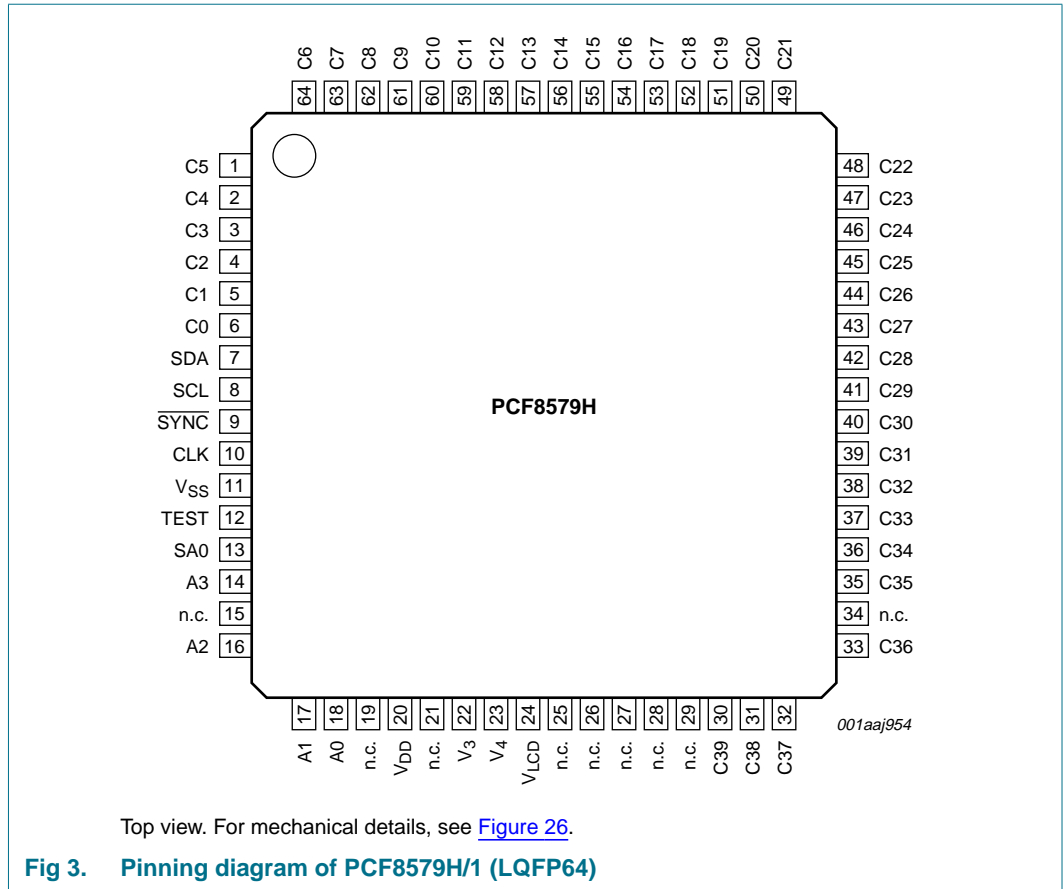
6. Block diagram

(1) Operates at LCD voltage levels, all other blocks operate at logic levels.

Fig 1. **Block diagram**

7. Pinning information

7.1 Pinning

Pin	Signal		Pin	Signal
1	SDA		56	C0
2	SCL		55	C1
3	$\overline{SYNC}$		54	C2
4	CLK		53	C3
5	V_{SS}		52	C4
6	TEST		51	C5
7	SA0		50	C6
8	A3		49	C7
9	A2		48	C8
10	A1		47	C9
11	A0		46	C10
12	V_{DD}		45	C11
13	n.c.		44	C12
14	V_3		43	C13
15	V_4		42	C14
16	V_{LCD}		41	C15
17	C39		40	C16
18	C38		39	C17
19	C37		38	C18
20	C36		37	C19
21	C35		36	C20
22	C34		35	C21
23	C33		34	C22
24	C32		33	C23
25	C31		32	C24
26	C30		31	C25
27	C29		30	C26
28	C28		29	C27

PCF8579T

001aaj888

Top view. For mechanical details, see Figure 25.

Fig 2.   **Pinning diagram of PCF8579T/1 (VSO56)**

Top view. For mechanical details, see Figure 26.

Fig 3. **Pinning diagram of PCF8579H/1 (LQFP64)**

Top view. For mechanical details, see Figure 27.

Fig 4.   Pinning diagram of PCF8579HT/1 (TQFP64)

7.2 Pin description

Table 3.   Pin description

Symbol	Pin		Description
	VSO56	**LQFP64, TQFP64**	
SDA	1	7	I^{2}C-bus serial data input/output
SCL	2	8	I^{2}C-bus serial clock input
$\overline{SYNC}$	3	9	cascade synchronization output
CLK	4	10	external clock input/output
V$_{SS}$	5	11	ground
TEST[1]	6	12	test pin
SA0	7	13	I^{2}C-bus slave address input (bit 0)
A3 to A0	8 to 11	14, 16 to 18	I^{2}C-bus subaddress inputs
V$_{DD}$	12	20	supply voltage
n.c.[2]	13	15, 19, 21, 25 to 29, 34	not connected
V$_3$, V$_4$	14, 15	22, 23	LCD bias voltage inputs
V$_{LCD}$	16	24	LCD supply voltage
C39 to C0	17 to 56	30 to 33, 35 to 64, 1 to 6	LCD column driver outputs

[1]   The TEST pin must be connected to V$_{SS}$.

[2]   Do not connect, these pins are reserved.

8. Functional description

The PCF8579 column driver is designed for use with the PCF8578. Together they form a general purpose LCD dot matrix chip set.

Typically up to 16 PCF8579s may be used with one PCF8578 (examples of cascading the devices see Table 16, Figure 21, Figure 22, Figure 23 and Figure 24). Each of the PCF8579s is identified by a unique 4-bit hardware subaddress, set by pins A0 to A3. The PCF8578 can operate with up to 32 PCF8579s when using two I^{2}C-bus slave addresses. The two slave addresses are set by the logic level on input SA0.

8.1 Power-on reset

At power-on the PCF8579 resets to a defined starting condition as follows:

1. Display blank (in conjunction with PCF8578)

2. 1:32 multiplex rate

3. Start bank 0 selected

4. Data pointer is set to X, Y address 0, 0

5. Character mode

6. Subaddress counter is set to 0

7. I^{2}C-bus interface is initialized

PCF8579_5

Product data sheet **Rev. 05 — 11 May 2009** 7 of 41

Remark: Do not transfer data on the I2C-bus for at least 1 ms after power-on to allow the reset action to complete.

8.2 Multiplexed LCD bias generation

The bias levels required to produce maximum contrast depend on the multiplex rate and the LCD threshold voltage (V_{th}). V_{th} is typically defined as the RMS voltage at which the LCD exhibits 10 % contrast. Table 4 shows the optimum voltage bias levels and Table 5 the discrimination ratios (D) for the different multiplex rates as functions of V_{oper}.

$$V_{oper} = V_{DD} - V_{LCD} \qquad (1)$$

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with the equation

$$V_{on(RMS)} = v_{oper}\sqrt{\frac{1}{n} + \frac{\sqrt{n}-1}{n(\sqrt{n}+1)}} \qquad (2)$$

and the RMS off-state voltage ($V_{off(RMS)}$) with the equation

$$V_{off(RMS)} = v_{oper}\sqrt{\frac{2(\sqrt{n}-1)}{\sqrt{n}(\sqrt{n}+1)^2}} \qquad (3)$$

where the values for n are determined by the multiplex rate (1:n). Valid values for n are:

n = 8 for 1:8 multiplex

n = 16 for 1:16 multiplex
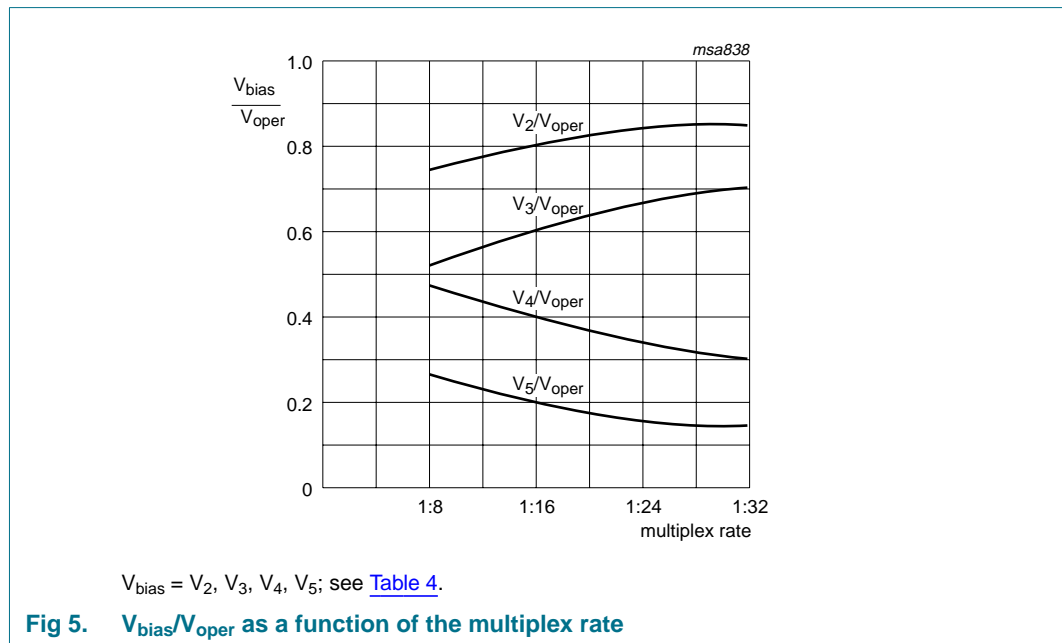
n = 24 for 1:24 multiplex

n = 32 for 1:32 multiplex

Table 4.   Optimum LCD voltages

Bias ratios	Multiplex rate			
	1:8	**1:16**	**1:24**	**1:32**
$\dfrac{V_2}{V_{oper}}$	0.739	0.800	0.830	0.850
$\dfrac{V_3}{V_{oper}}$	0.522	0.600	0.661	0.700
$\dfrac{V_4}{V_{oper}}$	0.478	0.400	0.339	0.300
$\dfrac{V_5}{V_{oper}}$	0.261	0.200	0.170	0.150

Table 5. **Discrimination ratios**

Discrimination ratios	Multiplex rate			
	1:8	1:16	1:24	1:32
$\dfrac{V_{off(RMS)}}{V_{oper}}$	0.297	0.245	0.214	0.193
$\dfrac{V_{on(RMS)}}{V_{oper}}$	0.430	0.316	0.263	0.230
$D = \dfrac{V_{on(RMS)}}{V_{off(RMS)}}$	1.447	1.291	1.230	1.196
$\dfrac{V_{oper}}{V_{th}}$	3.370	4.080	4.680	5.190

Figure 5 shows the values of Table 4 as graphs.

$V_{bias} = V_2, V_3, V_4, V_5$; see Table 4.

Fig 5. **V_{bias}/V_{oper} as a function of the multiplex rate**

8.3 LCD drive mode waveforms
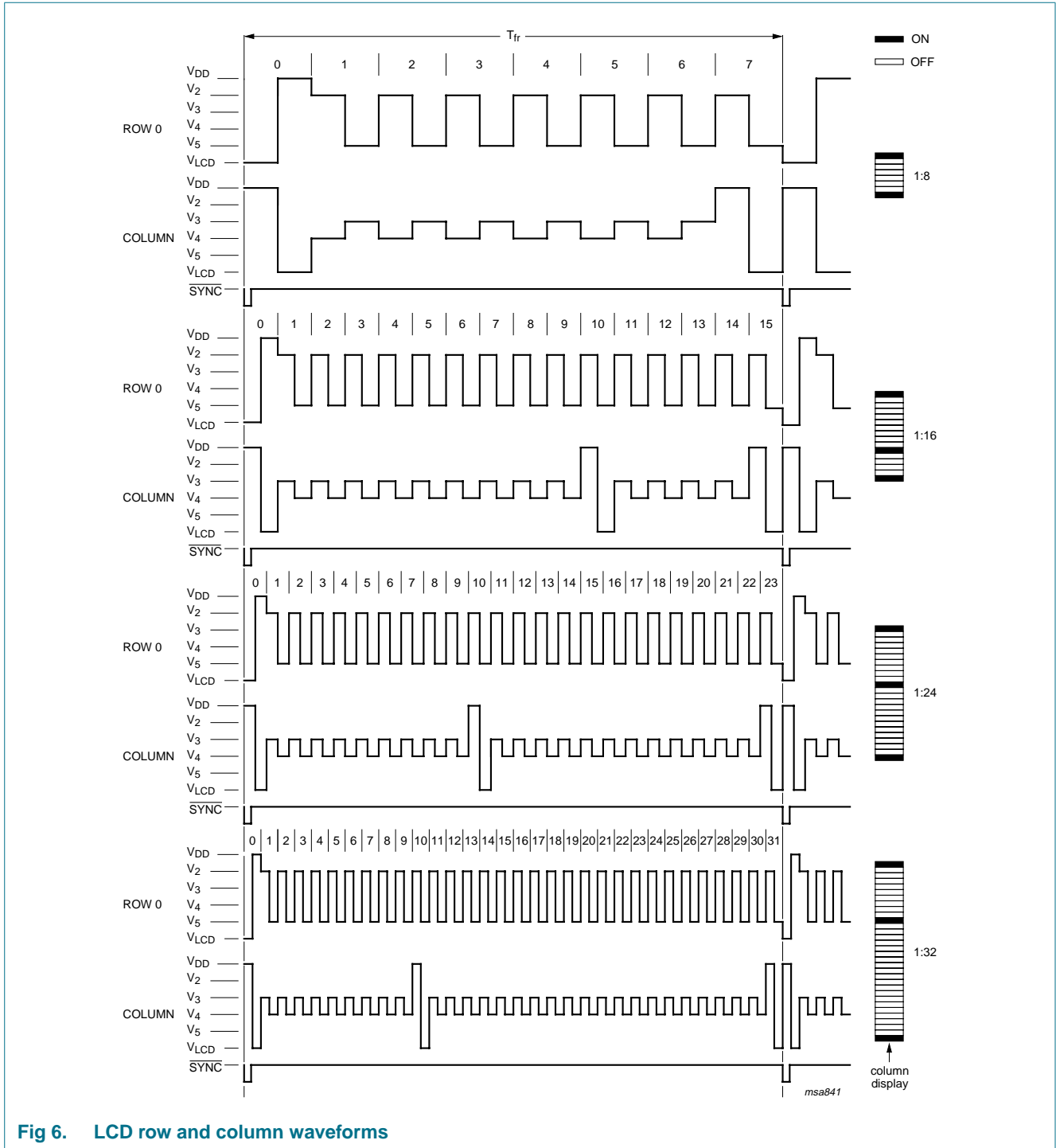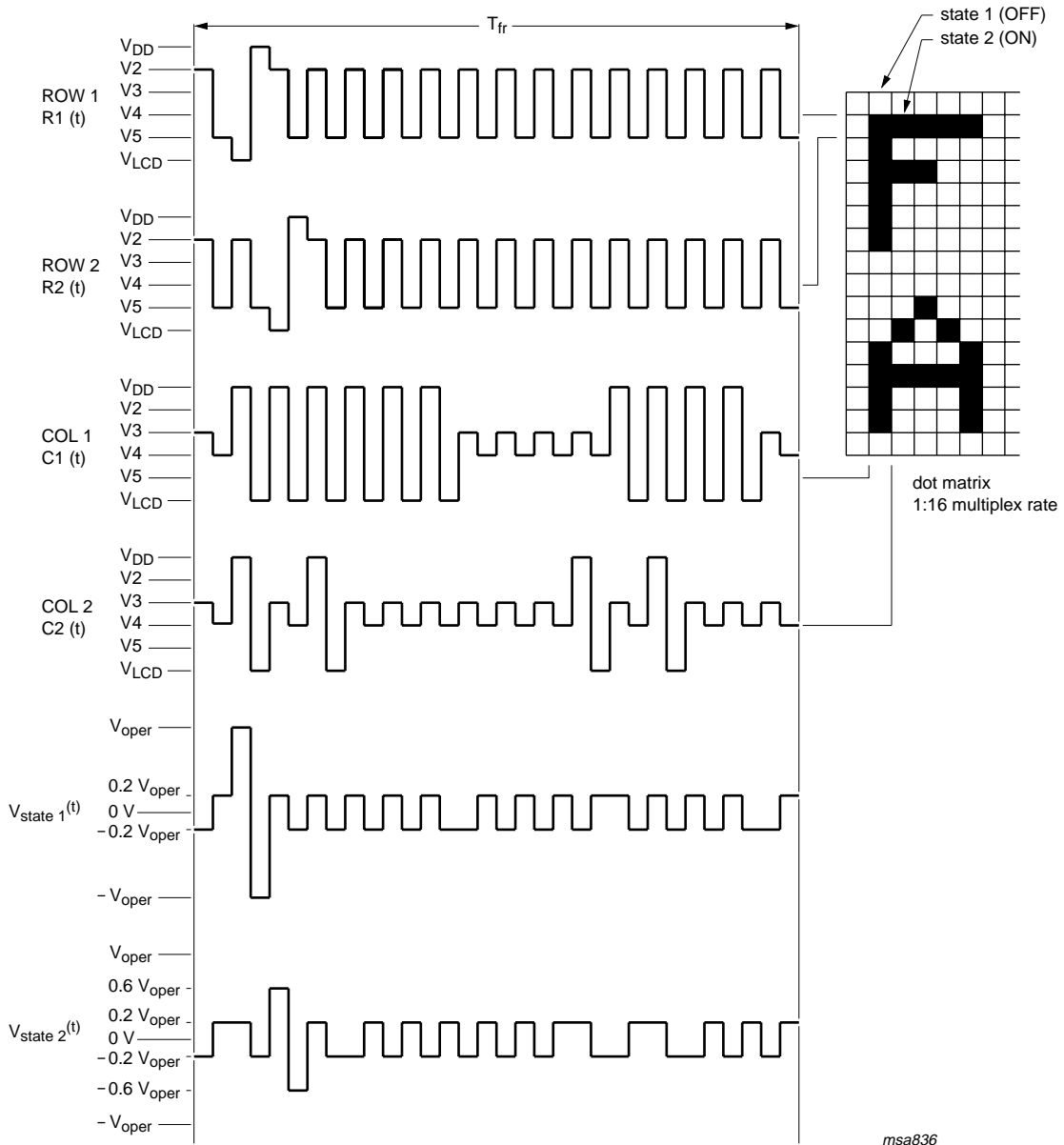

Fig 6. **LCD row and column waveforms**
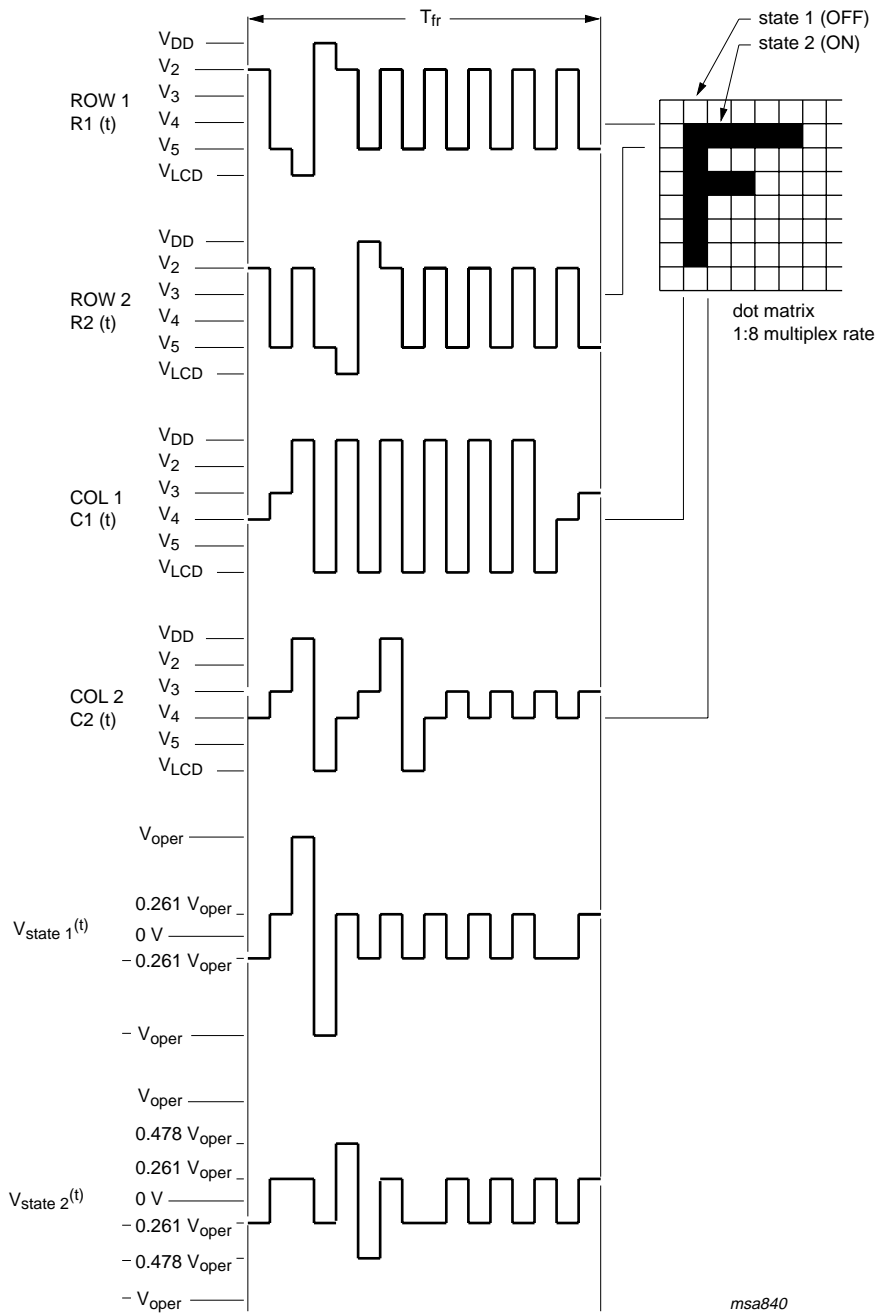
$V_{state1}(t) = C1(t) - R1(t).$

$$\frac{V_{on(RMS)}}{V_{oper}} = \sqrt{\frac{1}{8} + \frac{\sqrt{8}-1}{8(\sqrt{8}+1)}} = 0.430$$

$V_{state2}(t) = C2(t) - R2(t).$

$$\frac{V_{off(RMS)}}{V_{oper}} = \sqrt{\frac{2(\sqrt{8}-1)}{\sqrt{8}(\sqrt{8}+1)^2}} = 0.297$$

Fig 7. LCD drive mode waveforms for 1:8 multiplex rate

$V_{state1}(t) = C1(t) - R1(t).$

$$\frac{V_{on(RMS)}}{V_{oper}} = \sqrt{\frac{1}{16} + \frac{\sqrt{16}-1}{16(\sqrt{16}+1)}} = 0.316$$

$V_{state2}(t) = C2(t) - R2(t).$

$$\frac{V_{off(RMS)}}{V_{oper}} = \sqrt{\frac{2(\sqrt{16}-1)}{\sqrt{16}(\sqrt{16}+1)^2}} = 0.254$$

Fig 8.   LCD drive mode waveform for 1:16 multiplex rate

8.4 Timing generator

The timing generator of the PCF8579 organizes the internal data flow from the RAM to the display drivers. An external synchronization pulse $\overline{SYNC}$ is received from the PCF8578. This signal maintains the correct timing relationship between cascaded devices.

8.5 Column drivers

Outputs C0 to C39 are column drivers which must be connected to the LCD. Unused outputs should be left open-circuit.

8.6 Characteristics of the I^{2}C-bus

The I^{2}C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial Data Line (SDA) and a Serial Clock Line (SCL) which must be connected to a positive supply via a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

8.6.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this moment will be interpreted as control signals.

8.6.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of the data line, while the clock is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of the data line while the clock is HIGH, is defined as the STOP condition (P).

8.6.3 System configuration

A device transmitting a message is a transmitter, a device receiving a message is the receiver. The device that controls the message flow is the master and the devices which are controlled by the master are the slaves.

8.6.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each data byte of eight bits is followed by one acknowledge bit. The acknowledge bit is a HIGH level put on the bus by the transmitter, whereas the master generates an extra acknowledge related clock pulse. A slave receiver which is addressed must generate an acknowledge after the reception of each byte. Also a master must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter. The device that acknowledges must pull down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration). A master receiver must signal the end of a data transmission to the transmitter by **not** generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.
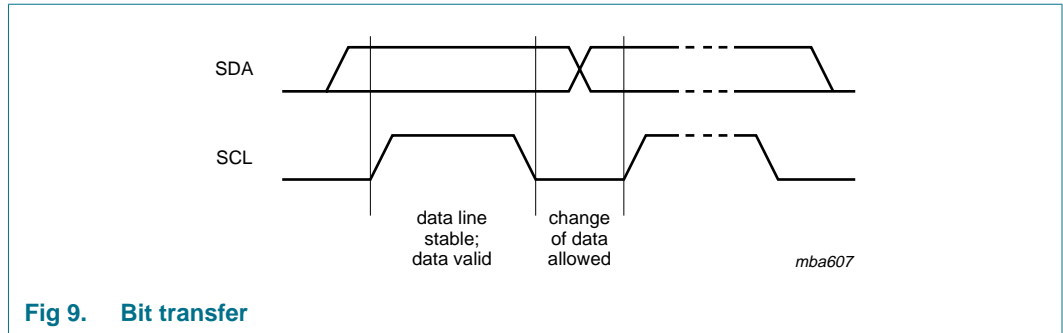
PCF8579_5

Product data sheet **Rev. 05 — 11 May 2009** 13 of 41
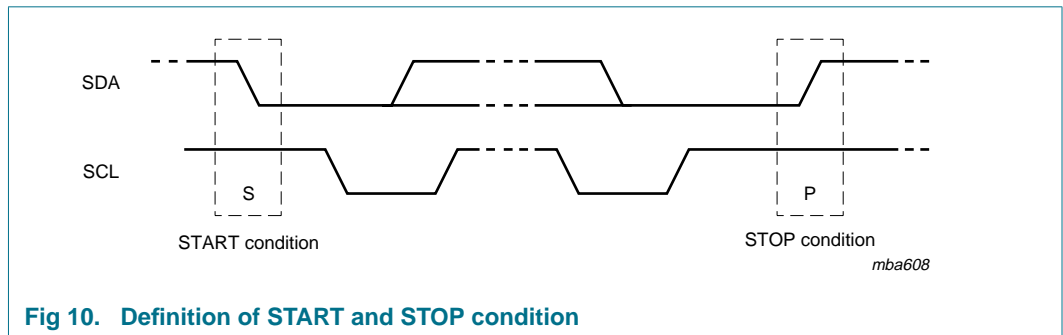
Fig 9. **Bit transfer**

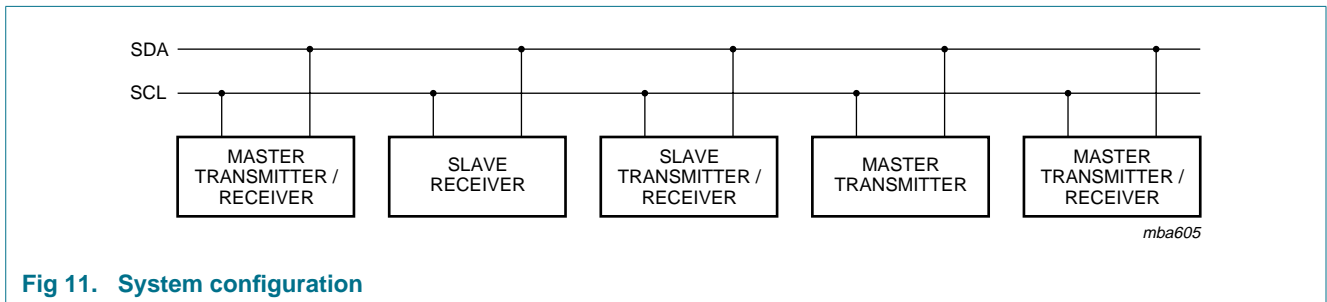**Fig 10.** **Definition of START and STOP condition**
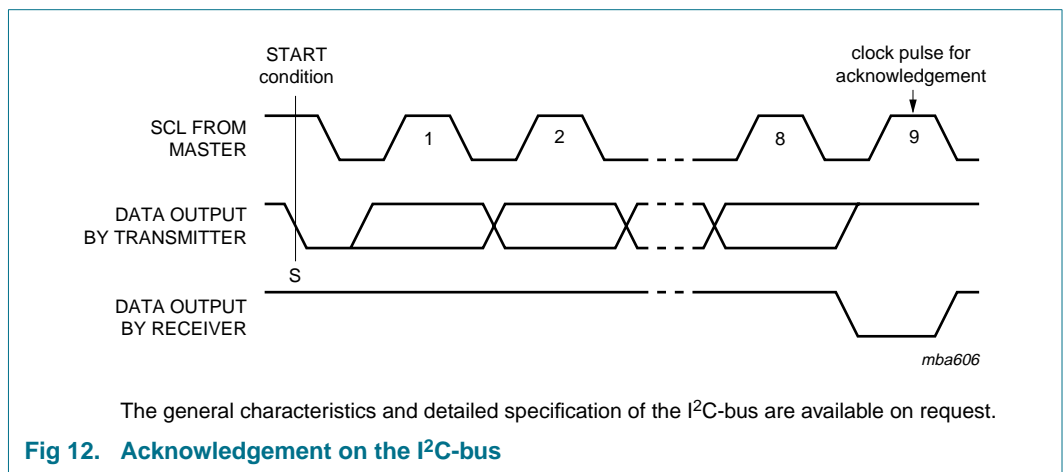

Fig 11. **System configuration**

The general characteristics and detailed specification of the I²C-bus are available on request.

Fig 12. **Acknowledgement on the I²C-bus**

PCF8579_5

Product data sheet **Rev. 05 — 11 May 2009** 14 of 41

8.6.5 I^{2}C-bus controller

The I^{2}C-bus controller detects the I^{2}C-bus protocol, slave address, commands and display data bytes. It performs the conversion of the data input (serial-to-parallel) and the data output (parallel-to-serial). The PCF8579 acts as an I^{2}C-bus slave transmitter/receiver. Device selection depends on the I^{2}C-bus slave address, the hardware subaddress and the commands transmitted.

8.6.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

8.6.7 I^{2}C-bus protocol

Two 7-bit slave addresses (0111100 and 0111101) are reserved for both the PCF8578 and PCF8579. The least significant bit of the slave address is set by connecting input SA0 to either logic 0 (V_{SS}) or logic 1 (V_{DD}). Therefore, two types of PCF8578 or PCF8579 can be distinguished on the same I^{2}C-bus which allows:

1. One PCF8578 to operate with up to 32 PCF8579s on the same I^{2}C-bus for very large applications (see Table 16).
2. The use of two types of LCD multiplex schemes on the same I^{2}C-bus.

In most applications the PCF8578 will have the same slave address as the PCF8579.

The I^{2}C-bus protocol is shown in Figure 13. All communications are initiated with a START condition (S) from the I^{2}C-bus master, which is followed by the desired slave address and read/write bit. All devices with this slave address acknowledge in parallel. All other devices ignore the bus transfer.

In WRITE mode (indicated by setting the read/write bit LOW) one or more commands follow the slave address acknowledgement. The commands are also acknowledged by all addressed devices on the bus. The last command must clear the continuation bit C. After the last command a series of data bytes may follow. The acknowledgement after each byte is made only by the (A0, A1, A2 and A3) addressed PCF8579 or PCF8578 with its implicit subaddress 0. After the last data byte has been acknowledged, the I^{2}C-bus master issues a STOP condition (P).

In READ mode, indicated by setting the read/write bit HIGH, data bytes may be read from the RAM following the slave address acknowledgement. After this acknowledgement the master transmitter becomes a master receiver and the PCF8579 becomes a slave transmitter. The master receiver must acknowledge the reception of each byte in turn. The master receiver must signal an end of data to the slave transmitter, by not generating an acknowledge on the last byte clocked out of the slave. The slave transmitter then leaves the data line HIGH, enabling the master to generate a STOP condition (P).

Display bytes are written into, or read from the RAM at the address specified by the data pointer and subaddress counter. Both the data pointer and subaddress counter are automatically incremented, enabling a stream of data to be transferred either to, or from the intended devices.

In multiple device applications, the hardware subaddress pins of the PCF8579s (A0 to A3) are connected to V_{SS} or V_{DD} to represent the desired hardware subaddress code. If two or more devices share the same slave address, then each device **must** be allocated a unique hardware subaddress.
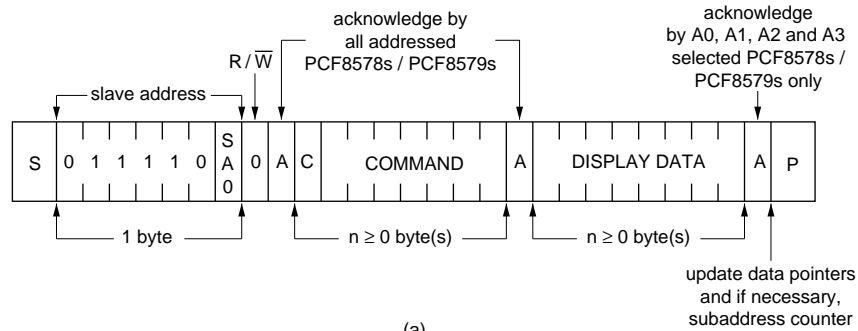
a. Master transmits to slave receiver (write mode)
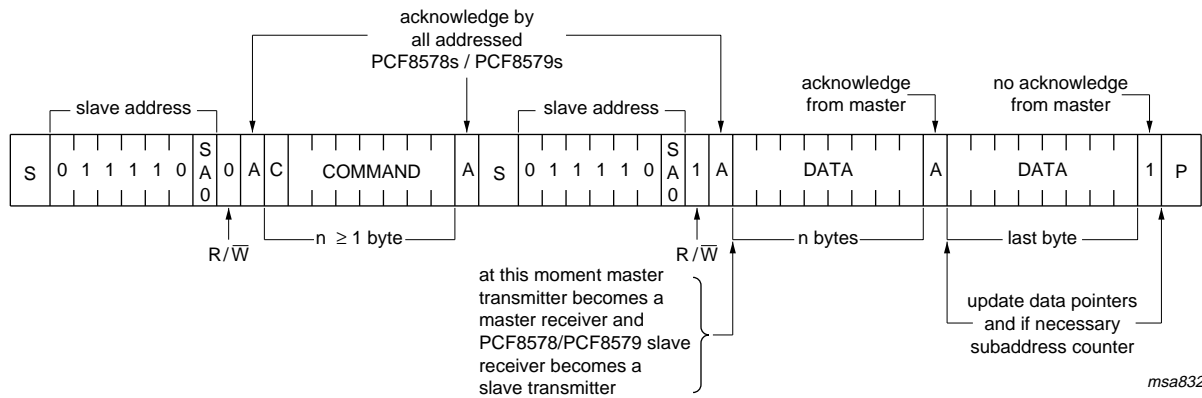
b. Master reads after sending command string (write commands; read data)

c. Master reads slave immediately after sending slave address (read mode)

Fig 13. I²C-bus protocol

8.7 Display RAM

The PCF8579 contains a 32×40-bit static RAM which stores the display data. The RAM is divided into 4 banks of 40 bytes ($4 \times 8 \times 40$ bits). During RAM access, data is transferred to or from the RAM via the I^{2}C-bus.
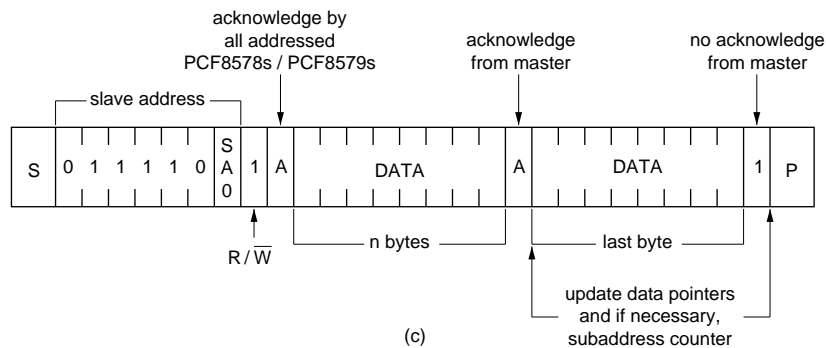
8.7.1 Data pointer

The addressing mechanism for the display RAM is realized using the data pointer. This allows an individual data byte or a series of data bytes to be written into, or read from, the display RAM, controlled by commands sent on the I^{2}C-bus.

8.7.2 Subaddress counter

The storage and retrieval of display data is dependent on the content of the subaddress counter. Storage and retrieval take place only when the contents of the subaddress counter matches with the hardware subaddress at pins A0, A1, A2 and A3.

8.8 Command decoder

The command decoder identifies command bytes that arrive on the I^{2}C-bus.

The five commands available to the PCF8579 are defined in Table 6.

Table 6.   Definition of PCF8579 commands

Command	Operation code								Reference
Bit	7	6	5	4	3	2	1	0	
set-mode	C	1	0	T	E[1:0]		M[1:0]		Table 8
set-start-bank	C	1	1	1	1	1	B[1:0]		Table 9
device-select	C	1	1	0	A[3:0]				Table 10
RAM-access	C	1	1	1	G[1:0]		Y[1:0]		Table 11
load-X-address	C	0	X[5:0]						Table 12

The most-significant bit of a command is the continuation bit C (see Table 7 and Figure 14). Commands are transferred in WRITE mode only.

Table 7.   C bit description

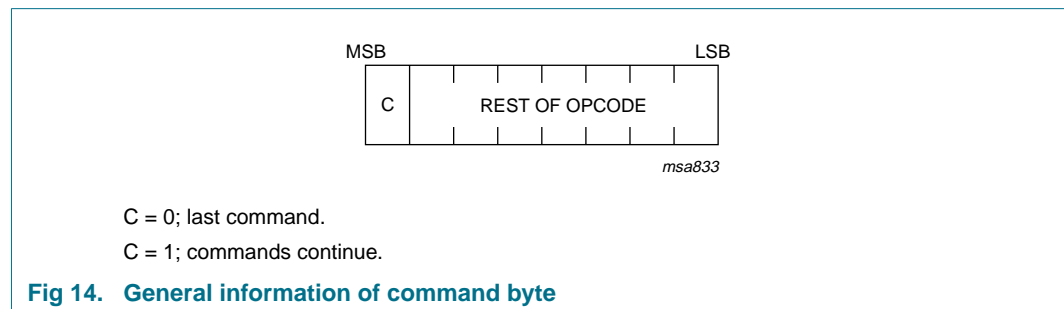| Bit	Symbol	Value	Description
7	C		continue bit
		0	last control byte in the transfer; next byte will be regarded as display data
		1	control bytes continue; next byte will be a command too

msa833

C = 0; last command.

C = 1; commands continue.

Fig 14. General information of command byte

Table 8.   Set-mode - command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 7
6, 5	-	10	fixed value
4	T		display mode
		0	PCF8578 row only
		1	PCF8578 mixed mode
3, 2	E[1:0]		display status
		00	blank
		01	normal
		10	all segments on
		11	inverse video
1, 0	M[1:0]		LCD drive mode
		01	1:8 MUX (8 rows)
		10	1:16 MUX (16 rows)
		11	1:24 MUX (24 rows)
		00	1:32 MUX (32 rows)

Table 9.   Set-start-bank - command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 7
6 to 2	-	11111	fixed value
1, 0	B[1:0]		start bank pointer (see Figure 18)[1]
		00	bank 0
		01	bank 1
		10	bank 2
		11	bank 3

[1]   Useful for scrolling, pseudo-motion and background preparation of new display content.

Table 10.   Device-select - command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 7
6 to 4	-	110	fixed value
3 to 0	A[3:0]	0 to 15[1]	hardware subaddress; 4 bit binary value; transferred to the subaddress counter to define one of sixteen hardware subaddresses

[1]   Values shown in decimal.

Table 11. RAM-access - command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 7
6 to 4	-	111	fixed value
3, 2	G[1:0]		RAM access mode;
			defines the auto-increment behavior of the address for RAM access (see Figure 17)
		00	character
		01	half-graphic
		10	full-graphic
		11	not allowed[1]
1, 0	Y[1:0]	0 to 3[2]	RAM row address;
			two bits of immediate data, transferred to the Y-address pointer to define one of four display RAM rows (see Figure 15)

[1] See operation code for set-start-bank in Table 9.

[2] Values shown in decimal.

Table 12. Load-X-address - command bit description

Bit	Symbol	Value	Description
7	C	0, 1	see Table 7
6	-	0	fixed value
5 to 0	X[5:0]	0 to 39[1]	RAM column address;
			six bits of immediate data, transferred to the X-address pointer to define one of forty display RAM columns (see Figure 15)

[1] Values shown in decimal.
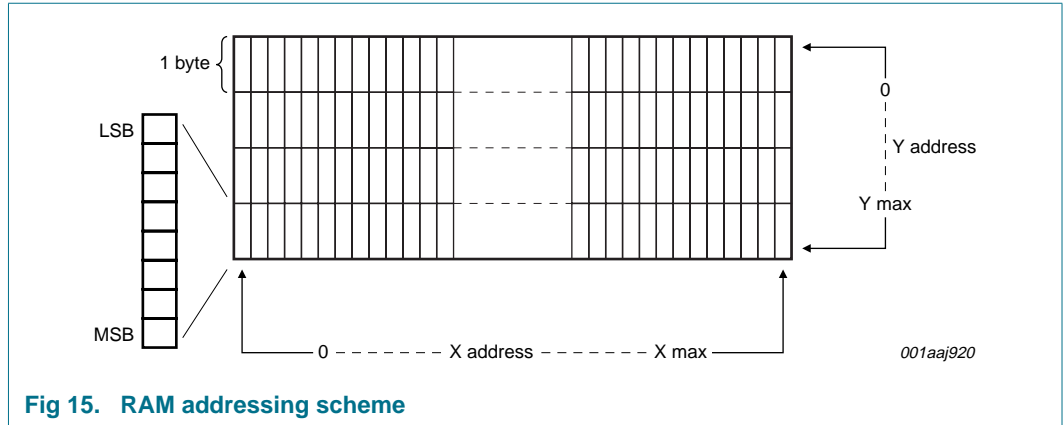
8.9 RAM access

Fig 15. RAM addressing scheme

There are three RAM-access modes:

- Character
- Half-graphic
- Full-graphic

These modes are specified by the bits G[1:0] of the RAM-access command. The RAM-access command controls the order in which data is written to or read from the RAM (see Figure 17).

To store RAM data, the user specifies the location into which the first byte will be loaded (see Figure 16):

- Device subaddress (specified by the device-select command)
- RAM X-address (specified by the bits X[5:0] of the load-X-address command)
- RAM bank (specified by the bits Y[1:0] of the RAM-access command)

Subsequent data bytes will be written or read according to the chosen RAM-access mode. Device subaddresses are automatically incremented between devices until the last device is reached. If the last device has subaddress 15, further display data transfers will lead to a wrap-around of the subaddress to 0.
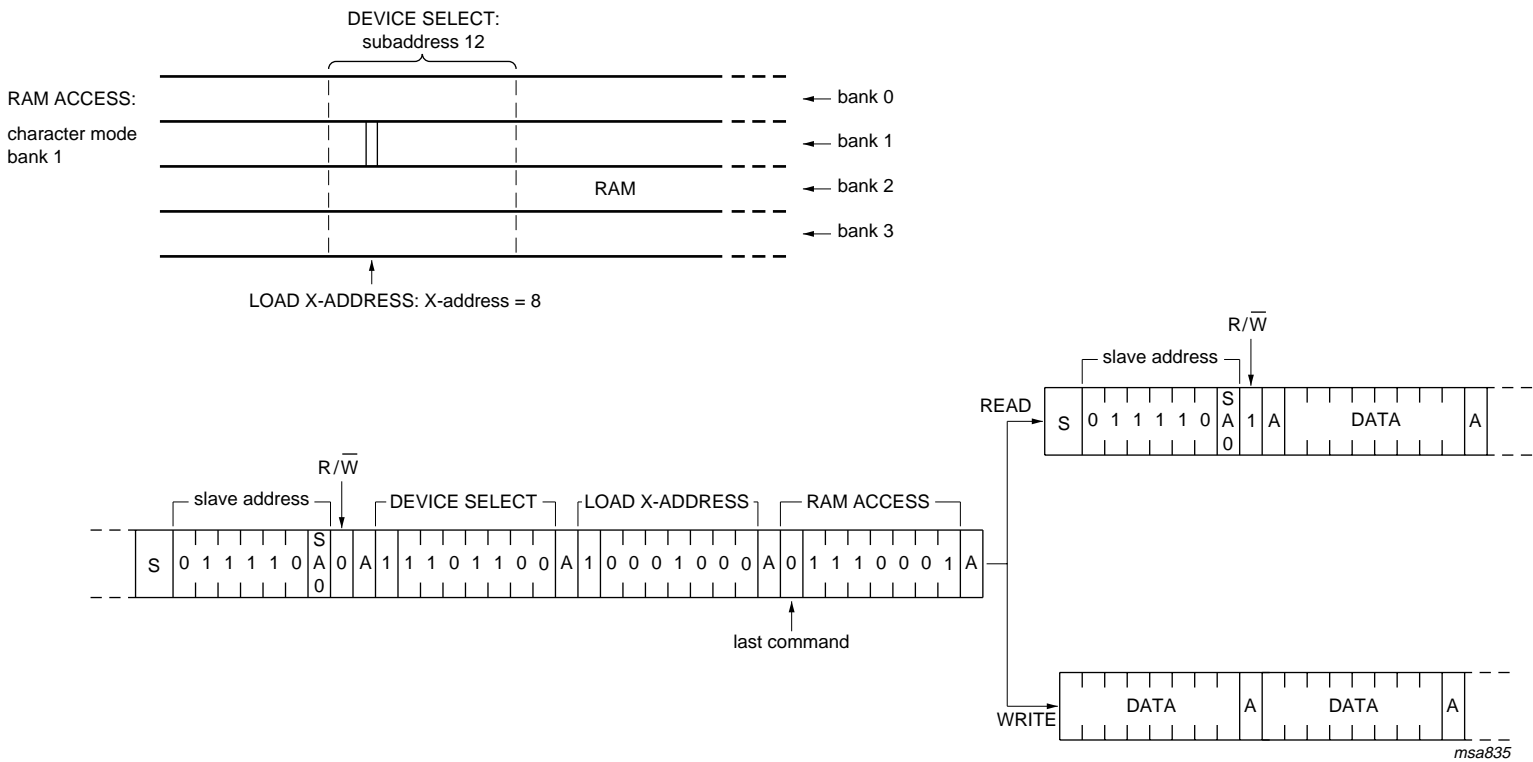
Fig 16.   Example of commands specifying initial data byte RAM locations

PCF8578/PCF8579   **PCF8579**

driver 1   driver 2   driver k

RAM
4 bytes

bank 0
bank 1
bank 2
bank 3

40-bits

PCF8578/PCF8579 system RAM
1 ≤ k ≤ 16

LSB

MSB

1 byte | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |

character mode

2 bytes
| 0 | 2 | 4 | 6 | 8 | 10 | 12 | 14 | 16 | 18 | 20 | 22 |
| 1 | 3 | 5 | 7 | 9 | 11 | 13 | 15 | 17 | 19 | 21 | 23 |

half-graphic mode

4 bytes
0	4	8	12	16	20	24	28	32	36	40	44
1	5	9	13	17	21	25	29	33	37	41	45
2	6	10	14	18	22	26	30	34	38	42	46
3	7	11	15	19	23	27	31	35	39	43	47

RAM data bytes are
written or read as
indicated above

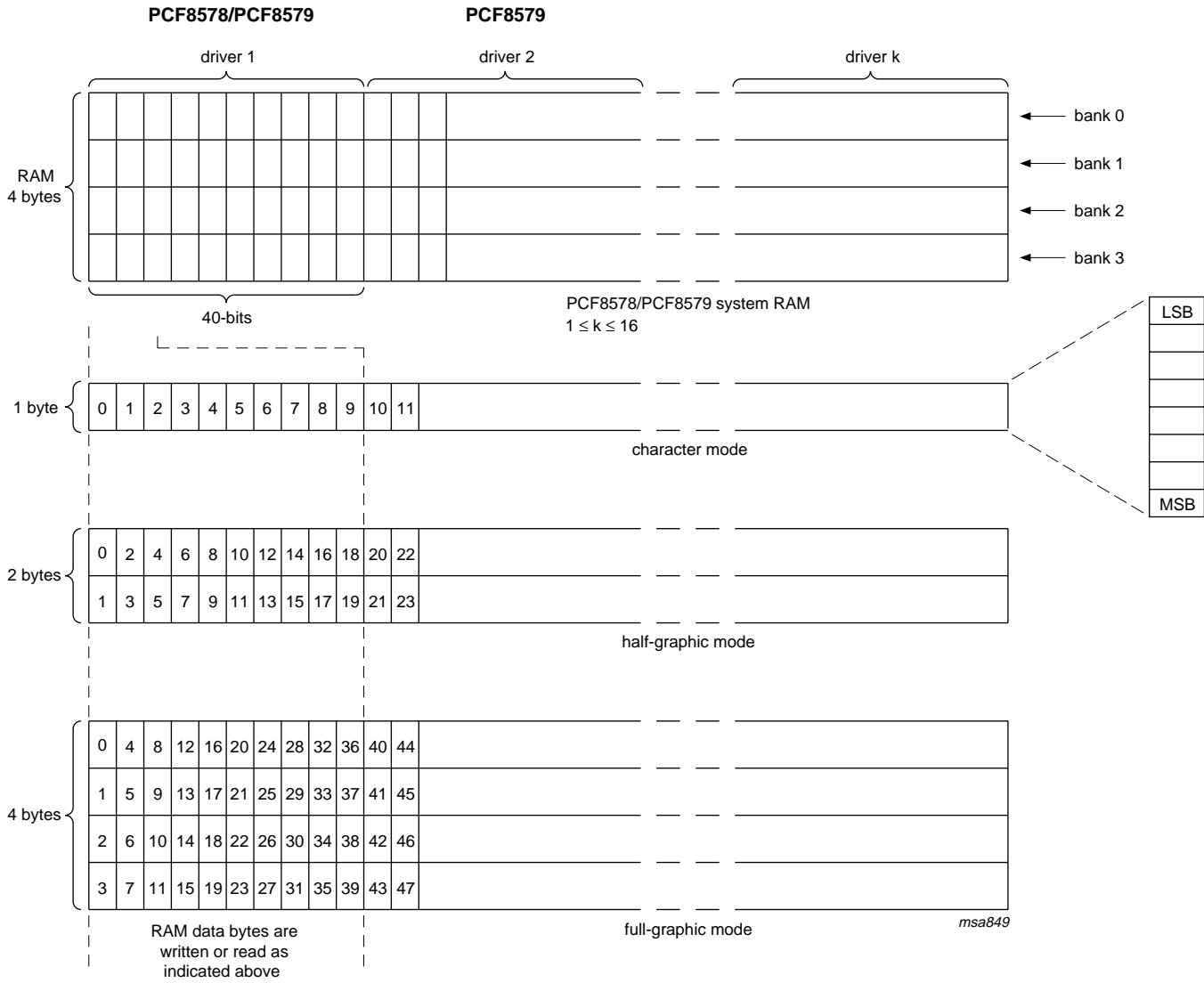full-graphic mode

msa849

Fig 17. RAM access mode

8.9.1 Display control

The display is generated by continuously shifting rows of RAM data to the dot matrix LCD via the column outputs. The number of rows scanned depends on the multiplex rate set by bits M[1:0] of the set-mode command.

1:32 multiplex rate and start bank = 2.

Fig 18. Relationship between display and set-start-bank
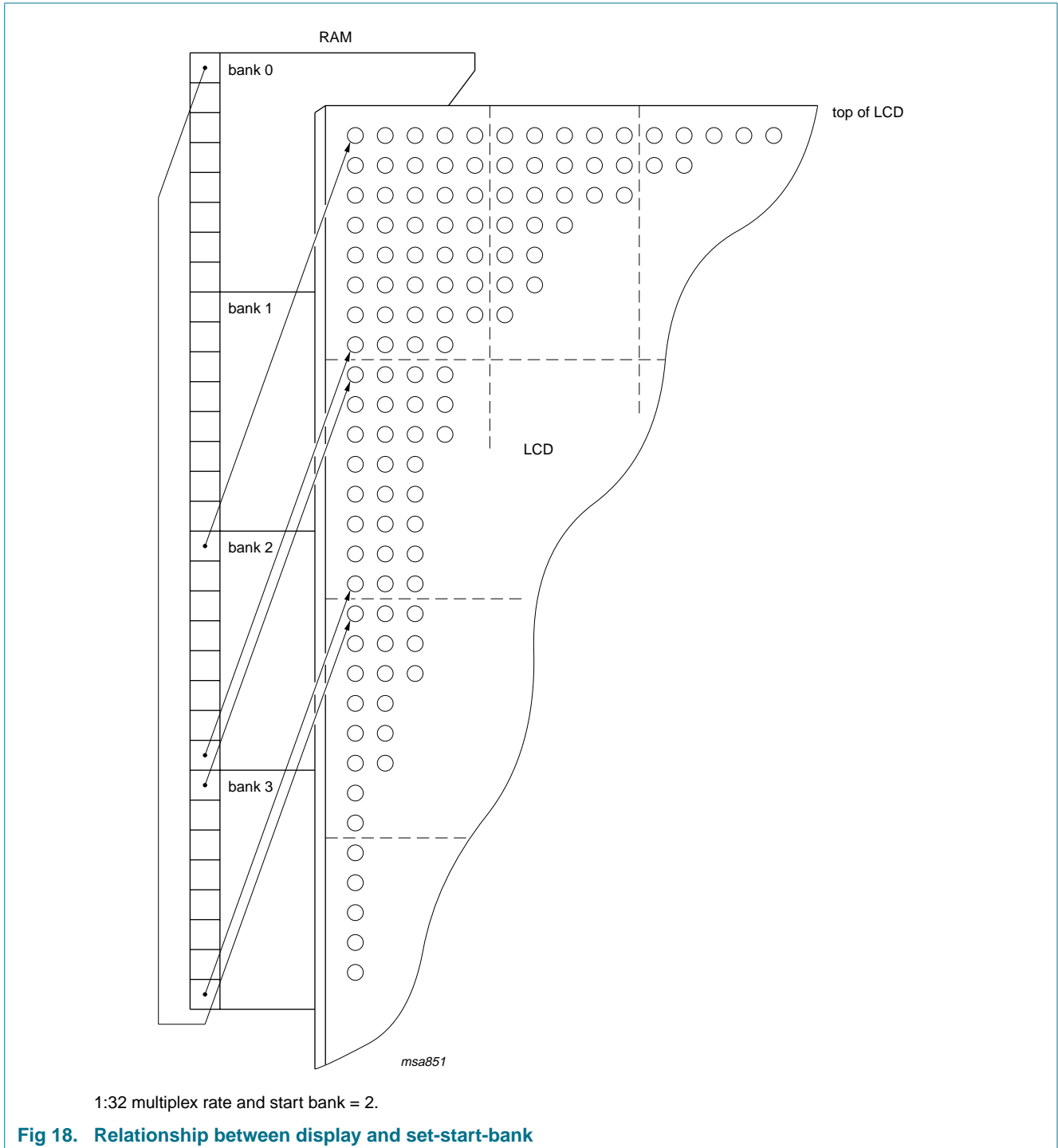
The display status (all dots on or off and normal or inverse video) is set by the bits E[1:0] of the set-mode command. For bank switching, the RAM bank corresponding to the top of the display is set by the bits B[1:0] of the set-start-bank command. This is shown in Figure 18. This feature is useful when scrolling in alphanumeric applications.

9. Limiting values

Table 13. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD}	supply voltage		−0.5	+8.0	V
V_{LCD}	LCD supply voltage		$V_{DD} - 11$	+8.0	V
V_I	input voltage	V_{DD} related; on pins SDA, SCL, CLK, TEST, SA0 and OSC	−0.5	+8.0	V
		V_{LCD} related; V_3 and V_4	$V_{DD} - 11$	+8.0	V
V_O	output voltage	V_{DD} related; $\overline{SYNC}$ and CLK	−0.5	+8.0	V
		V_{LCD} related; R0 to R7, R8/C8 to R31/C31 and C32 to C39	$V_{DD} - 11$	+8.0	V
I_I	input current		−10	+10	mA
I_O	output current		−10	+10	mA
I_{DD}	supply current		−50	+50	mA
$I_{DD(LCD)}$	LCD supply current		−50	+50	mA
I_{SS}	ground supply current		−50	+50	mA
P_{tot}	total power dissipation	per package	-	400	mW
P_o	output power		-	100	mW
T_{stg}	storage temperature	[1]	−65	+150	°C

[1] According to the NXP store and transport conditions (document *SNW-SQ-623*) the devices have to be stored at a temperature of +5 °C to +45 °C and a humidity of 25 % to 75 %.

PCF8579_5

Product data sheet **Rev. 05 — 11 May 2009** **24 of 41**

10. Static characteristics

Table 14. Static characteristics

V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; V_{LCD} = V_{DD} − 3.5 V to V_{DD} − 9 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			2.5	-	6.0	V
V_{LCD}	LCD supply voltage			V_{DD} − 9	-	V_{DD} − 3.5	V
I_{DD}	supply current	f_{clk} = 2 kHz	[1]	-	9	20	µA
V_{POR}	power-on reset voltage		[2]	-	1.3	1.8	V
Logic							
V_{IL}	LOW-level input voltage			V_{SS}	-	0.3V_{DD}	V
V_{IH}	HIGH-level input voltage			0.7V_{DD}	-	V_{DD}	V
I_L	leakage current	at pins SDA, SCL, $\overline{\text{SYNC}}$, CLK, TEST and SA0, A0 to A3; V_i = V_{DD} or V_{SS}		−1	-	+1	mA
I_{OL}	LOW-level output current	at pin SDA; V_{OL} = 0.4 V; V_{DD} = 5 V		3	-	-	mA
C_i	input capacitance	at pin SCL and SDA	[3]	-	-	5	pF
LCD outputs							
I_L	leakage current	at pins V_3 and V_4; V_i = V_{DD} or V_{LCD}		−2	-	+2	µA
$V_{offset(DC)}$	DC offset voltage	on pins C0 to C39		-	±20	-	mV
R_O	output resistance	on pins at C0 to C39	[4]	-	3	6	kΩ

[1] Outputs are open; inputs at V_{DD} or V_{SS}; I2C-bus inactive; external clock with 50 % duty factor.

[2] Resets all logic when V_{DD} < V_{POR}.

[3] Periodically sampled; not 100 % tested.

[4] Resistance measured between output terminal (C0 to C39) and bias input (V_3, V_4, V_{DD} and V_{LCD}) when the specified current flows through one output under the following conditions (see Table 4):

  a) V_{oper} = V_{DD} − V_{LCD} = 9 V.

  b) V_3 − V_{LCD} ≥ 4.70 V; V_4 − V_{LCD} ≤ 4.30 V; I_{load} = 100 µA.

11. Dynamic characteristics

Table 15.   Dynamic characteristics

All timing values are referenced to V_{IH} and V_{IL} levels with an input voltage swing of V_{SS} to V_{DD}. V_{DD} = 2.5 V to 6 V; V_{SS} = 0 V; $V_{LCD} = V_{DD} - 3.5$ V to $V_{DD} - 9$ V; $T_{amb} = -40 °C$ to $+85 °C$; unless otherwise specified.

| Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{clk}	clock frequency	50 % duty factor [1]	-	-	10	kHz
$t_{PD(drv)}$	driver propagation delay	$V_{DD} - V_{LCD}$ = 9 V; with test load of 45 pF	-	-	100	μs
I²C-bus						
f_{SCL}	SCL clock frequency		-	-	100	kHz
$t_{w(spike)}$	spike pulse width		-	-	100	ns
t_{BUF}	bus free time between a STOP and START condition		4.7	-	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	-	-	μs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	-	-	μs
t_{LOW}	LOW period of the SCL clock		4.7	-	-	μs
t_{HIGH}	HIGH period of the SCL clock		4.0	-	-	μs
t_r	rise time of both SDA and SCL signals		-	-	1	μs
t_f	fall time of both SDA and SCL signals		-	-	0.3	μs
$t_{SU;DAT}$	data set-up time		250	-	-	ns
$t_{HD;DAT}$	data hold time		0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition		4.0	-	-	μs

[1]   Typically 0.9 kHz to 3.3 kHz.
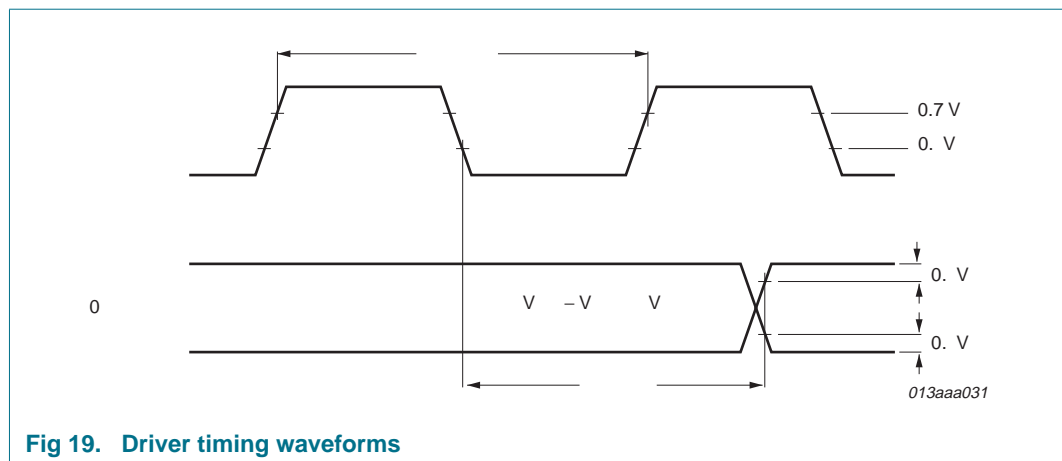
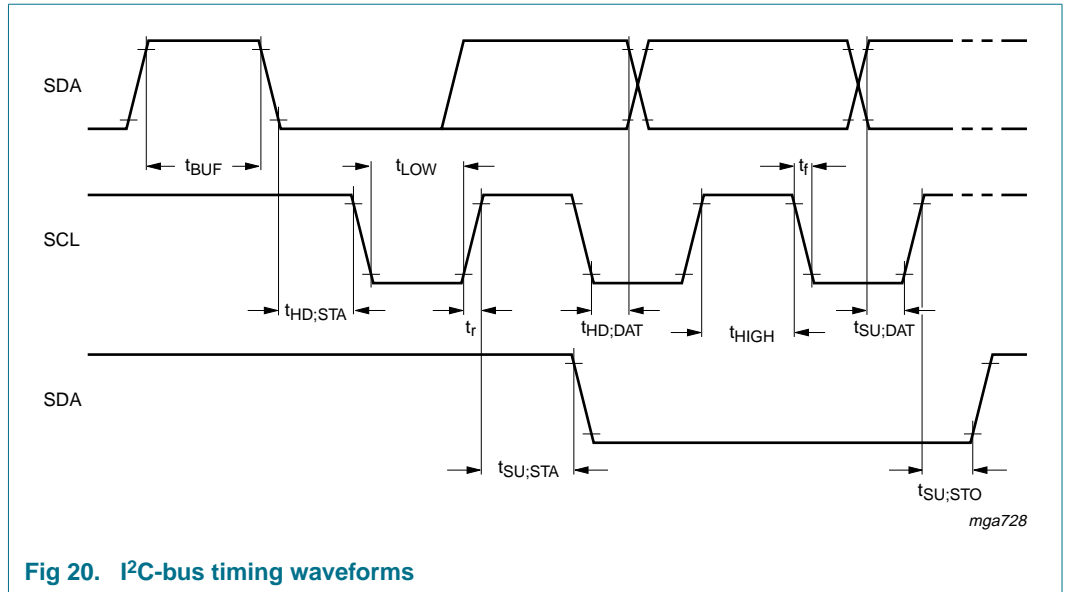**Fig 19.   Driver timing waveforms**

Fig 20. I²C-bus timing waveforms

12. Application information

Large display configurations of one PCF8578 and up to 32 PCF8579 can be recognized on the same I^{2}C-bus by using the 4-bit hardware subaddress A[3:0] and the I^{2}C-bus slave address SA0.

Table 16. Example of addressing one PCF8578 and 32 PCF8579
Pins connected to V_{SS} are logic 0; pins connected to V_{DD} are logic 1.

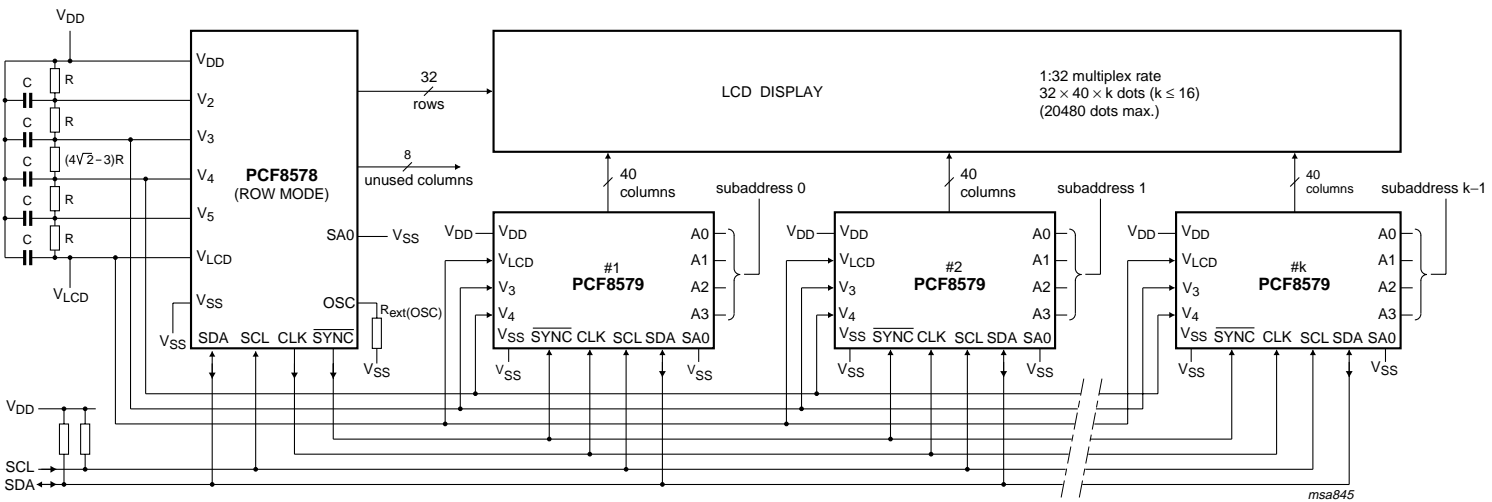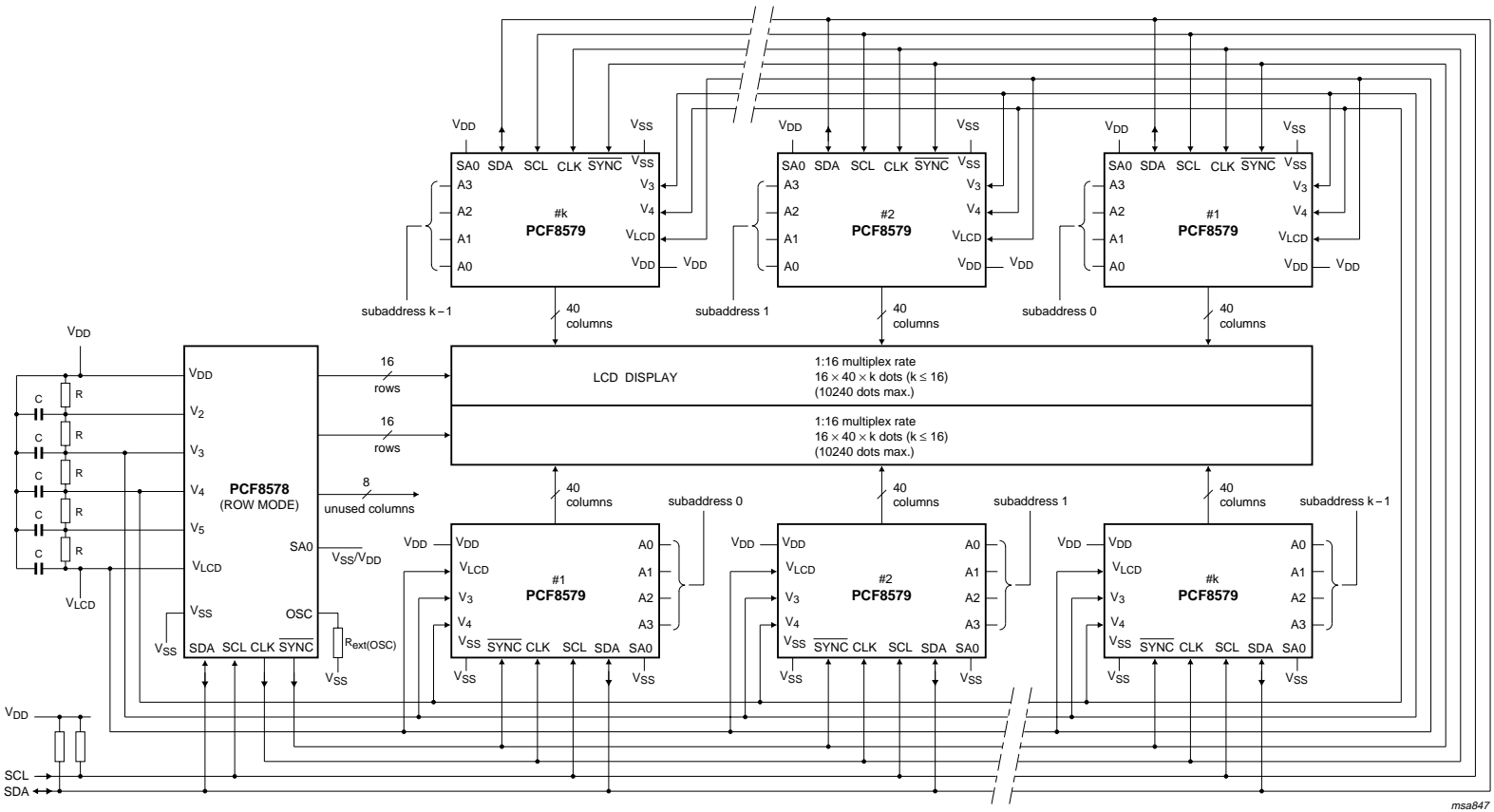| Cluster	SA0	A3	A2	A1	A0	Device
PCF8578						
-	0	-	-	-	-	0
PCF8579						
1	0	0	0	0	0	0
		0	0	0	1	1
		0	0	1	0	2
		0	0	1	1	3
		0	1	0	0	4
		0	1	0	1	5
		0	1	1	0	6
		0	1	1	1	7
		1	0	0	0	8
		1	0	0	1	9
		1	0	1	0	10
		1	0	1	1	11
		1	1	0	0	12
		1	1	0	1	13
		1	1	1	0	14
		1	1	1	1	15
2	1	0	0	0	0	16
		0	0	0	1	17
		0	0	1	0	18
		0	0	1	1	19
		0	1	0	0	20
		0	1	0	1	21
		0	1	1	0	22
		0	1	1	1	23
		1	0	0	0	24
		1	0	0	1	25
		1	0	1	0	26
		1	0	1	1	27
		1	1	0	0	28
		1	1	0	1	29
		1	1	1	0	30
		1	1	1	1	31

Fig 21. Typical LCD driver system with 1:32 multiplex rate

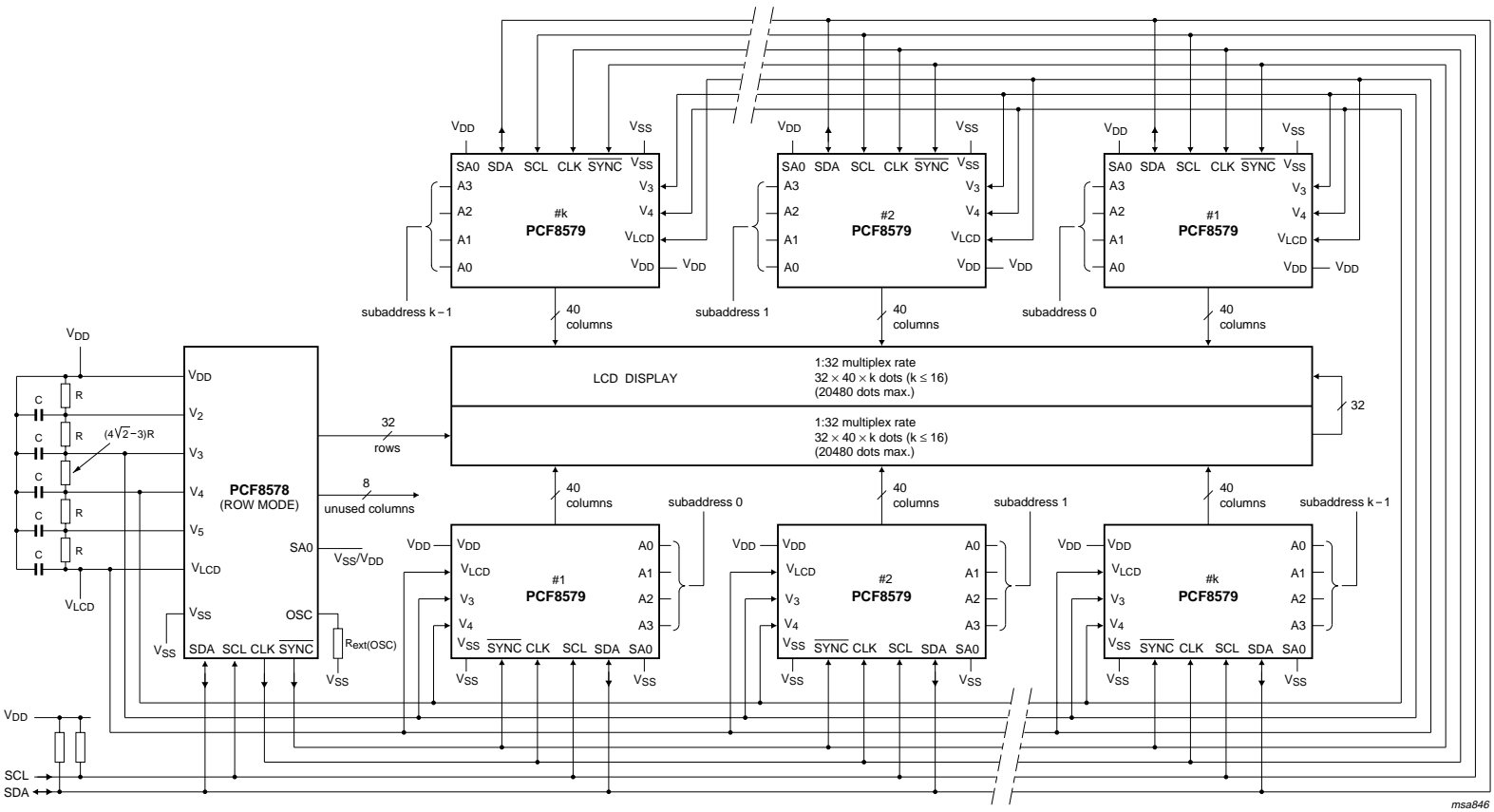**Fig 22. Split screen application with 1:16 multiplex rate for improved contrast**

msa847

Fig 23. Split screen application with 1:32 multiplex rate

V_{SS}
SCL V_{DD}
SDA V_{LCD}

R0

$R_{ext(OSC)}$
$(4\sqrt{2}-3)R$
R R R R

n.c.
n.c.

PCF8578

R31/C31

LCD DISPLAY

C0   C27   C28   C39   C0   C27   C28   C39

PCF8579

PCF8579

n.c.

n.c.

to other
PCF8579s

msa852

Fig 24. Example of single plane wiring, single screen with 1:32 multiplex rate (PCF8578 in row driver mode)

13. Package outline

VSO56: plastic very small outline package; 56 leads   **SOT190-1**

DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D[1]	E[2]	e	H_E	L	Lₚ	Q	v	w	y	Z[1]	θ
mm	3.3	0.3 0.1	3.0 2.8	0.25	0.42 0.30	0.22 0.14	21.65 21.35	11.1 11.0	0.75	15.8 15.2	2.25	1.6 1.4	1.45 1.30	0.2	0.1	0.1	0.90 0.55	7° 0°
inches	0.13	0.012 0.004	0.12 0.11	0.01	0.017 0.012	0.0087 0.0055	0.85 0.84	0.44 0.43	0.0295	0.62 0.60	0.089	0.063 0.055	0.057 0.051	0.008	0.004	0.004	0.035 0.022	

Notes

1. Plastic or metal protrusions of 0.3 mm (0.012 inch) maximum per side are not included.

2. Plastic interlead protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

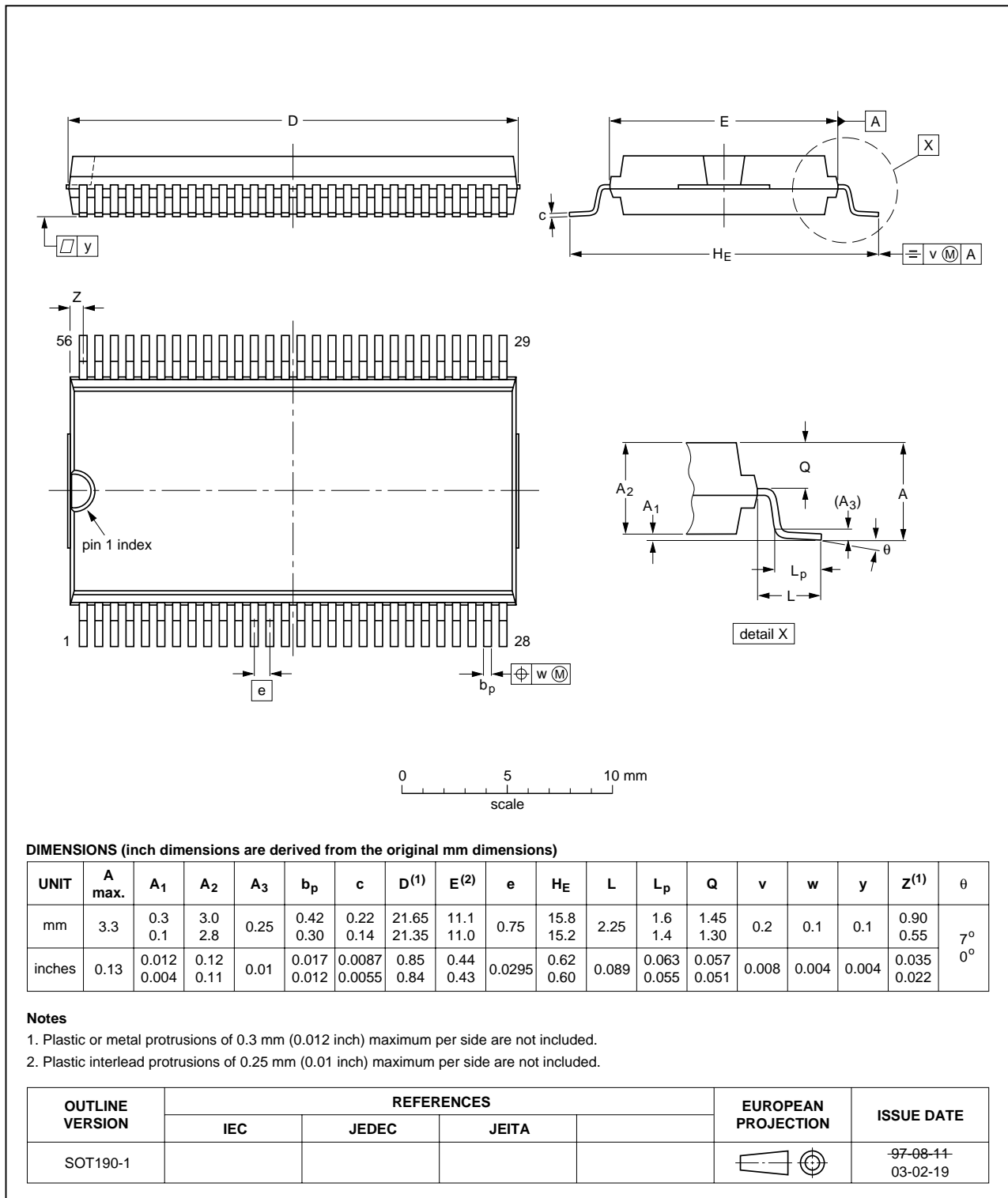| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT190-1						~~97-08-11~~ 03-02-19

Fig 25. Package outline of PCF8579T/1 (VSO56)

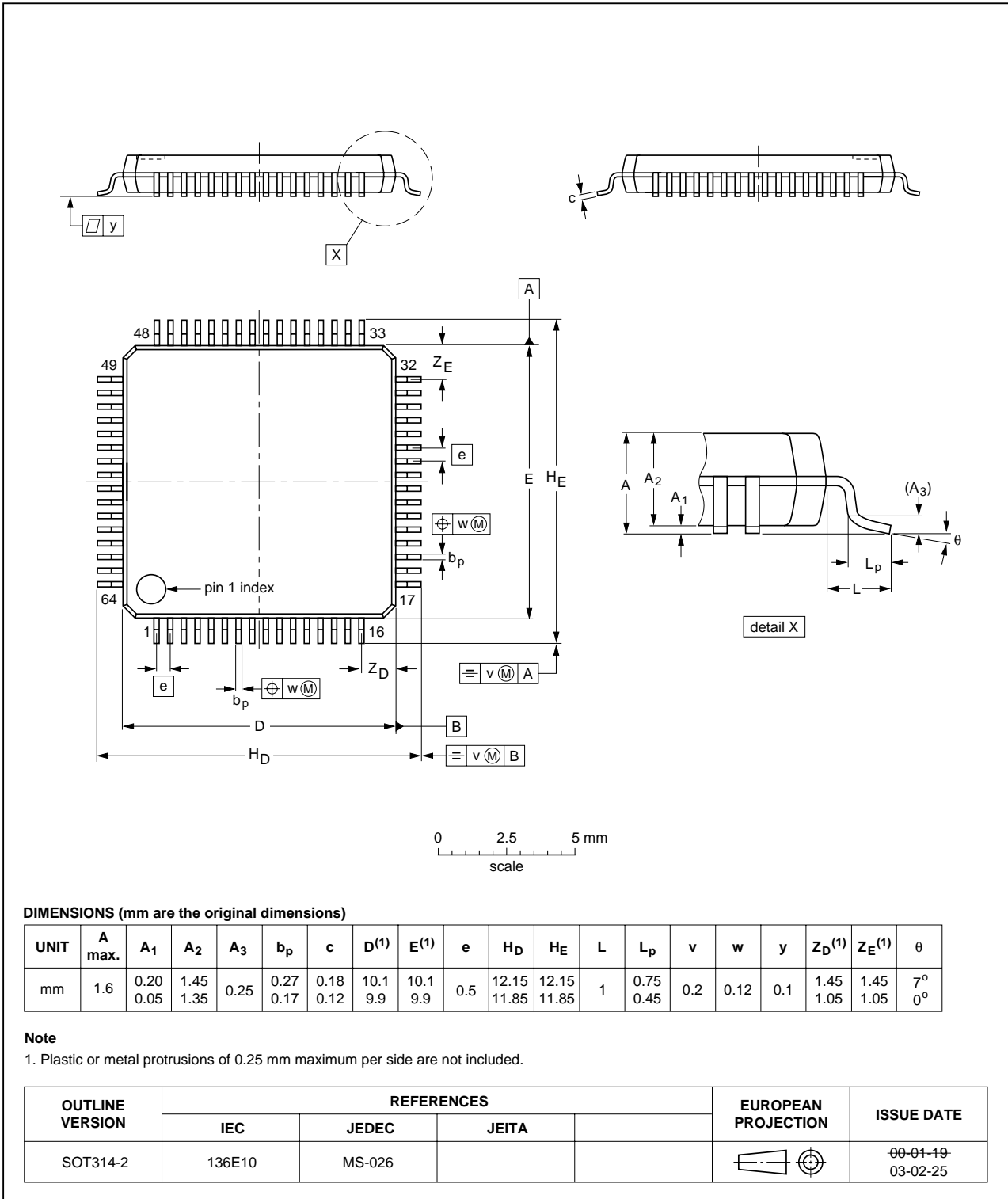LQFP64: plastic low profile quad flat package; 64 leads; body 10 x 10 x 1.4 mm   SOT314-2

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	H_D	H_E	L	L_p	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.6	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.12	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT314-2	136E10	MS-026				00-01-19 03-02-25

Fig 26. Package outline PCF8579H/1 (LQFP64)

PCF8579_5

Product data sheet   Rev. 05 — 11 May 2009   34 of 41

TQFP64: plastic thin quad flat package; 64 leads; body 10 x 10 x 1.0 mm

SOT357-1

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A₁	A₂	A₃	bₚ	c	D(1)	E(1)	e	H_D	H_E	L	Lₚ	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.2	0.15 0.05	1.05 0.95	0.25	0.27 0.17	0.18 0.12	10.1 9.9	10.1 9.9	0.5	12.15 11.85	12.15 11.85	1	0.75 0.45	0.2	0.08	0.1	1.45 1.05	1.45 1.05	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT357-1	137E10	MS-026				~~00-01-19~~ 02-03-14

Fig 27. Package outline PCF8579HT/1 (TQFP64)

PCF8579_5

14. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

14.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

14.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

14.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

14.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 28) than a SnPb process, thus reducing the process window

- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board

- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 17 and 18

Table 17. SnPb eutectic process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 18. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 28.

PCF8579_5

Product data sheet

Rev. 05 — 11 May 2009

37 of 41

MSL: Moisture Sensitivity Level

Fig 28. Temperature profiles for large and small components
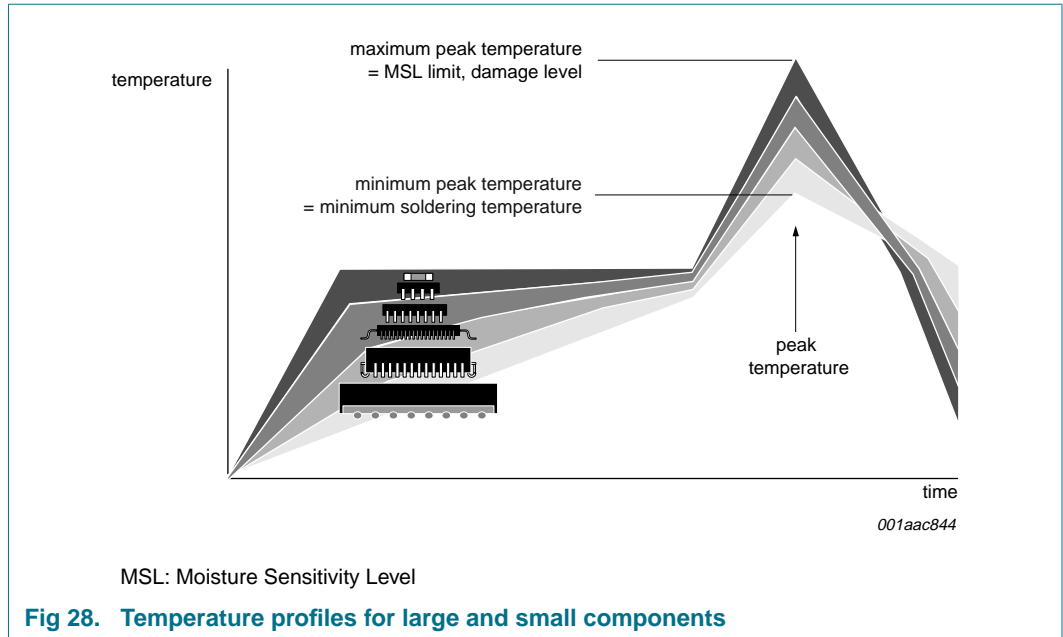
For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

15. Abbreviations

Table 19. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
DC	Direct Current
I^{2}C	Inter-Integrated Circuit
IC	Integrated Circuit
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MSB	Most Significant Bit
MSL	Moisture Sensitivity Level
PCB	Printed-Circuit Board
POR	Power-On Reset
RC	Resistance-Capacitance
RAM	Random Access Memory
RMS	Root Mean Square
SCL	Serial Clock Line
SDA	Serial Data Line
SMD	Surface Mount Device

PCF8579_5

Product data sheet Rev. 05 — 11 May 2009 38 of 41

16. Revision history

Table 20. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8579_5	20090511	Product data sheet	-	PCF8579_4
Modifications:	- The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. - Legal texts have been adapted to the new company name where appropriate. - Added package type TQFP64 - Removed bare die types - Rearranged information in data sheet - Changed letter symbols to NXP approved symbols - Added RAM addressing scheme (Figure 15) - Added addressing example (Table 16)			
PCF8579_4	20030901	Product data sheet	-	PCF8579_3
PCF8579_3	19970401	Product data sheet	-	PCF8579_2
PCF8579_2	19961025	Product data sheet	-	PCF8579_1
PCF8579_1	19940125	Product data sheet	-	-

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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19. Contents