Peregrine Semiconductor

Product Specification

PE4259

SPDT High Power UltraCMOS®
10 MHz–3.0 GHz RF Switch

Features

- Single-pin or complementary CMOS logic control inputs
- Low insertion loss:
  - 0.35 dB @ 1000 MHz
  - 0.5 dB @ 2000 MHz
- Isolation of 30 dB @ 1000 MHz
- High ESD tolerance of 2 kV HBM
- Typical input 1 dB compression point of +33.5 dBm
- 1.8V minimum power supply voltage
- Ultra-small SC-70 package

Product Description

The PE4259 UltraCMOS® RF switch is designed to cover a broad range of applications from 10 MHz through 3000 MHz. This reflective switch integrates on-board CMOS control logic with a low voltage CMOS-compatible control interface, and can be controlled using either single-pin or complementary control inputs. Using a nominal +3-volt power supply voltage, a typical input 1dB compression point of +33.5 dBm can be achieved.

The PE4259 is manufactured on Peregrine's UltraCMOS process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

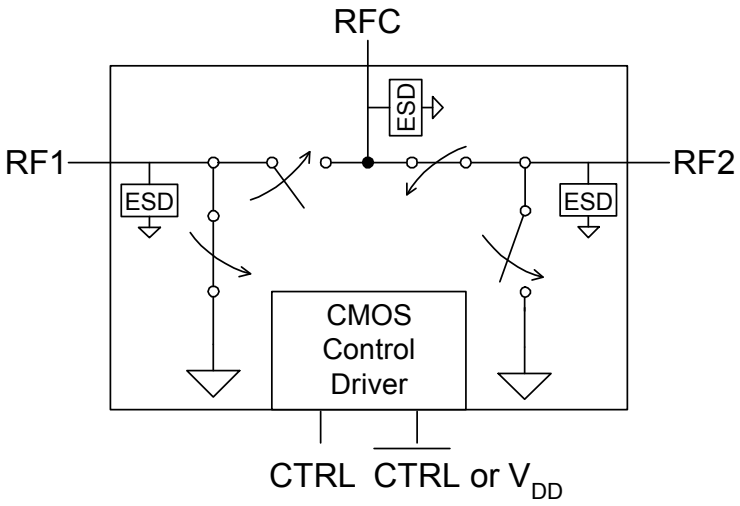

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Figure 2. Package Type SC-70
6-lead SC-70

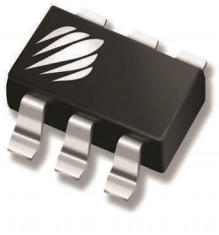


Table 1. Electrical Specifications @ +25 °C, V_{DD} = 3V ($Z_S = Z_L = 50\Omega$)

Parameter	Condition	Minimum	Typical	Maximum	Unit
Operation frequency[1]		10		3000	MHz
Insertion loss[3]	1000 MHz 2000 MHz		0.35 0.50	0.45 0.60	dB dB
Isolation	1000 MHz 2000 MHz	29 19	30 20		dB dB
Return loss[3]	1000 MHz 2000 MHz	21 24	22 27		dB dB
'ON' switching time	50% CTRL to 0.1 dB of final value, 1 GHz		1.50		us
'OFF' switching time	50% CTRL to 25 dB isolation, 1 GHz		1.50		us
Video feedthrough[2]			15		mV_{pp}
Input 1dB compression point	1000 MHz @ 2.3–3.3V 1000 MHz @ 1.8–2.3V 2500 MHz @ 2.3–3.3V 2500 MHz @ 1.8–2.3V	31.5 29.5 28.5 28	33.5 30.5 30.5 29		dBm dBm dBm dBm
Input IP3	1000 MHz, 20 dBm input power		55		dBm

Notes: 1. Device linearity will begin to degrade below 10 MHz.
2. The DC transient at the output of any port of the switch when the control voltage is switched from Low to High or High to Low in a 50Ω test set-up, measured with 1ns risetime pulses and 500 MHz bandwidth.
3. A tuning capacitor must be added to the application board to optimize the insertion loss and return loss performance. See *Figure 6* for details.

Figure 3. Pin Configuration (Top View)

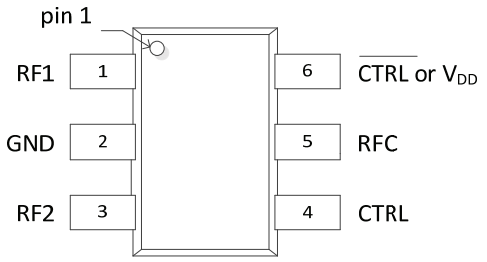


Table 2. Pin Descriptions

Pin No.	Pin Name	Description
1	RF1*	RF port 1.
2	GND	Ground connection. Traces should be physically short and connected to ground plane for best performance.
3	RF2[1]	RF port 2.
4	CTRL	Switch control input, CMOS logic level.
5	RFC[1]	RF common.
6	$\overline{CTRL}$ or V_{DD}	This pin supports two interface options: *Single-pin control mode.* A nominal 3-volt supply connection is required. *Complementary-pin control mode.* A complementary CMOS control signal to CTRL is supplied to this pin. Bypassing on this pin is not required in this mode.

Note: * All RF pins must be DC blocked with an external series capacitor or held at 0 VDC.

Table 3. Operating Ranges

Parameter	Min	Typ	Max	Unit
V_{DD} Power supply voltage	1.8	3.0	3.3	V
I_{DD} Power supply current (V_{DD} = 3V, V_{CNTL} = 3V)		9	20	µA
Control voltage high	0.7x V_{DD}			V
Control voltage low			0.3x V_{DD}	V

Moisture Sensitivity Level

The Moisture Sensitivity Level rating for the PE4259 in the SC70 package is MSL1.

Switching Frequency

The PE4259 has a maximum 25 kHz switching rate.

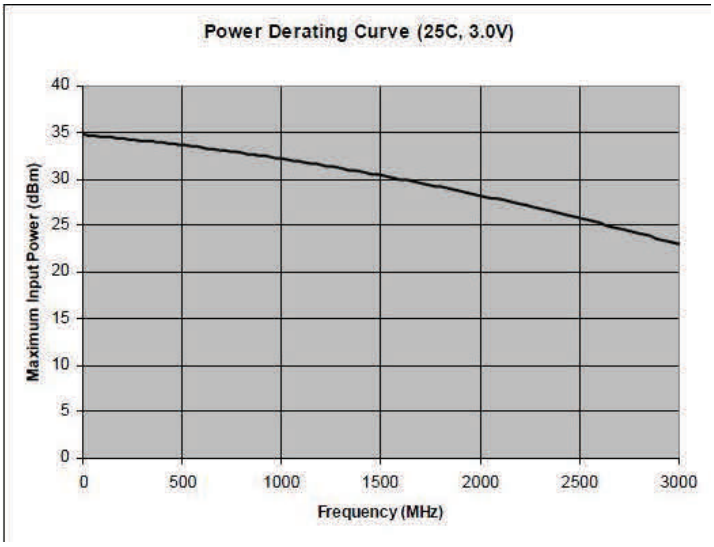
Table 4. Absolute Maximum Ratings

Symbol	Parameter/Condition	Min	Max	Unit
V_{DD}	Power supply voltage	–0.3	4.0	V
V_I	Voltage on any DC input	–0.3	V_{DD}+ 0.3	V
T_{ST}	Storage temperature range	–65	150	°C
T_{OP}	Operating temperature range	–40	85	°C
P_{IN}	Input power (50Ω)		+34*	dBm
V_{ESD}	ESD Voltage (HBM, ML_STD 883 Method 3015.7)		2000	V
	ESD Voltage (MM, JEDEC, JESD22-A114-B)		100	V

Note: * To maintain optimum device performance, do not exceed Max P_{IN} at desired operating frequency (see *Figure 4*).

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Figure 4. Maximum Input Power



Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS devices are immune to latch-up.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Table 5. Single-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = High	RFC to RF1
Pin 6 (V_{DD}) = V_{DD} Pin 4 (CTRL) = Low	RFC to RF2

Table 6. Complementary-pin Control Logic Truth Table

Control Voltages	Signal Path
Pin 6 ($\overline{CTRL}$ or V_{DD}) = Low Pin 4 (CTRL) = High	RFC to RF1
Pin 6 ($\overline{CTRL}$ or V_{DD}) = High Pin 4 (CTRL) = Low	RFC to RF2

Thermal Data

Psi-JT (Ψ_{JT}), junction top-of-package, is a thermal metric to estimate junction temperature of a device on the customer application PCB (JEDEC JESD51-2).

$\Psi_{JT} = (T_J - T_T)/P$

Where

Ψ_{JT} = junction-to-top of package characterization parameter, °C/W

T_J = die junction temperature, °C

T_T = package temperature (top surface, in the center), °C

P = power dissipated by device, Watts

Table 7. Thermal Data

Parameter	Typ	Unit
Maximum junction temperature, T_{JMAX} (RF input power, CW = 31.5 dBm, +85 °C ambient)	99	°C
Ψ_{JT}	37	°C/W
θ_{JA}, junction-to-ambient thermal resistance	104	°C/W

Control Logic Input

The PE4259 is a versatile RF CMOS switch that supports two operating control modes; single-pin control mode and complementary-pin control mode.

Single-pin control mode enables the switch to operate with a single control pin (pin 4) supporting a +3-volt CMOS logic input, and requires a dedicated +3-volt power supply connection on pin 6 (V_{DD}). This mode of operation reduces the number of control lines required and simplifies the switch control interface typically derived from a CMOS μProcessor I/O port.

Complementary-pin control mode allows the switch to operate using complementary control pins CTRL and $\overline{CTRL}$ (pins 4 and 6), that can be directly driven by +3-volt CMOS logic or a suitable μProcessor I/O port. This enables the PE4259 to be used as a potential alternate source for SPDT RF switch products used in positive control voltage mode and operating within the PE4259 operating limits.

Evaluation Kit

The SPDT switch EK Board was designed to ease customer evaluation of Peregrine's PE4259. The RF common port is connected through a 50Ω transmission line via the top SMA connector, J1. RF1 and RF2 are connected through 50Ω transmission lines via SMA connectors J2 and J3, respectively. A through 50Ω transmission is available via SMA connectors J4 and J5. This transmission line can be used to estimate the loss of the PCB over the environmental conditions being evaluated.

The board is constructed of a two metal layer FR4 material with a total thickness of 0.031". The bottom layer provides ground for the RF transmission lines. The transmission lines were designed using a coplanar waveguide with ground plane model using a trace width of 0.0476", trace gaps of 0.030", dielectric thickness of 0.028", metal thickness of 0.0021" and ε_r of 4.4.

J6 and J7 provide a means for controlling DC and digital inputs to the device. J6-1 is connected to the device V_{DD} or $\overline{CTRL}$ input. J7-1 is connected to the device CTRL input.

Figure 5. Evaluation Board Layout

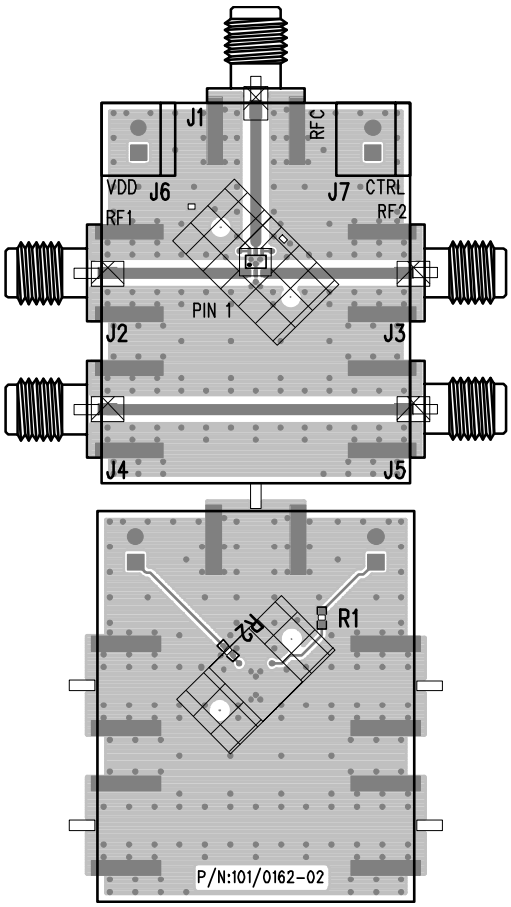


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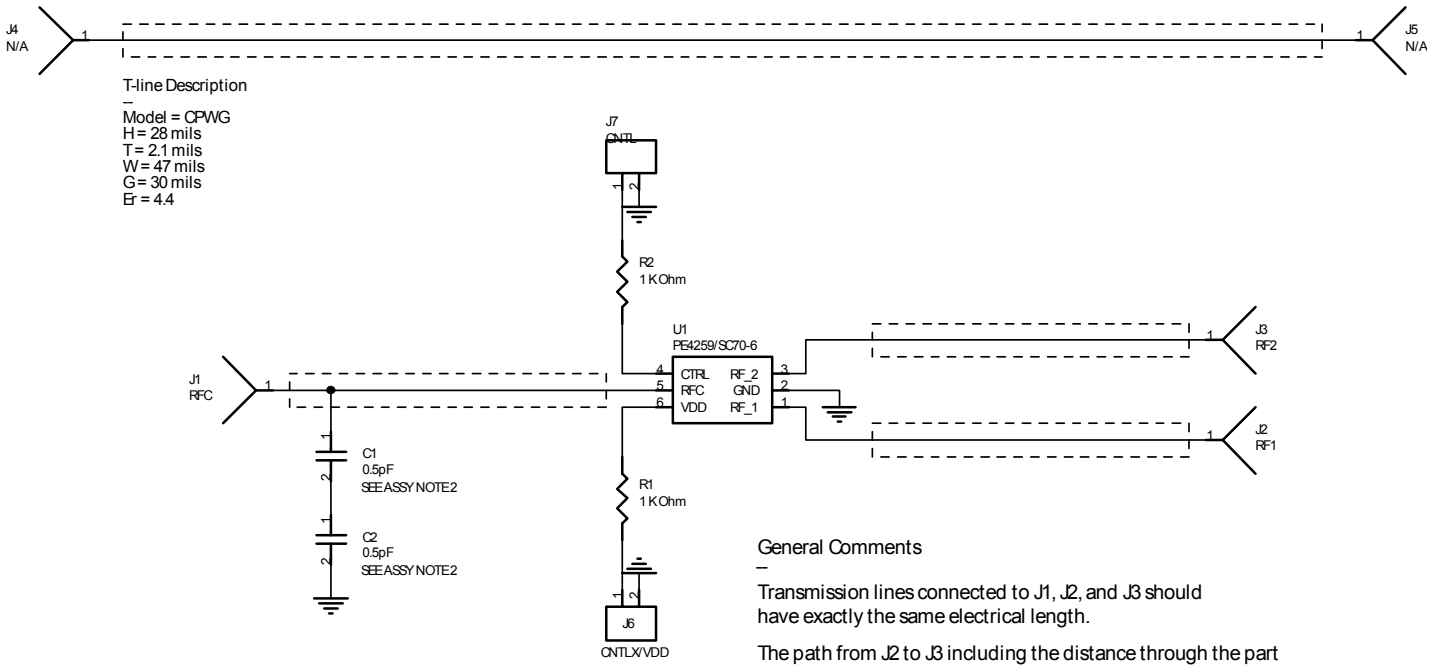
Figure 6. Evaluation Board Schematic



NOTES:

1. USE PCB PART NUMBER 101-0162-02.
2. ADD TWO 0.5PF CAPS IN SERIES TO BE SHUNTED ON THE J1 SMA INPUT.
   SOLDER C1 SIDE 1 TO THE RF TRACE CLOSE TO THE J1 PIN.
   SOLDER C1 SIDE 2 TO C2 SIDE 1.
   SOLDER C2 SIDE 2 TO GROUND.

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Typical Performance Data @ –40 °C to 85 °C (Unless Otherwise Noted)

Figure 7. Insertion Loss

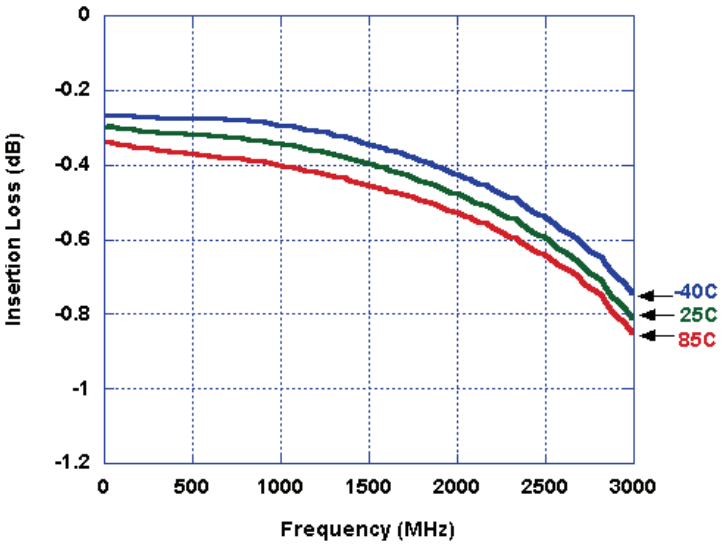


Figure 8. Isolation – Input to Output

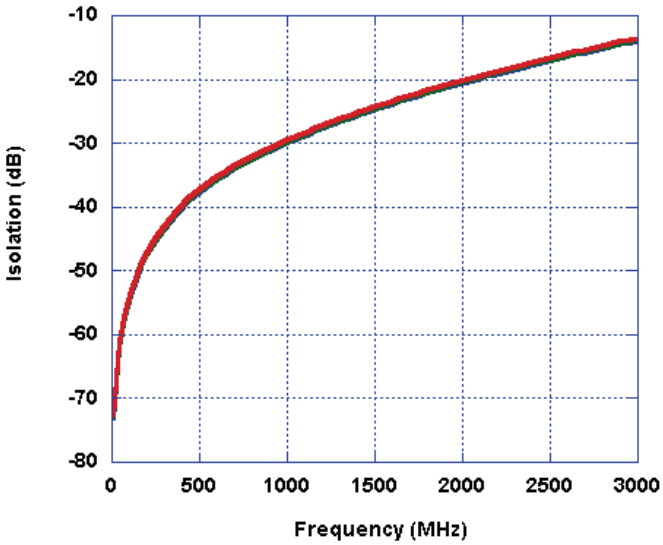


Figure 9. Isolation – Output to Output

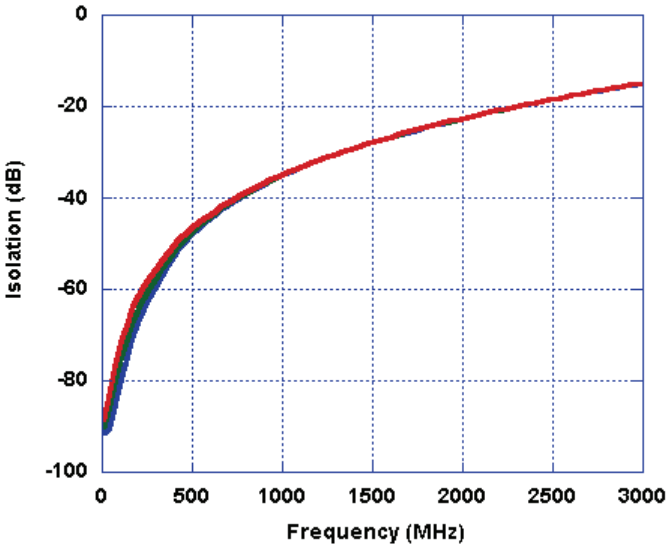
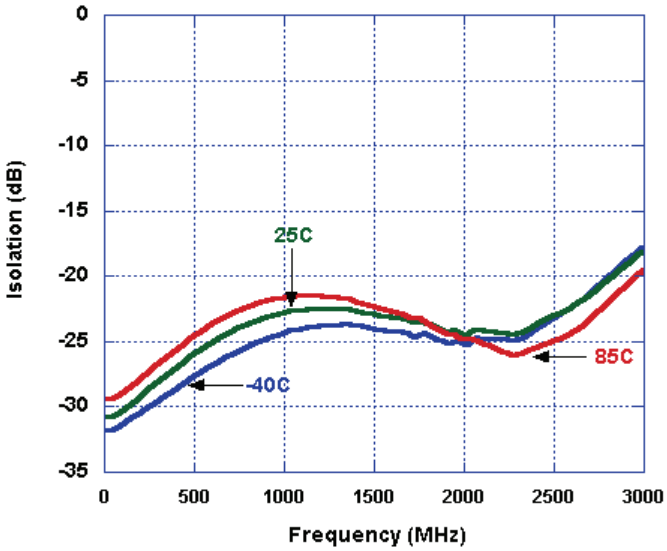


Figure 10. Return Loss (Input)



Typical Performance Data @ V_{DD} = 2.3V, T = 25 °C

Figure 11. Insertion Loss

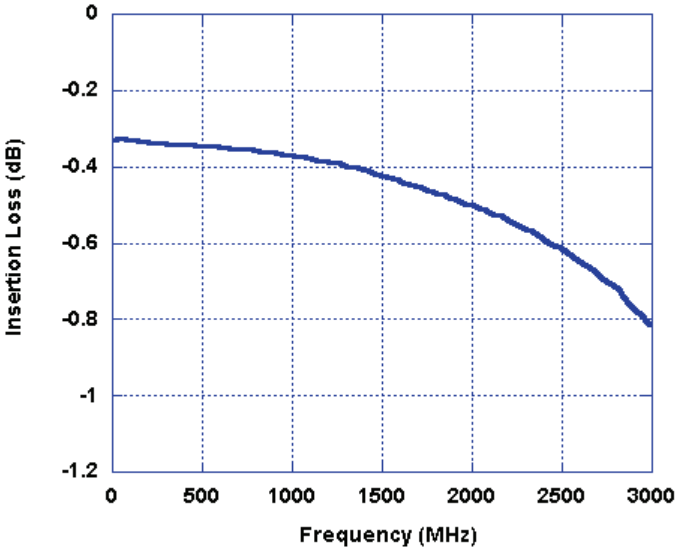


Figure 12. Isolation – Input to Output

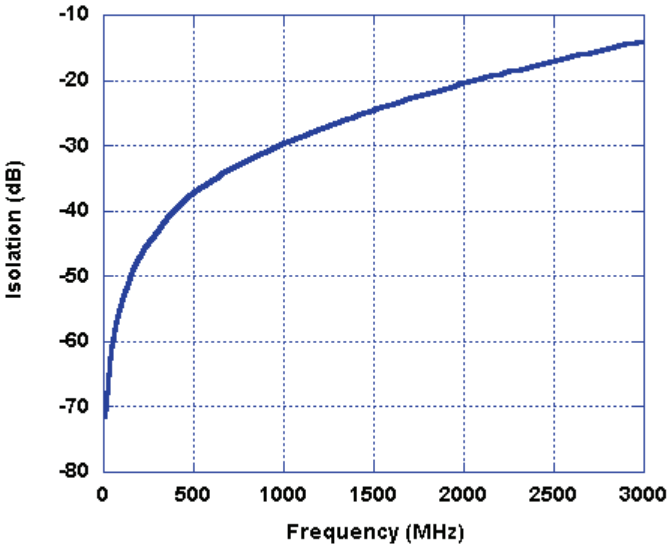


Figure 13. Isolation – Output to Output

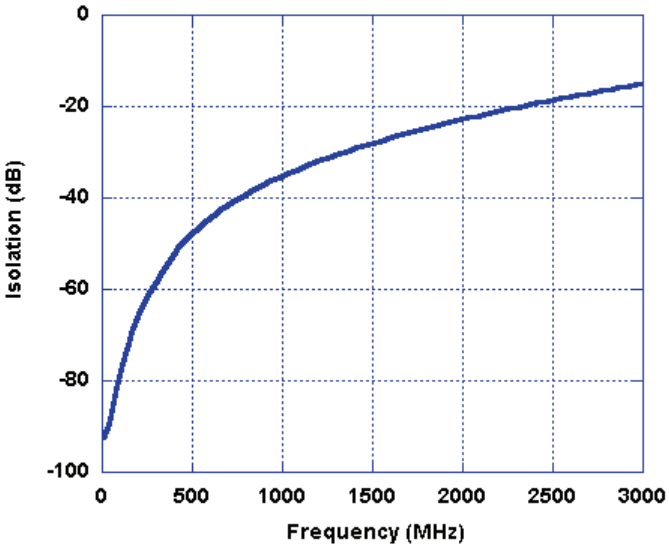


Figure 14. Return Loss (Input and Output)

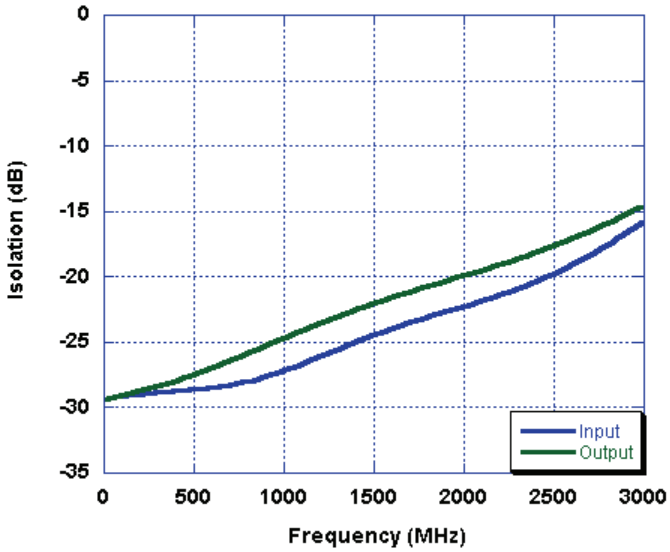


Figure 15. Package Drawing

6-lead SC-70

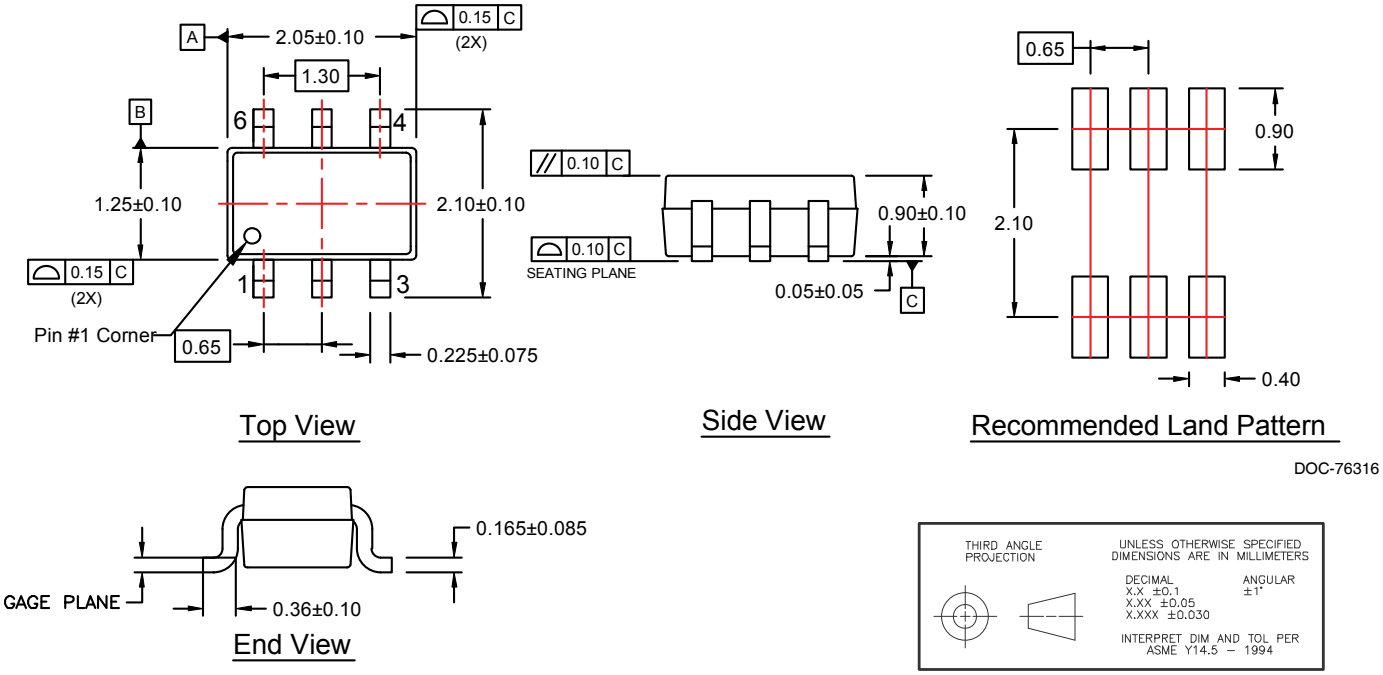
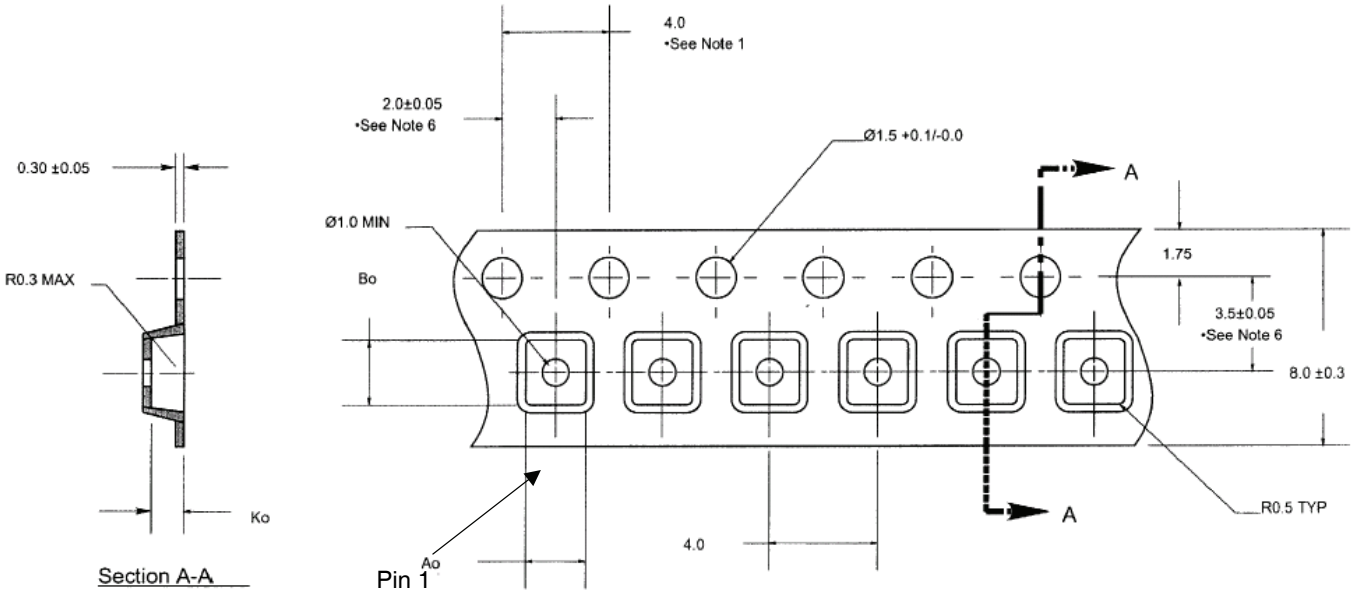


Figure 16. Top Marking Specifications

PRT-50103

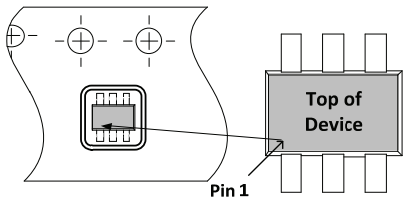
● = Pin 1 Indicator
PPP = Part Number
YWW = Date Code

Figure 16. Tape and Reel Specifications



Notes:
1. 10 sprocket hole pitch cumulative tolerance ±.02.
2. Camber not to exceed 1mm in 100mm.
3. Material: Black Conductive Advantek Polystyrene.
4. Ao and Bo measured on a plane 0.3mm above the bottom of the pocket
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier.
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Ao = 2.25 mm
Bo = 2.4 mm
Ko = 1.2 mm



Device Orientation in Tape

Table 7. Ordering Information

Order Code	Part Marking	Description	Package	Shipping Method
4259-63	259	PE4259G-06SC70-3000C	Green 6-lead SC-70	3000 units / T&R
EK4259-01	PE4259-EK	PE4259-06SC70-EK	Evaluation Kit	1 / Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.