TXS0108E-Q1 Automotive 8-Bit Bi-directional, Level-Shifting, Voltage Translator for Open-Drain and Push-Pull Applications

1 Features

- AEC-Q100 qualified for automotive applications:
  - Device temperature grade 1: –40°C to 125°C
  - Device HBM ESD classification level 2
  - Device CDM ESD classification level C6
- No direction-control signal needed
- Maximum data rates:
  - 110Mbps (push pull)
  - 1.2Mbps (open drain)
- 1.4V to 3.6V on A port and 1.65V to 5.5V on B port ($V_{CCA} \leq V_{CCB}$)
- No power-supply sequencing required – either V_{CCA} or V_{CCB} can be ramped first
- Latch-up performance exceeds 100mA per JESD 78, class II
- ESD protection exceeds JESD 22 (A port):
  - 2000V Human Body Model (A114-B)
  - 150V Machine Model (A115-A)
  - 1000V Charged-Device Model (C101)
- IEC 61000-4-2 ESD (B-port):
  - ± 8kV Contact Discharge
  - ± 6kV Air Discharge

2 Applications

- Automotive

3 Description

This device is an 8-bit non-inverting level translator which uses two separate configurable power-supply rails. The A port tracks the V_{CCA} pin supply voltage. The V_{CCA} pin accepts any supply voltage between 1.4V and 3.6V. The B port tracks the V_{CCB} pin supply voltage. The V_{CCB} pin accepts any supply voltage between 1.65V and 5.5V. Two input supply pins allows for low Voltage bidirectional translation between any of the 1.5V, 1.8V, 2.5V, 3.3V, and 5V voltage nodes.

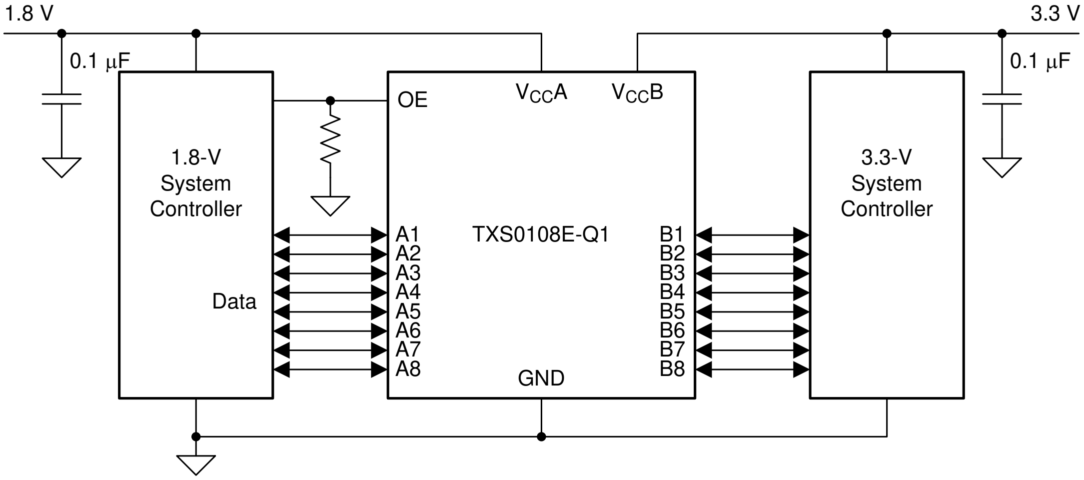
When the output-enable (OE) input is low, all outputs are placed in the high-impedance (Hi-Z) state.

To put the device in the Hi-Z state during power-up or power-down periods, tie OE to GND through a pull-down resistor. The current-sourcing capability of the driver determines the minimum value of the resistor.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
TXS0108E-Q1	PW (TSSOP, 20)	6.50mm × 6.40mm
	RKS (VQFN, 20)	4.5mm x 2.5mm
	DGS (VSSOP, 20)	3.00mm x 5.10mm

(1) For more information, see Section 11
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Simplified Application

Table of Contents

4 Pin Configuration and Functions

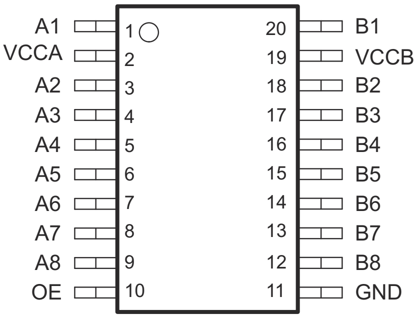


Figure 4-1. PW or DGS Package, 20-Pin TSSOP (Top View)

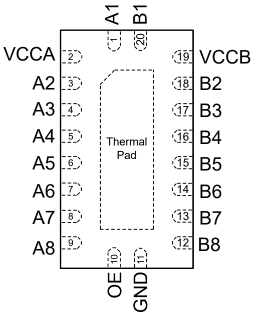


Figure 4-2. RKS Package, 20-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A1	1	I/O	Input/output 1. Referenced to V_{CCA}
A2	3	I/O	Input/output 2. Referenced to V_{CCA}
A3	4	I/O	Input/output 3. Referenced to V_{CCA}
A4	5	I/O	Input/output 4. Referenced to V_{CCA}
A5	6	I/O	Input/output 5. Referenced to V_{CCA}
A6	7	I/O	Input/output 6. Referenced to V_{CCA}
A7	8	I/O	Input/output 7. Referenced to V_{CCA}
A8	9	I/O	Input/output 8. Referenced to V_{CCA}
B1	20	I/O	Input/output 1. Referenced to V_{CCB}
B2	18	I/O	Input/output 2. Referenced to V_{CCB}
B3	17	I/O	Input/output 3. Referenced to V_{CCB}
B4	16	I/O	Input/output 4. Referenced to V_{CCB}
B5	15	I/O	Input/output 5. Referenced to V_{CCB}
B6	14	I/O	Input/output 6. Referenced to V_{CCB}
B7	13	I/O	Input/output 7. Referenced to V_{CCB}
B8	12	I/O	Input/output 8. Referenced to V_{CCB}
GND	11	–	Ground
OE	10	I	3-state output-mode enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}.
VCCA	2	–	A-port supply voltage. $1.4V \le V_{CCA} \le 3.6V$, $V_{CCA} \le V_{CCB}$.
VCCB	19	–	B-port supply voltage. $1.65V \le V_{CCB} \le 5.5V$.

(1) I = input, O = output

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage, V_{CCA}		–0.5	4.6	V
Supply voltage, V_{CCB}		–0.5	6.5	V
Input voltage, V_I (2)	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high-impedance or power-off state, V_O (2)	A port	–0.5	4.6	V
	B port	–0.5	6.5	
Voltage applied to any output in the high or low state, V_O (2) (3)	A port	–0.5	$V_{CCA} + 0.5$	V
	B port	–0.5	$V_{CCB} + 0.5$	V
Input clamp current, I_{IK}	$V_I < 0$		–50	mA
Output clamp current, I_{OK}	$V_O < 0$		–50	mA
Continuous output current, I_O		–50	50	mA
Continuous current through V_{CCA}, V_{CCB}, or GND		–100	100	mA
Junction temperature, T_J			150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input and output negative Voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		IEC 61000-4-2 ESD (B-Port) Contact Discharge	±8000	
		IEC 61000-4-2 ESD (B-Port) Air Gap Discharge	±6000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2)

					MIN	MAX	UNIT
V_{CCA}	Supply voltage[3]				1.4	3.6	V
V_{CCB}	Supply voltage[3]				1.65	5.5	V
V_{IH}	High-level input voltage	A-Port I/Os	V_{CCA} (V) = 1.4 to 1.95	V_{CCB} (V) = 1.65 to 5.5	V_{CCI} – 0.2	V_{CCI}	V
			V_{CCA} (V) = 1.95 to 3.6	V_{CCB} (V) = 1.65 to 5.5	V_{CCI} – 0.4	V_{CCI}	
		B-Port I/Os	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	V_{CCI} – 0.4	V_{CCI}	V
		OE	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	V_{CCA} × 0.65	5.5	V
V_{IL}	Low-level input voltage	A-Port I/Os	V_{CCA} (V) = 1.4 to 1.95	V_{CCB} (V) = 1.65 to 5.5	0	0.15	V
			V_{CCA} (V) = 1.95 to 3.6	V_{CCB} (V) = 1.65 to 5.5	0	0.15	
		B-Port I/Os	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	0	0.15	V
		OE	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5	0	V_{CCA} × 0.35	V
Δt/Δv	Input transition rise or fall rate	A-Port I/Os Push-pull	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5		10	ns/V
		B-Port I/Os Push-pull	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5		10	ns/V
		Control input	V_{CCA} (V) = 1.4 to 3.6	V_{CCB} (V) = 1.65 to 5.5		10	ns/V
T_A	Operating free-air temperature				–40	125	°C

(1) V_{CCI} is the V_{CC} associated with the data input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6V.

5.4 Thermal Information

THERMAL METRIC (1)		TXS0108E-Q1		UNIT
		PW (TSSOP)	RKS (VQFN)	
		20 PINS	20 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	88.9	54.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	32.9	54.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	50.9	27.8	
Ψ_{JT}	Junction-to-top characterization parameter	1.4	2.9	
Ψ_{JB}	Junction-to-board characterization parameter	50.5	27.7	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	11.5	

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics: T_A = –40°C to 125°C

over recommended operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS	V_{CCA} (V)	V_{CCB} (V)	T_A = 25°C			T_A = –40°C to 125°C		UNIT
					MIN	TYP	MAX	MIN	MAX	
V_{OHA}	Port A output high voltage	I_{OH} = –20μA, $V_{IB} \geq V_{CCB} - 0.4V$	1.4 to 3.6	1.65 to 5.5				$V_{CCA} \times 0.67$		V
V_{OLA}	Port A output low voltage	I_{OL} = 180μA, $V_{IB} \leq 0.15V$	1.4	1.65 to 5.5					0.4	V
		I_{OL} = 220μA, $V_{IB} \leq 0.15V$	1.65	1.65 to 5.5					0.4	
		I_{OL} = 300μA, $V_{IB} \leq 0.15V$	2.3	1.65 to 5.5					0.4	
		I_{OL} = 400μA, $V_{IB} \leq 0.15V$	3	1.65 to 5.5					0.55	
V_{OHB}	Port B output high voltage	I_{OH} = –20μA, $V_{IA} \geq V_{CCA} - 0.2V$	1.4 to 3.6	1.65 to 5.5				$V_{CCB} \times 0.67$		V
V_{OLB}	Port B output low voltage	I_{OL} = 220μA, $V_{IA} \leq 0.15V$	1.4 to 3.6	1.65					0.4	V
		I_{OL} = 300μA, $V_{IA} \leq 0.15V$	1.4 to 3.6	2.3					0.4	
		I_{OL} = 400μA, $V_{IA} \leq 0.15V$	1.4 to 3.6	3					0.55	
		I_{OL} = 620μA, $V_{IA} \leq 0.15V$	1.4 to 3.6	4.5					0.55	
I_I	Input leakage current	OE: $V_I = V_{CCI}$ or GND	1.4	1.65 to 5.5	–1		1		2	μA
I_{OZ}	High-impedance state output current	A or B port	1.4	1.65 to 5.5	–1		1	–2	2	μA
I_{CCA}	V_{CCA} supply current	$V_I = V_O$ = Open, I_O = 0	1.4 to 3.6	2.3 to 5.5					2	μA
			3.6	0					2	
			0	5.5					–1	
I_{CCB}	V_{CCB} supply current	$V_I = V_O$ = Open, I_O = 0	1.4 to 3.6	2.3 to 5.5					6	μA
			3.6	0					–1	
			0	5.5					1.5	
I_{CCA} + I_{CCB}	Combined supply current	$V_I = V_{CCI}$ or GND, I_O = 0	1.4 to 3.6	2.3 to 5.5					8	μA
I_{CCZA}	High-impedance state V_{CCA} supply current	$V_I = V_O$ = Open, I_O = 0, OE = GND	1.4 to 3.6	1.65 to 5.5					2	μA
I_{CCZB}	High-impedance state V_{CCB} supply current	$V_I = V_O$ = Open, I_O = 0, OE = GND	1.4 to 3.6	1.65 to 5.5					6	μA
C_i	Input capacitance	OE	3.3	3.3		4.5			6.75	pF
C_{io}	Input-to-output internal capacitance	A port	3.3	3.3		6			7.6	pF
		B port	3.3	3.3		5.5			6.9	

---

(1) V_{CCO} is the V_{CC} associated with the output port.
(2) V_{CCI} is the V_{CC} associated with the input port.
(3) V_{CCA} must be less than or equal to V_{CCB}, and V_{CCA} must not exceed 3.6V.

5.6 Timing Requirements: V_{CCA} = 1.5V ± 0.1 V

over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (unless otherwise noted)

				$V_{CC B}$ = 1.8V ± 0.15V		$V_{CC B}$ = 2.5V ± 0.2V		$V_{CC B}$= 3.3V ± 0.3V		$V_{CC B}$= 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull			40		60		60		60	Mbps
		Open-drain			0.8		0.8		1		1	
t_w	Pulse duration	Data inputs	Push-pull	25		16.7		16.7		16.7		ns
			Open-drain	1250		1250		1000		1000		

5.7 Timing Requirements: V_{CCA} = 1.8V ± 0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (unless otherwise noted)

				$V_{CC B}$ = 1.8V ± 0.15V		$V_{CC B}$ = 2.5V ± 0.2V		$V_{CC B}$= 3.3V ± 0.3V		$V_{CC B}$= 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull			45		65		70		70	Mbps
		Open-drain			0.8		0.8		0.8		1	
t_w	Pulse duration	Data inputs	Push-pull	22.2		15.3		15.3		15.3		ns
			Open-drain	1250		1250		1250		1000		

5.8 Timing Requirements: V_{CCA} = 2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (unless otherwise noted)

				V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
	Data rate	Push-pull			80		95		100	Mbps
		Open-drain			0.8		0.8		1	
t_w	Pulse duration	Data inputs	Push-pull	12.5		10.5		10		ns
			Open-drain	1250		1250		1000		

5.9 Timing Requirements: V_{CCA} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (unless otherwise noted)

				V_{CCB} = 3.3V ± 0.3V		V_{CC} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	
	Data rate	Push-pull			100		110	Mbps
		Open-drain			0.8		1.2	
t_w	Pulse duration	Data inputs	Push-pull	10		9.1		ns
			Open-drain	1250		833		

5.10 Switching Characteristics: V_{CCA} = 1.5V ± 0.1V

over recommended operating free-air temperature range, V_{CCA} = 1.5V ± 0.1V (unless otherwise noted)

PARAMETER		TEST CONDITIONS		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		11		9.2		8.6		8.6	ns
			Open-drain driving	2.5	14.4	2	12.8	2	12.2	1.9	12	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		12		10		9.8		9.7	
			Open-drain driving	0.9	720	0.9	554	1	473	1.5	384	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		12.7		11.1		11		12	ns
			Open-drain driving	3.4	13.2	2.6	9.6	2.3	8.5	2	7.5	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		9.5		6.2		5.1		4.2	
			Open-drain driving		745		603		519		407	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		480		480		480		480	ns
t_{dis}	Disable time	OE-to-A or B			400		400		400		400	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	3	13.1	2.4	9.8	2	9	2	8.9	ns
			Open-drain driving	220	982	180	716	140	592	100	481	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	2.6	11.4	1.6	7.4	1	6	0.7	5	ns
			Open-drain driving	220	1020	150	756	100	653	40	370	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	ns
			Open-drain driving	2.4	10	1.8	8.2	1.7	9	1.5	9.15	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	2	8.7	1.3	5.5	1	3.8	1	3.1	
			Open-drain driving	2	11.5	1.3	8.6	1	9.6	1	7.7	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns

5.11 Switching Characteristics: V_{CCA} = 1.8V ± 0.15V

over recommended operating free-air temperature range, V_{CCA} = 1.8V ± 0.15V (unless otherwise noted)

PARA-METER		TEST CONDITIONS		V_{CCB} = 1.8V ± 0.15V		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		8.2		6.4		5.7		5.6	ns
			Open-drain driving	2.1	11.4	1.7	9.9	1.6	9.3	1.5	8.9	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		9		5.6		6.5		6.3	
			Open-drain driving	0.15	729	0.2	584	0.3	466	0.3	346	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		9.8		8		7.4		7	ns
			Open-drain driving	3.19	12.1	2	8.5	1.9	7.3	1.8	6.2	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		10.2		7		5.8		5	
			Open-drain driving		733		578		459		323	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		350		350		350		350	ns
t_{dis}	Disable time	OE-to-A or B	Push-pull driving		410		410		410		410	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	2.7	11.9	2	8.6	1.9	7.8	1.8	7.4	ns
			Open-drain driving	250	996	200	691	150	508	110	365	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	2.5	10.5	1.7	7.4	1.1	5.3	60	4.7	ns
			Open-drain driving	250	1001	170	677	120	546	32	323	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	2.1	8.8	1.6	7.1	1.4	6.8	1.4	6.06	ns
			Open-drain driving	2.2	9	1.7	7.2	1.4	6.8	1.2	6.1	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	2	8.3	1.3	5.4	0.9	3.9	0.7	3	
			Open-drain driving	2	10.5	1	10.7	1	9.6	0.6	7.8	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1		1	ns

5.12 Switching Characteristics: V_{CCA} = 2.5V ± 0.2V

over recommended operating free-air temperature range, V_{CCA} = 2.5V ± 0.2V (unless otherwise noted)

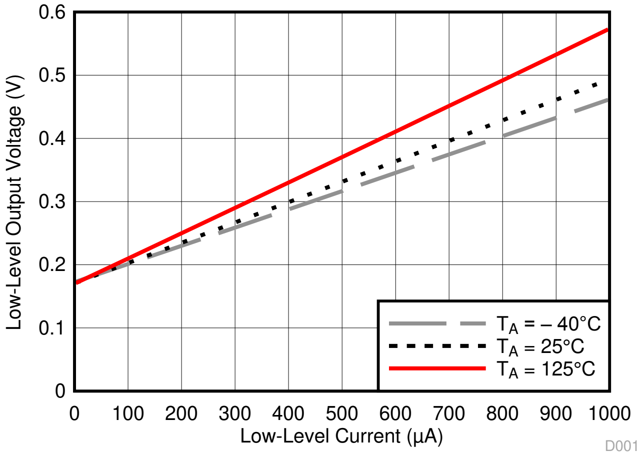
PARA-METER		TEST CONDITIONS		V_{CCB} = 2.5V ± 0.2V		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		5		4		3.7	ns
			Open-drain driving		6.2		6.3		5.8	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		5.2		4.3		3.9	
			Open-drain driving		592		488		368	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		5.4		4.7		4.2	ns
			Open-drain driving		7.3		6		4.9	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		5.9		4.4		3.5	
			Open-drain driving		595		381		345	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		200		200		200	ns
t_{dis}	Disable time	OE-to-A or B			400		400		400	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	1.89	7.3	1.6	6.4	1.5	5.8	ns
			Open-drain driving	110.00	692	157	529	116	377	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	1.70	6.5	1.3	5.1	0.9	4.32	ns
			Open-drain driving	107.00	693	140	483	77	304	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	1.50	5.7	1.2	4.7	1.3	3.8	ns
			Open-drain driving	1.50	5.6	1.2	4.7	1.1	4.2	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	1.40	5.4	0.9	4.1	0.7	3	
			Open-drain driving	0.40	14.2	0.5	19.4	0.4	3	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1		1	ns

5.13 Switching Characteristics: V_{CCA} = 3.3V ± 0.3V

over recommended operating free-air temperature range, V_{CCA} = 3.3V ± 0.3V (unless otherwise noted)

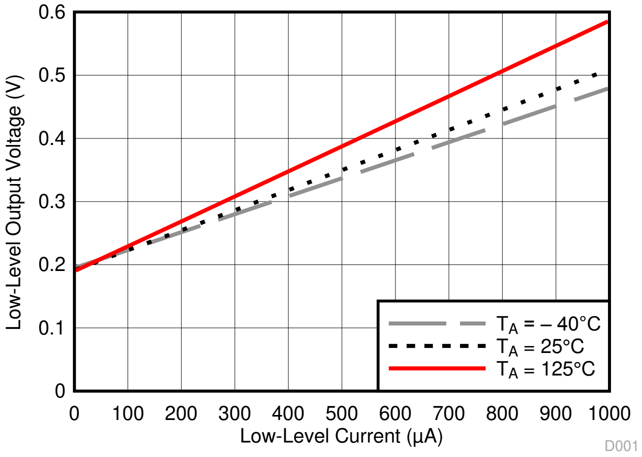
PARAMETER		TEST CONDITION (DRIVING)		V_{CCB} = 3.3V ± 0.3V		V_{CCB} = 5V ± 0.5V		UNIT
				MIN	MAX	MIN	MAX	
t_{PHL}	Propagation delay time high-to-low output	A-to-B	Push-pull driving		3.8		3.28	ns
			Open-drain driving		5.3		4.8	
t_{PLH}	Propagation delay time low-to-high output	A-to-B	Push-pull driving		3.9		3.5	
			Open-drain driving		439		352	
t_{PHL}	Propagation delay time high-to-low output	B-to-A	Push-pull driving		4.2		3.8	ns
			Open-drain driving		5.5		4.5	
t_{PLH}	Propagation delay time low-to-high output	B-to-A	Push-pull driving		4.32		4.3	
			Open-drain driving		449		339	
t_{en}	Enable time	OE-to-A or B	Push-pull driving		200		200	ns
t_{dis}	Disable time	OE-to-A or B	Push-pull driving		400		400	ns
t_{rA}	Input rise time	A-port rise time	Push-pull driving	1.5	5.7	1.4	5	ns
			Open-drain driving	129	446	99.6	337	
t_{rB}	Input rise time	B-port rise time	Push-pull driving	1.35	5	1	4.24	ns
			Open-drain driving	129	427	77	290	
t_{fA}	Input fall time	A-port fall time	Push-pull driving	1.4	4.5	1.3	3.5	ns
			Open-drain driving	1.4	4.4	1.2	3.7	
t_{fB}	Input fall time	B-port fall time	Push-pull driving	1.3	4.2	1.1	3.1	
			Open-drain driving	1.3	4.2	1.1	3.1	
$t_{SK(O)}$	Skew (time), output	Channel-to-channel skew	Push-pull driving		1		1	ns

5.14 Typical Characteristics



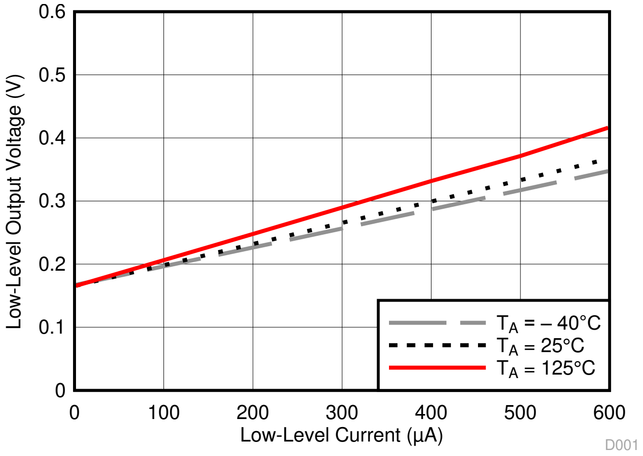
V_{CCA} = 2.3V V_{CCB} = 2.7V $V_{IL(A)}$ = 0.15V

Figure 5-1. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



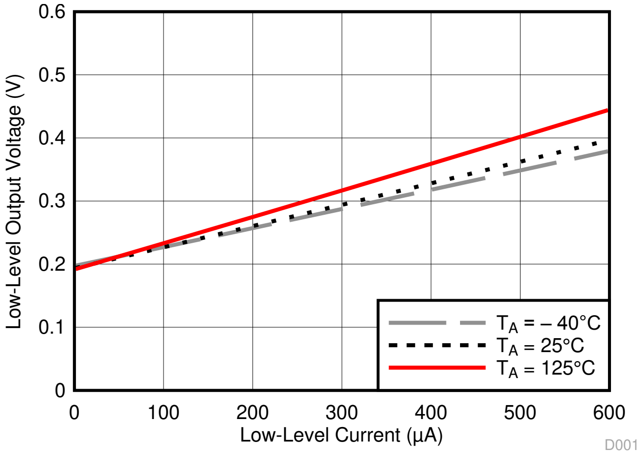
V_{CCA} = 3V V_{CCB} = 5.5V $V_{IL(A)}$ = 0.15V

Figure 5-2. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



V_{CCA} = 1.65V V_{CCB} = 1.95V $V_{IL(A)}$ = 0.15V

Figure 5-3. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)



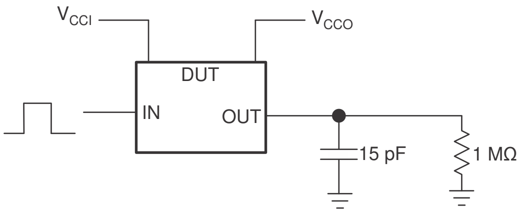
V_{CCA} = 1.65V V_{CCB} = 5.5V $V_{IL(A)}$ = 0.15V

Figure 5-4. Low-Level Output Voltage ($V_{OL(Bx)}$) vs Low-Level Current ($I_{OL(Bx)}$)

6 Parameter Measurement Information

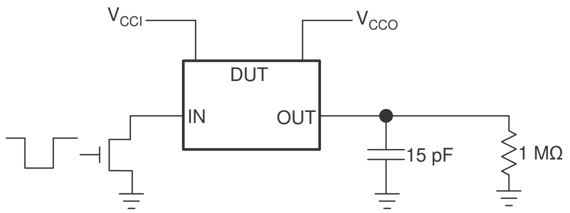
6.1 Load Circuits

Figure 6-1 shows the push-pull driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time. Figure 6-2 shows the open-drain driver circuit used for measuring data rate, pulse duration, propagation delay, output rise-time and fall-time.



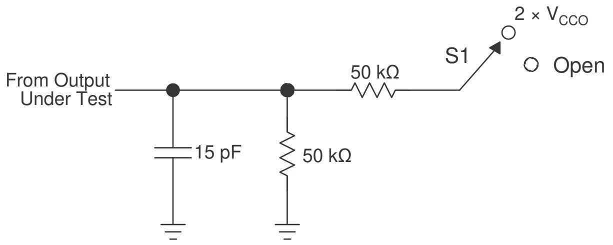
A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-1. Data Rate, Pulse Duration, Propagation Delay, Output Rise-Time And Fall-Time Measurement Using a Push-Pull Driver



A. V_{CCI} is the V_{CC} associated with the input port.
B. V_{CCO} is the V_{CC} associated with the output port.

Figure 6-2. Data Rate (10pF), Pulse Duration (10pF), Propagation Delay, Output Rise-Time And Fall-Time Measurement Using an Open-Drain Driver



TEST	S1
t_{PZL}, t_{PLZ} (t_{dis})	2 × V_{CCO}
t_{PHZ}, t_{PZH} (t_{en})	Open

A. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
B. t_{PZL} and t_{PZH} are the same as t_{en}.

Figure 6-3. Load Circuit for Enable-Time and Disable-Time Measurement

6.2 Voltage Waveforms

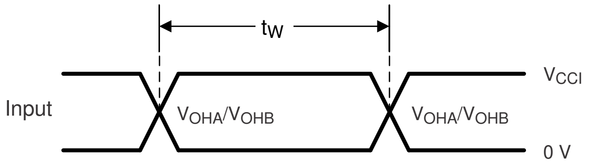


Figure 6-4. Pulse Duration (Push-Pull)

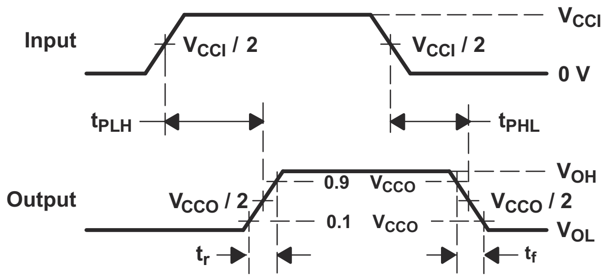
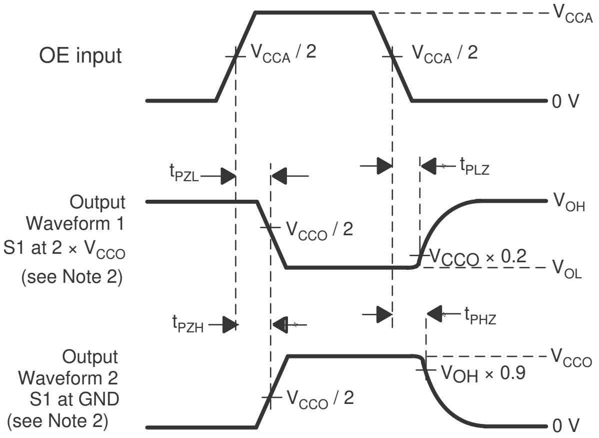


Figure 6-5. Propagation Delay Times



- C_L includes probe and jig capacitance.
- Waveform 1 in Figure 6-6 is for an output with internal such that the output is high, except when OE is high (see Figure 6-3). Waveform 2 in Figure 6-6 is for an output with conditions such that the output is low, except when OE is high.
- All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, dv/dt ≥ 1V/ns.
- The outputs are measured one at a time, with one transition per measurement.
- t_{PLZ} and t_{PHZ} are the same as t_{dis}.
- t_{PZL} and t_{PZH} are the same as t_{en}.
- t_{PLH} and t_{PHL} are the same as t_{pd}.
- V_{CCI} is the V_{CC} associated with the input port.
- V_{CCO} is the V_{CC} associated with the output port.

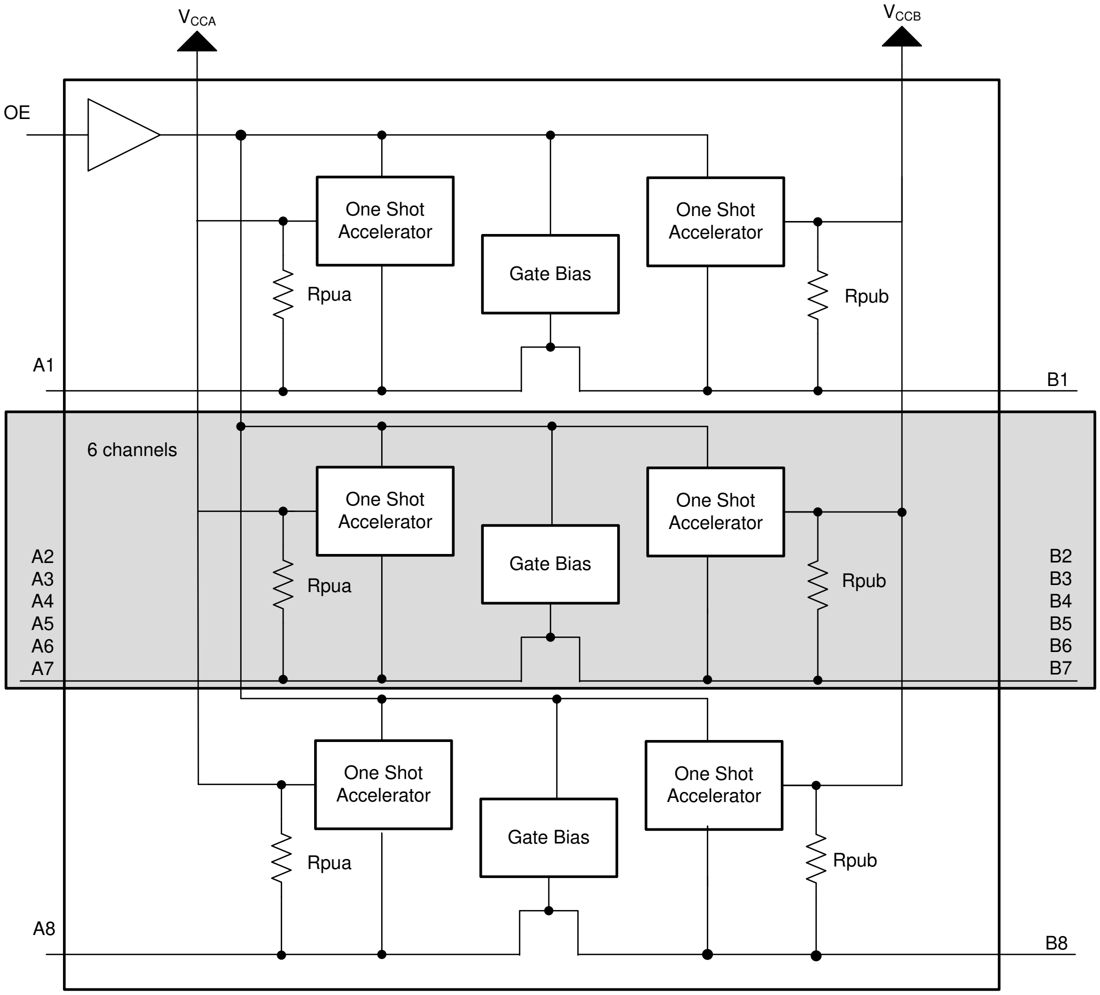
Figure 6-6. Enable and Disable Times

7 Detailed Description

7.1 Overview

The TXS0108E-Q1 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.4V to 3.6V. The B-port accepts I/O voltages from 1.65V to 5.5V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

7.2 Functional Block Diagram



Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low.

7.3 Feature Description

7.3.1 Architecture

Figure 7-1 shows semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300Ω to 500Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design does not need a direction-control signal to control the direction of data flow from A to B or from B to A. The resulting implementation supports both low-speed open-drain operation as well as high-speed push-pull operation.

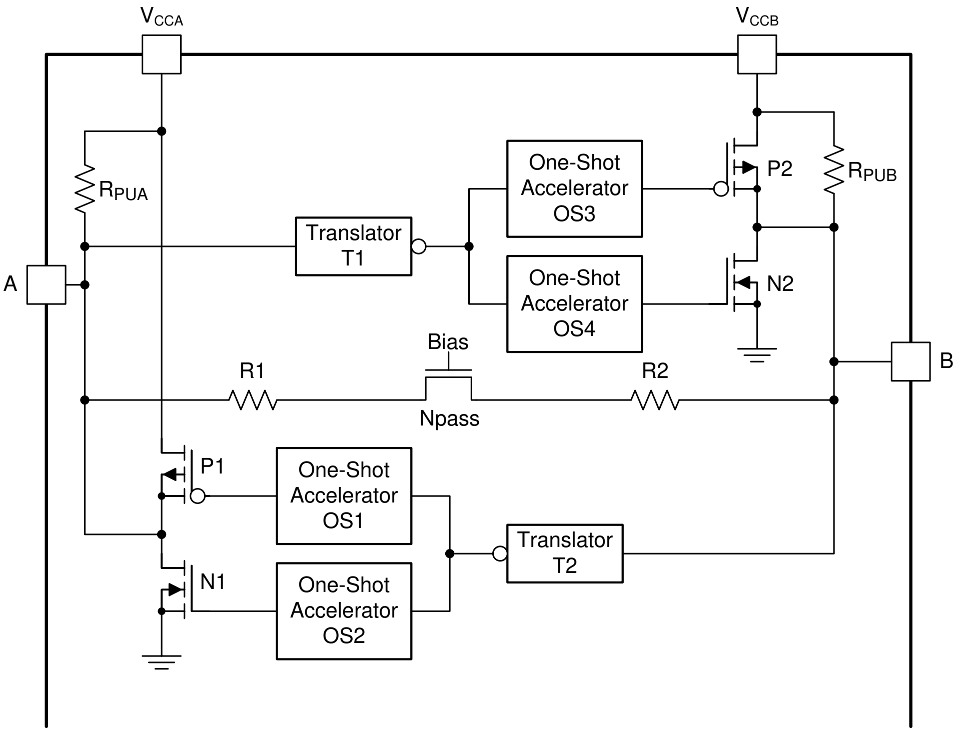


Figure 7-1. Architecture of a TXS0108E-Q1 Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

7.3.2 Input Driver Requirements

The continuous DC-current *sinking* capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the TXS0108E-Q1 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current *sourcing* capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.

The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving TXS0108E-Q1 data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

7.3.3 Output Load Considerations

TI recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and so that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by allowing any reflection to see a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the TXS0108E-Q1 output. Therefore, TI recommends that this lumped-load capacitance is considered to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

7.3.4 Enable and Disable

The TXS0108E-Q1 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (t_{dis}) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{en}) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

7.3.5 Pull-up or Pull-down Resistors on I/O Lines

The TXS0108E-Q1 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower V_{OL} values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

7.4 Device Functional Modes

The TXS0108E-Q1 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TXS0108E-Q1 can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The device is an excellent choice for use in applications where an open-drain driver is connected to the data I/Os. The device is appropriate for applications where a push-pull driver is connected to the data I/Os, but the TXB0104 device, *4-Bit Bidirectional Voltage-Level Translator* might be a better option for such push-pull applications. The device is a semi-buffered auto-direction-sensing voltage translator design is optimized for translation applications (for example, MMC Card Interfaces) that require the system to start out in a low-speed open-drain mode and then switch to a higher speed push-pull mode.

8.2 Typical Application

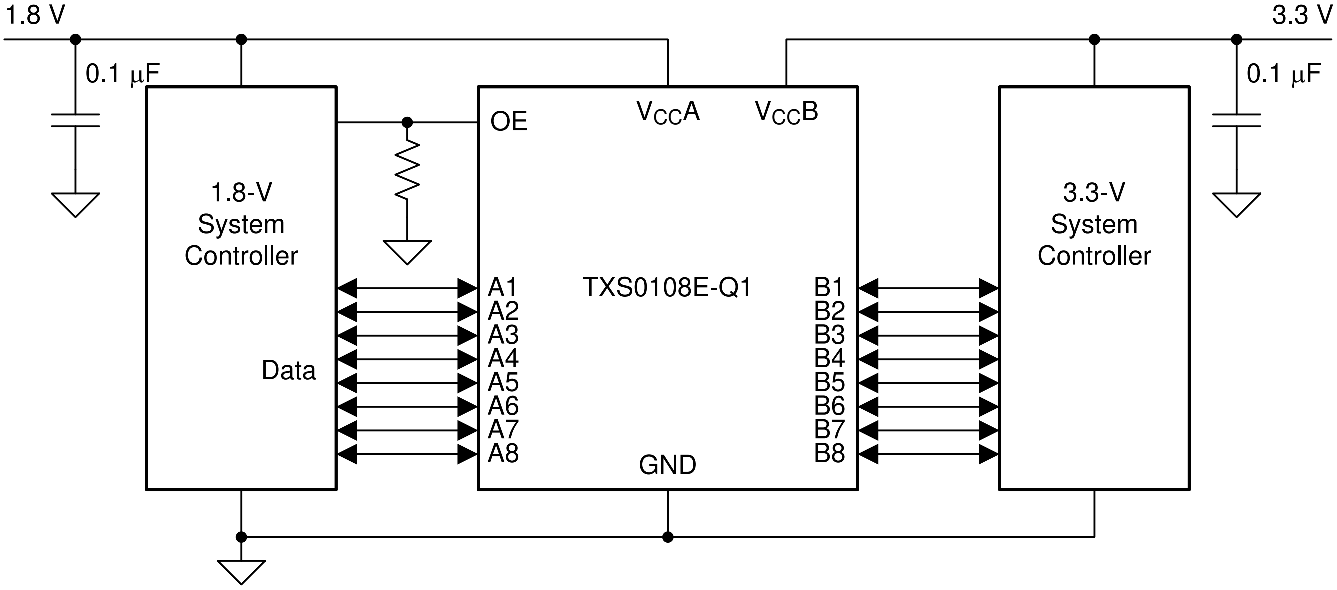


Figure 8-1. Typical Application Circuit

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1. Ensure that $V_{CCA} \le V_{CCB}$.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	1.4V to 3.6V
Output voltage range	1.65V to 5.5V

8.2.2 Detailed Design Procedure

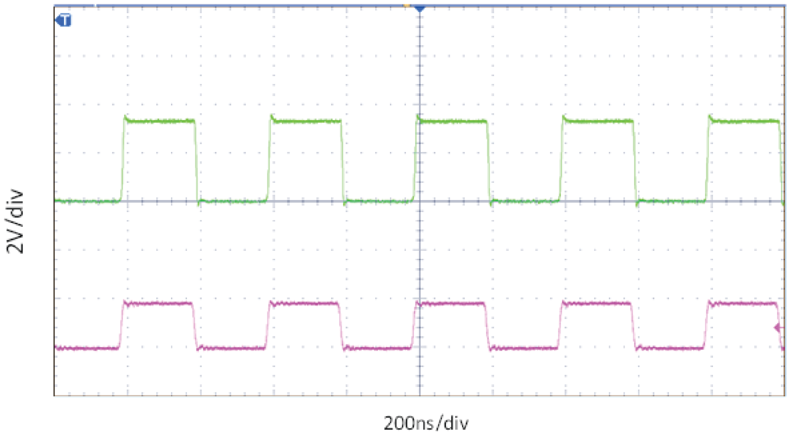
To begin the design process, determine the following:

- Input voltage range

  - Use the supply voltage of the device that is driving the TXS0108E-Q1 device to determine the input voltage range. For a valid logic high the value must exceed the V_{IH} of the input port. For a valid logic low the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the TXS0108E-Q1 device is driving to determine the output voltage range.
  - The TXS0108E-Q1 device has smart internal pull-up resistors. External pull-up resistors can be added to reduce the total RC of a signal trace if necessary.
- An external pull-down resistor decreases the output VOH and VOL. Use Equation 1 to calculate the VOH as a result of an external pull-down resistor.

$$V_{OH} = V_{CCx} \times R_{PD} / (R_{PD} + 4k\Omega) \quad (1)$$

8.2.3 Application Curves



V_{CCA} = 1.8V V_{CCB} = 3.3V

Figure 8-2. Level-Translation of a 2.5MHz Signal

8.3 Power Supply Recommendations

During operation, ensure that $V_{CCA} \leq V_{CCB}$ at all times. The sequencing of each power supply will not damage the device during the power up operation, so either power supply can be ramped up first. The output-enable (OE) input circuit is designed so that it is supplied by V_{CCA} and when the (OE) input is low, all outputs are placed in the high-impedance state. To put the outputs in the high-impedance state during power up or power down, tie the OE input pin to GND through a pull-down resistor, and do not enable the OE input until V_{CCA} and V_{CCB} are fully ramped and stable. The current-sourcing capability of the driver determines the minimum value of the pull-down resistor to ground.

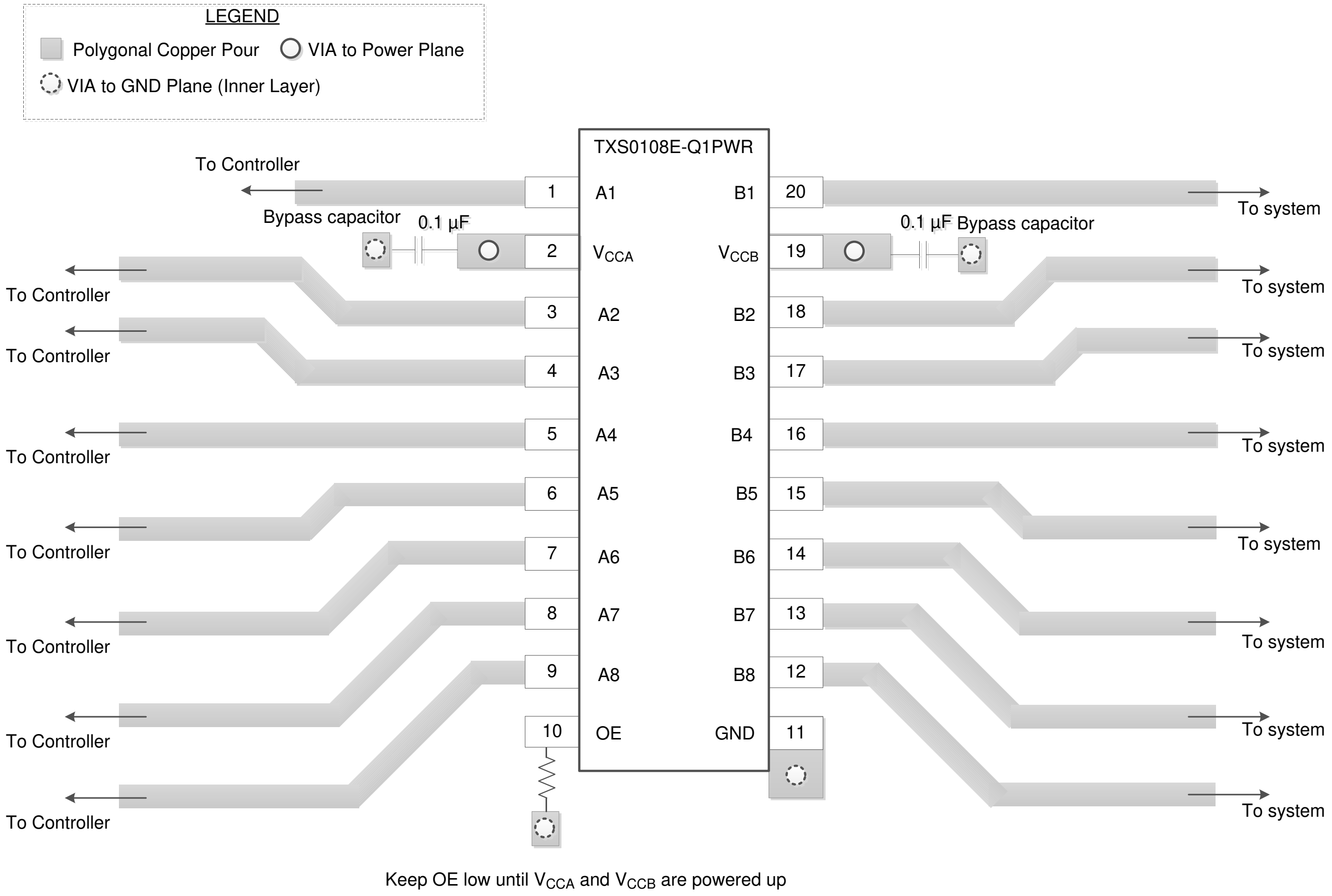
8.4 Layout

8.4.1 Layout Guidelines

For device reliability, following common printed-circuit board layout guidelines is recommended.

- Bypass capacitors should be used on power supplies. Place the capacitors as close as possible to the VCCA, VCCB, and GND pin.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one shot duration, approximately 30ns, causing any reflection to encounter low impedance at the source driver.

8.4.2 Layout Example



Keep OE low until V_{CCA} and V_{CCB} are powered up

Figure 8-3. Layout Example

9 Device and Documentation Support

9.1 Documentation Support

Related Documentation

For related documentation, see the following:

- Texas Instruments, A guide to Voltage level translation using TXS devices
- Texas Instruments, Factors affecting the Vol of TXS Auto Bidirectional Devices
- Texas Instruments, Effects of Pullup and Pulldown resistors on TXS Devices

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision F (November 2024) to Revision G (November 2024) **Page**

- Added DGS package..1

Changes from Revision E (April 2024) to Revision F (November 2024) **Page**

- Updated thermal values..6

Changes from Revision D (January 2024) to Revision E (April 2024) **Page**

- Added the RKS package.. 1
- Updated EN/DIS times in the *Switching Characteristics* 9

Changes from Revision C (July 2023) to Revision D (January 2024)	Page
• Updated *Switching Characteristics*	9

Changes from Revision B (May 2020) to Revision C (July 2023)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1

Changes from Revision A (February 2016) to Revision B (May 2020)	Page
• Changed V_{CCB} MAX from 5.5V to 6.5V in the *Absolute Maximum Ratings* table	5

Changes from Revision * (June 2015) to Revision A (February 2016)	Page
• Made changes to Pin Functions	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TXS0108EQDGSRQ1	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	XS108Q
TXS0108EQDGSRQ1.A	Active	Production	VSSOP (DGS) | 20	5000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	XS108Q
TXS0108EQPWRQ1	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF08EQ1
TXS0108EQPWRQ1.A	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF08EQ1
TXS0108EQPWRQ1.B	Active	Production	TSSOP (PW) | 20	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	YF08EQ1
TXS0108EQWRKSRQ1	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TXS108Q
TXS0108EQWRKSRQ1.A	Active	Production	VQFN (RKS) | 20	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TXS108Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TXS0108E-Q1 :

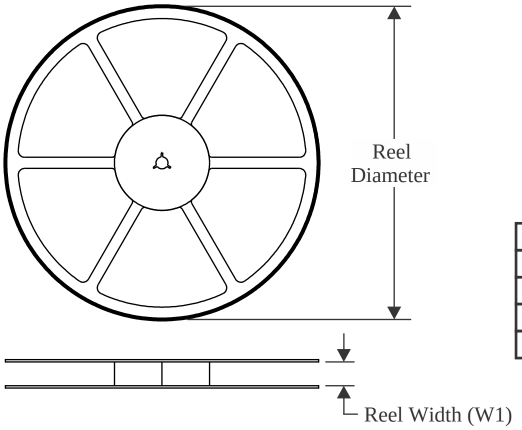
- Catalog : TXS0108E

NOTE: Qualified Version Definitions:

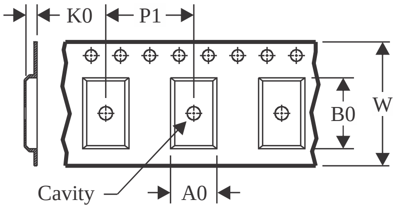
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

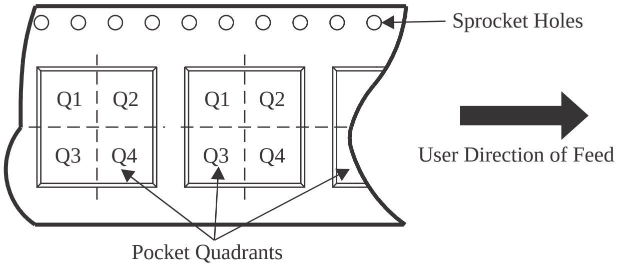


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

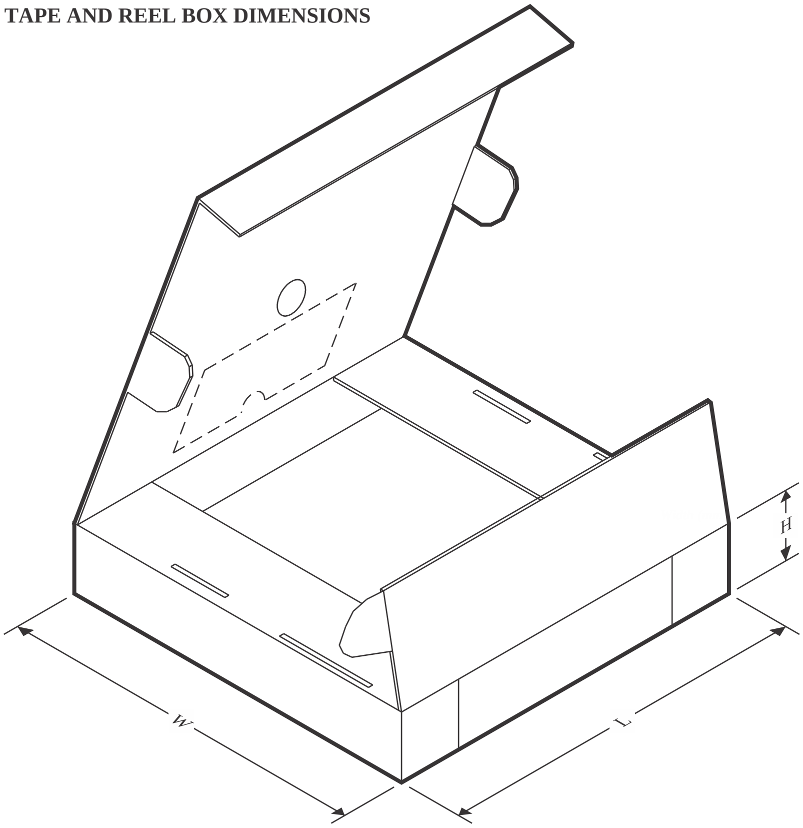
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TXS0108EQDGSRQ1	VSSOP	DGS	20	5000	330.0	16.4	5.4	5.4	1.45	8.0	16.0	Q1
TXS0108EQPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1
TXS0108EQWRKSRQ1	VQFN	RKS	20	3000	180.0	12.4	2.8	4.8	1.2	4.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



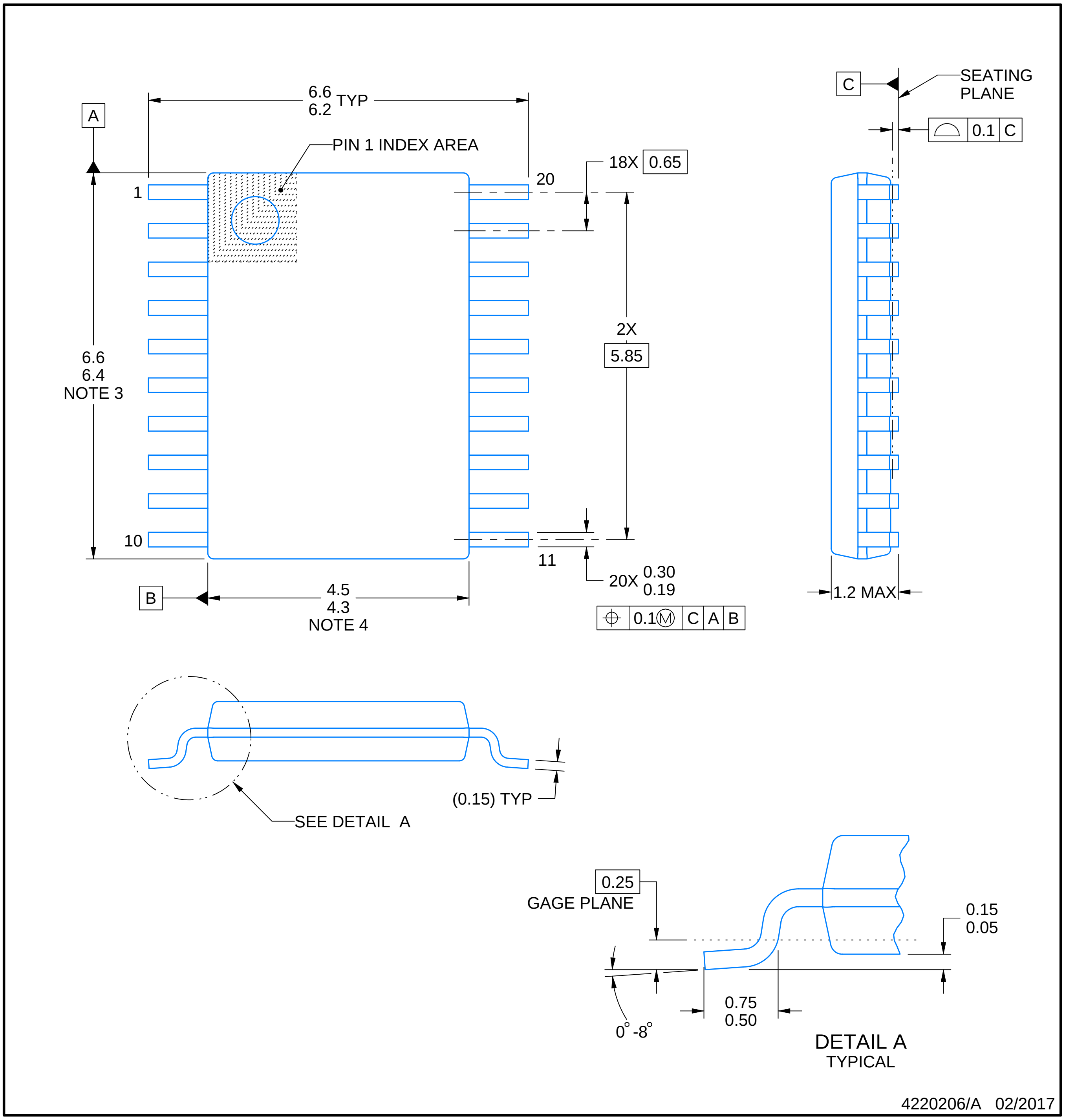
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TXS0108EQDGSRQ1	VSSOP	DGS	20	5000	353.0	353.0	32.0
TXS0108EQPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0
TXS0108EQWRKSRQ1	VQFN	RKS	20	3000	210.0	185.0	35.0

PACKAGE OUTLINE

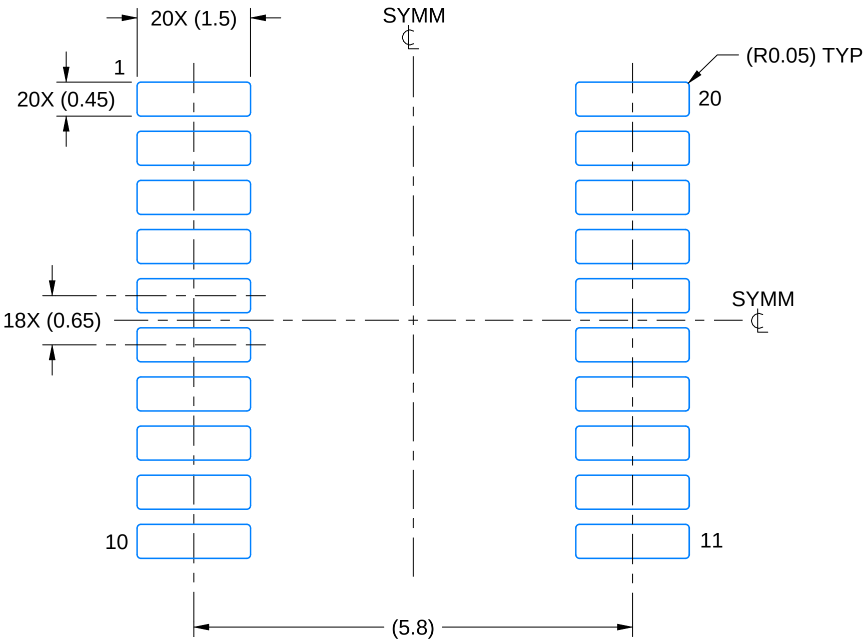
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

NON-SOLDER MASK
DEFINED
(PREFERRED)

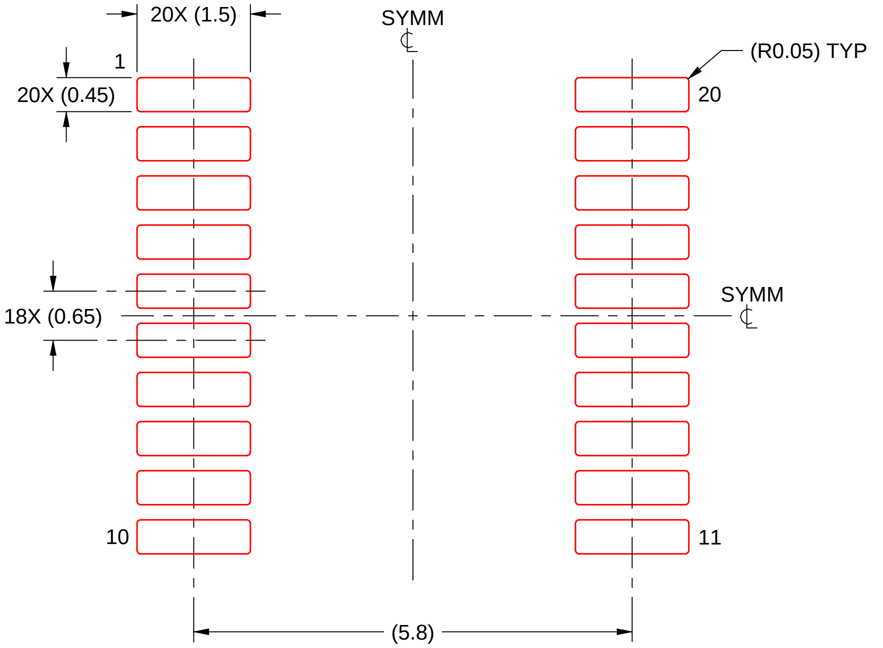
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

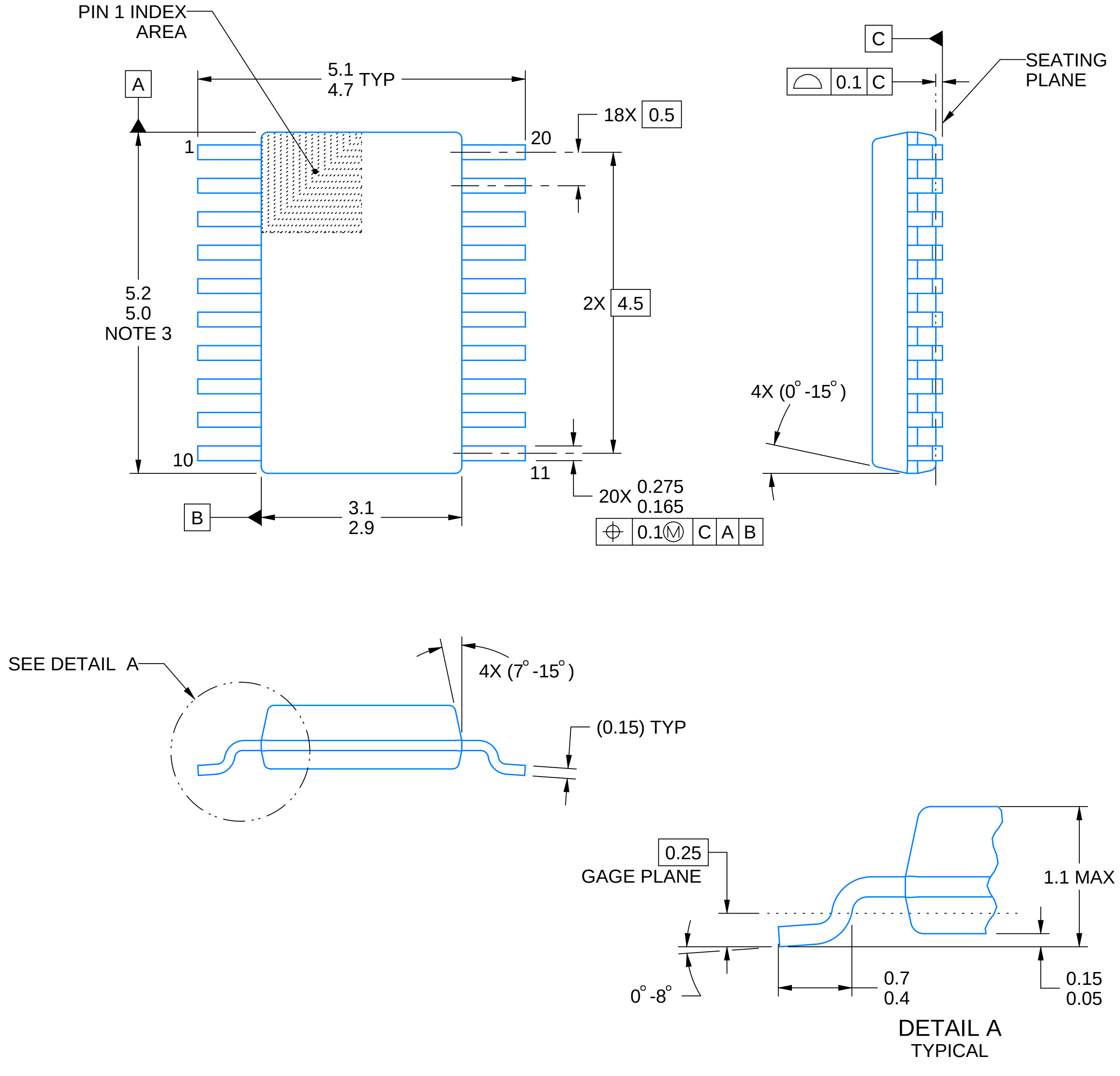
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0020A

VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

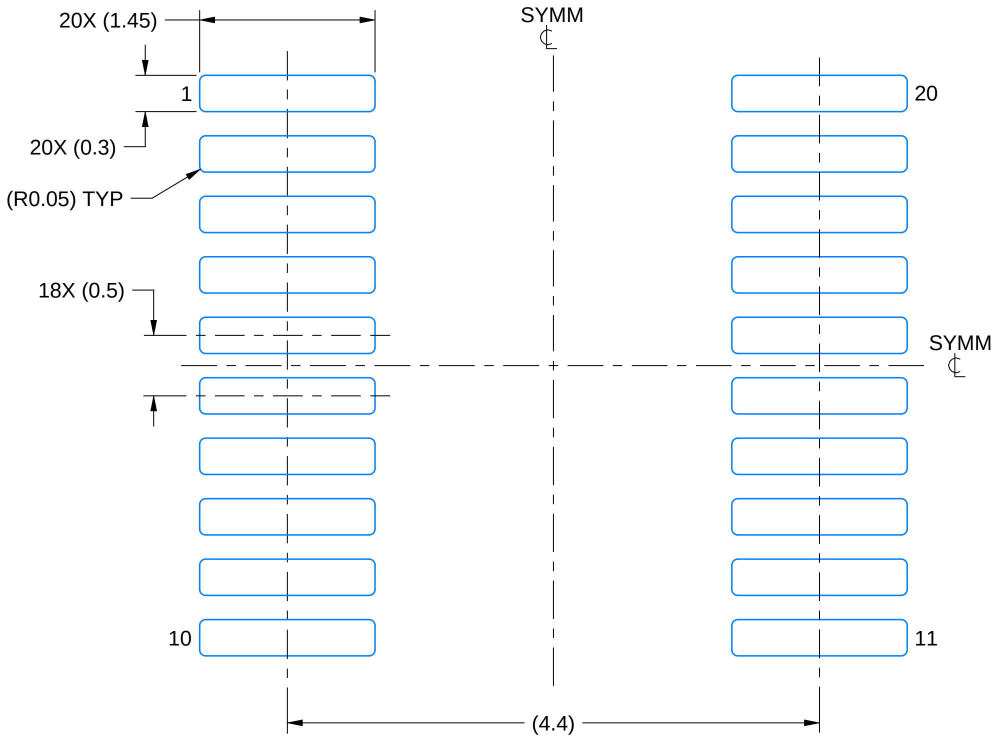


4226367/A 10/2020

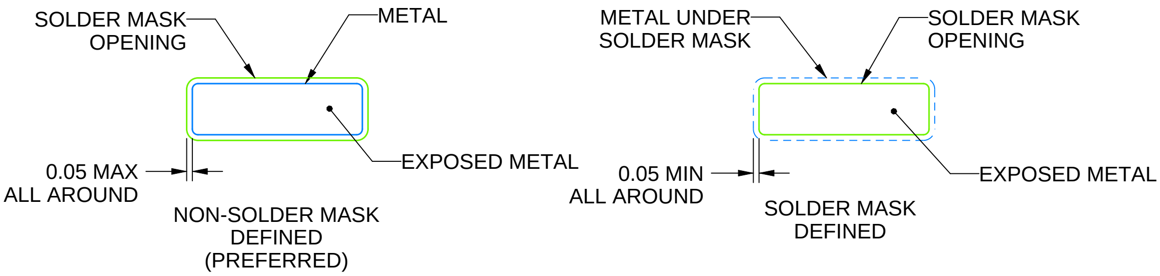
NOTES:

PowerPAD is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
SCALE: 16X

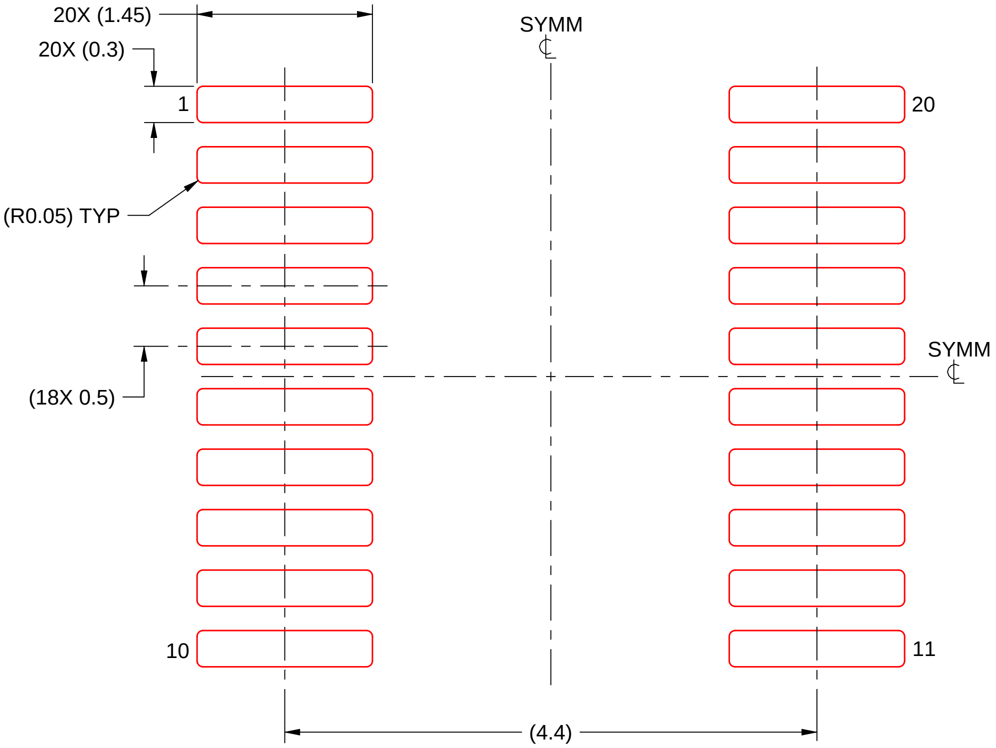


SOLDER MASK DETAILS

4226367/A 10/2020

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 16X

4226367/A 10/2020

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

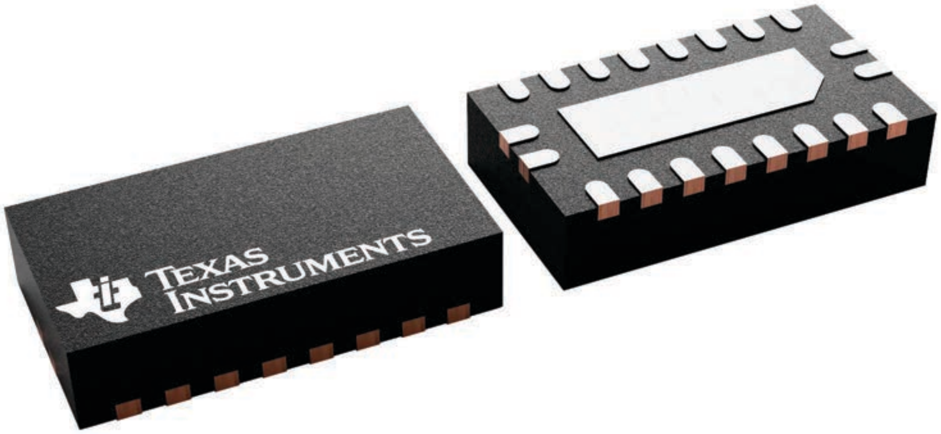
RKS 20

VQFN - 1 mm max height

2.5 x 4.5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

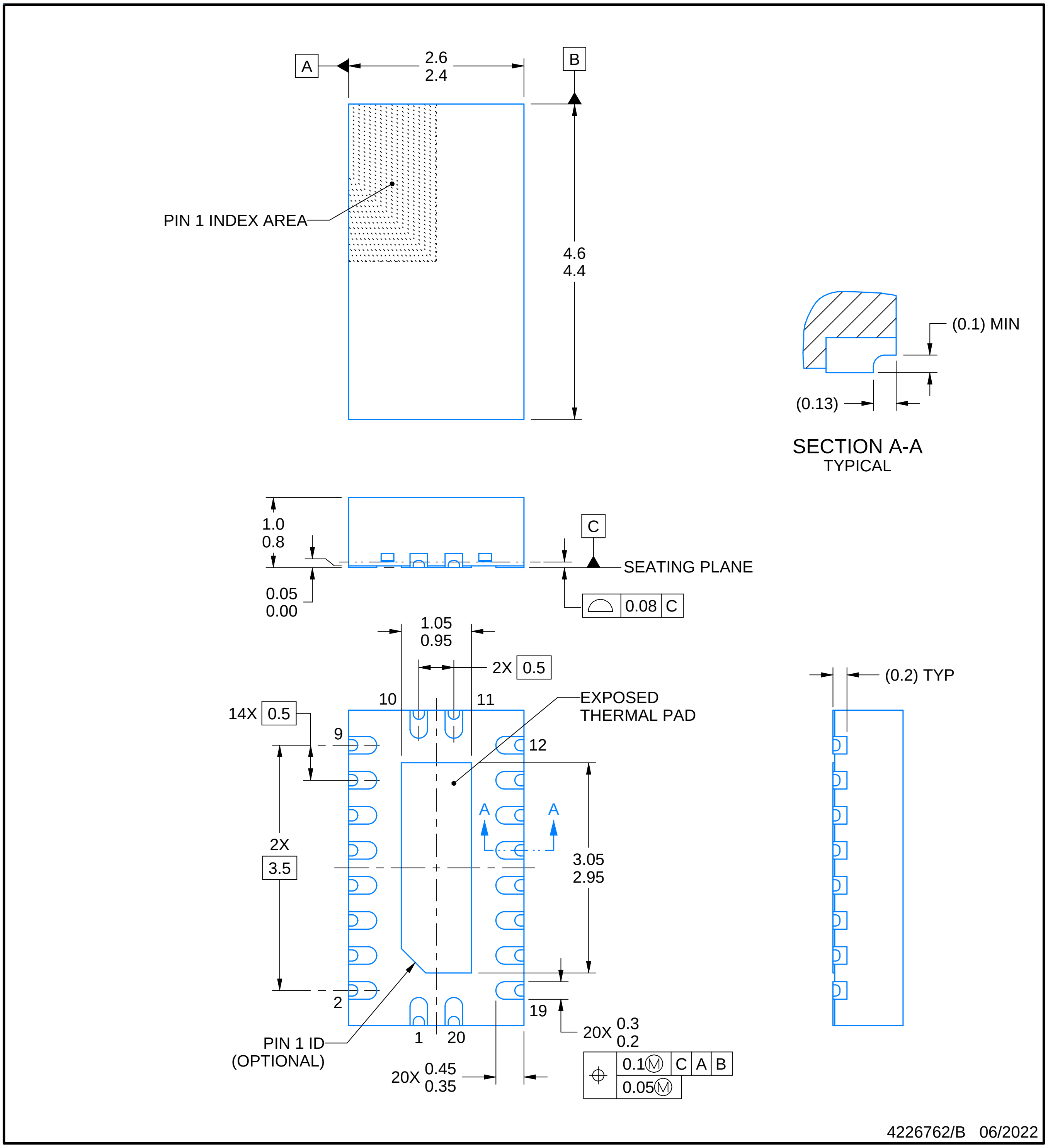
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



PACKAGE OUTLINE

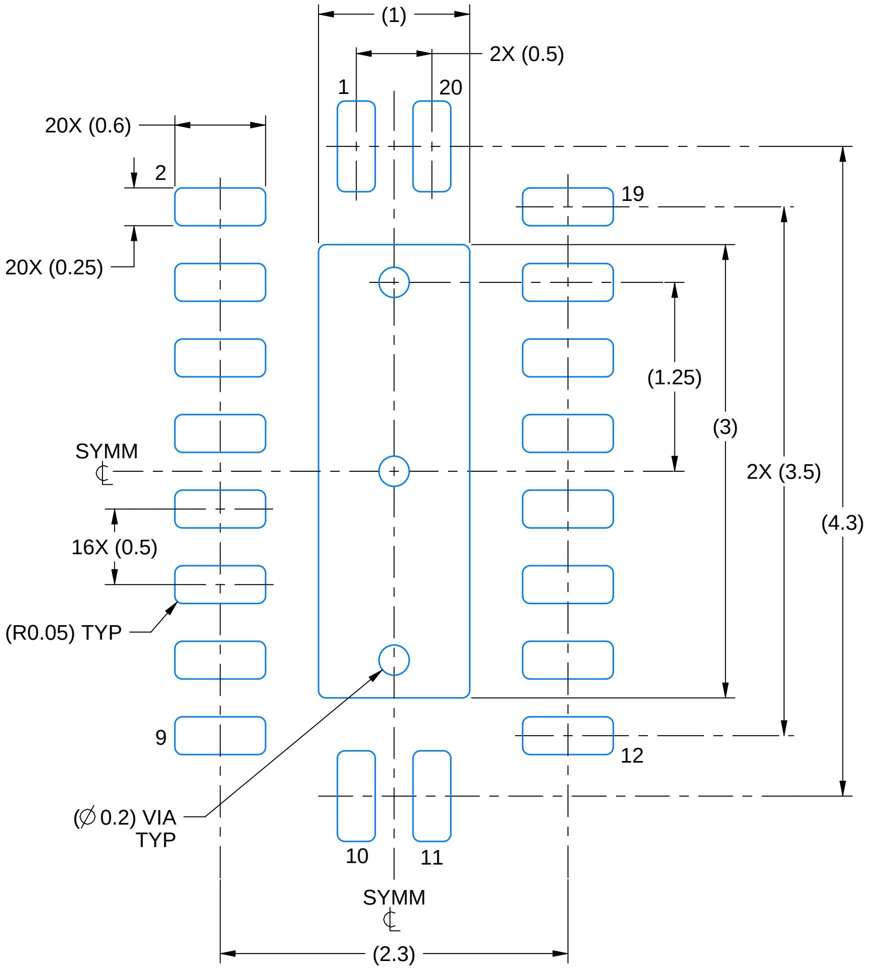
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

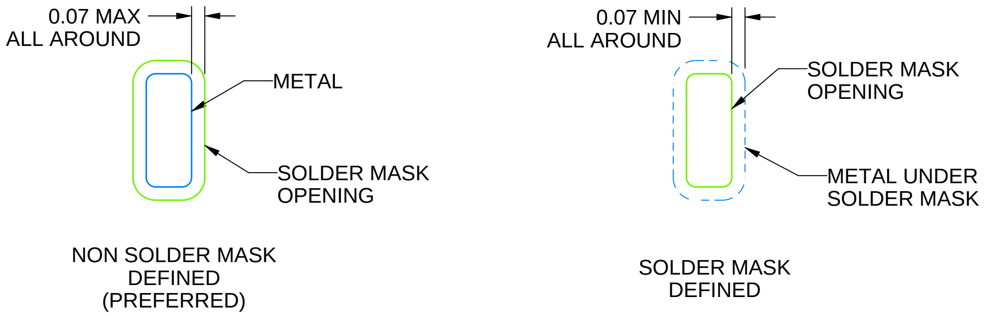


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



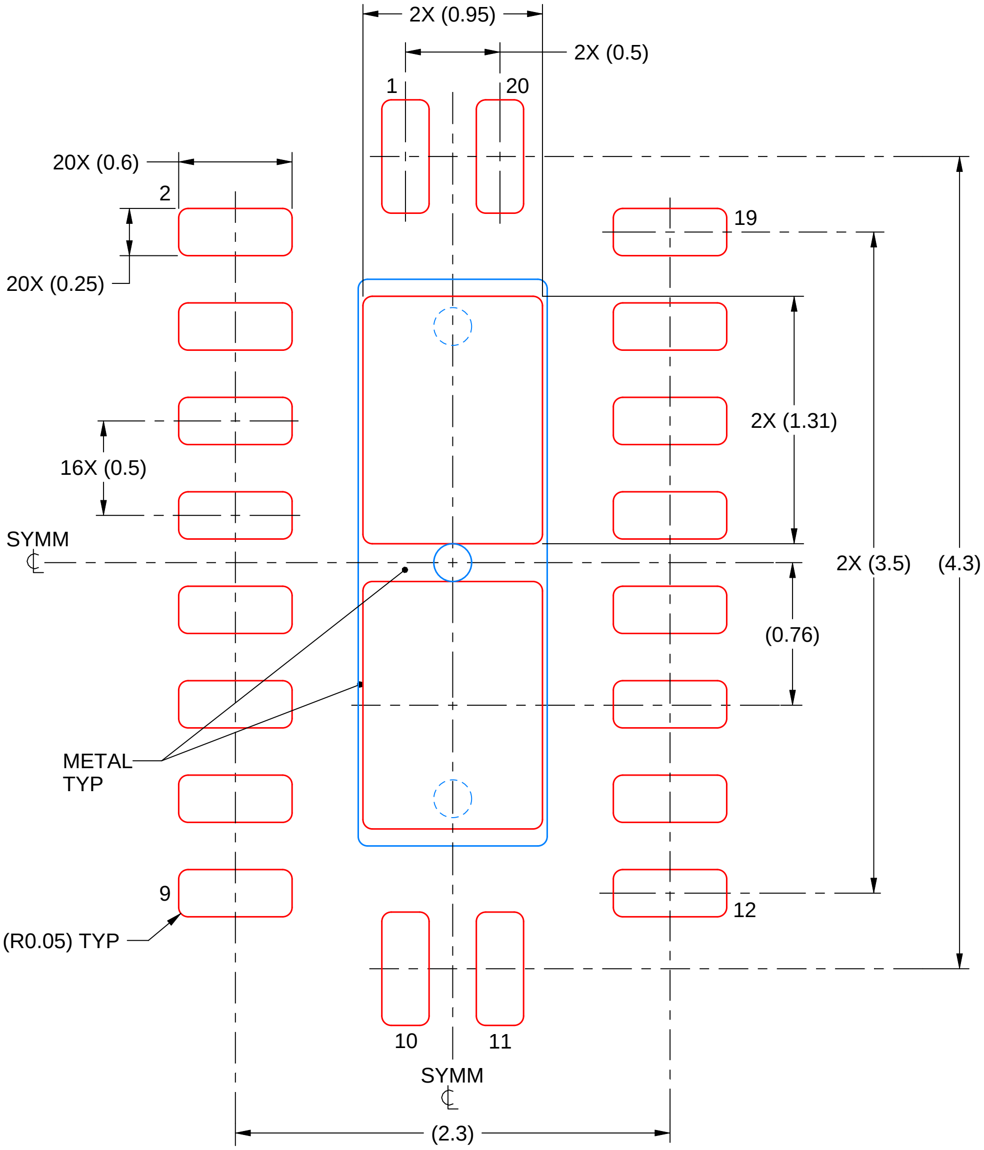
LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
83% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4226762/B 06/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated