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2N5551 / MMBT5551

NPN General-Purpose Amplifier

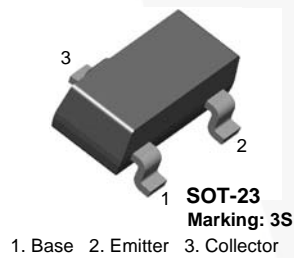
Description

This device is designed for general-purpose high-voltage amplifiers and gas discharge display drivers.

2N5551



MMBT5551



Ordering Information⁽¹⁾

Part Number	Top Mark	Package	Packing Method
2N5551TA	5551	TO-92 3L	Ammo
2N5551TFR	5551	TO-92 3L	Tape and Reel
2N5551TF	5551	TO-92 3L	Tape and Reel
2N5551BU	5551	TO-92 3L	Bulk
MMBT5551	3S	SOT-23 3L	Tape and Reel

Note:

- Suffix "-C" means Center Collector in 2N5551 (1. Emitter 2. Collector 3. Base)
Suffix "-Y" means h_{FE} 180~240 in 2N5551 (Test condition: $I_C = 10$ mA, $V_{CE} = 5.0$ V)

Absolute Maximum Ratings⁽²⁾

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Units
V_{CEO}	Collector-Emitter Voltage	160	V
V_{CBO}	Collector-Base Voltage	180	V
V_{EBO}	Emitter-Base Voltage	6	V
I_C	Collector current - Continuous	600	mA
$T_J, T_{stg}^{(2)}$	Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$

Notes:

- These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
- These ratings are based on a maximum junction temperature of 150°C .
These are steady-state limits. Fairchild Semiconductor should be consulted on applications involving pulsed or low-duty cycle operations.

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Maximum		Units
		2N5551	MMBT5551	
P_D	Total Device Dissipation	625	350	mW
	Derate above 25°C	5.0	2.8	mW/ $^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	83.3		$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	200	357	$^\circ\text{C}/\text{W}$

Electrical Characteristics⁽⁴⁾Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Condition	Min.	Max.	Units
Off Characteristics					
$V_{(BR)CEO}$	Collector-Emitter Breakdown Voltage	$I_C = 1.0\text{ mA}, I_B = 0$	160		V
$V_{(BR)CBO}$	Collector-Base Breakdown Voltage	$I_C = 100\ \mu\text{A}, I_E = 0$	180		V
$V_{(BR)EBO}$	Emitter-Base Breakdown Voltage	$I_E = 10\ \mu\text{A}, I_C = 0$	6.0		V
I_{CBO}	Collector Cut-Off Current	$V_{CB} = 120\text{ V}, I_E = 0$		50	nA
		$V_{CB} = 120\text{ V}, I_E = 0, T_A = 100^\circ\text{C}$		50	μA
I_{EBO}	Emitter Cut-Off Current	$V_{EB} = 4.0\text{ V}, I_C = 0$		50	nA
On Characteristics					
h_{FE}	DC Current Gain	$I_C = 1.0\text{ mA}, V_{CE} = 5.0\text{ V}$	80		
		$I_C = 10\text{ mA}, V_{CE} = 5.0\text{ V}$	80	250	
		$I_C = 50\text{ mA}, V_{CE} = 5.0\text{ V}$	30		
$V_{CE(sat)}$	Collector-Emitter Saturation Voltage	$I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$		0.15	V
		$I_C = 50\text{ mA}, I_B = 5.0\text{ mA}$		0.20	V
$V_{BE(sat)}$	Base-Emitter On Voltage	$I_C = 10\text{ mA}, I_B = 1.0\text{ mA}$		1.0	V
		$I_C = 50\text{ mA}, I_B = 5.0\text{ mA}$		1.0	V
Small-Signal Characteristics					
f_T	Current Gain Bandwidth Product	$I_C = 10\text{ mA}, V_{CE} = 10\text{ V},$ $f = 100\text{ MHz}$	100		MHz
C_{obo}	Output Capacitance	$V_{CB} = 10\text{ V}, I_E = 0, f = 1.0\text{ MHz}$		6.0	pF
C_{ibo}	Input Capacitance	$V_{BE} = 0.5\text{ V}, I_C = 0, f = 1.0\text{ MHz}$		20	pF
H_{fe}	Small-Signal Current Gain	$I_C = 1.0\text{ mA}, V_{CE} = 10\text{ V}, f = 1.0\text{ kHz}$	50	250	
NF	Noise Figure	$I_C = 250\ \mu\text{A}, V_{CE} = 5.0\text{ V},$ $R_S = 1.0\text{ k}\Omega, f = 10\text{ Hz to }15.7\text{ kHz}$		8.0	dB

Note:4. PCB board size FR-4 76 x 114 x 0.6 T mm³ (3.0 inch x 4.5 inch x 0.062 inch) with minimum land pattern size.

Typical Performance Characteristics

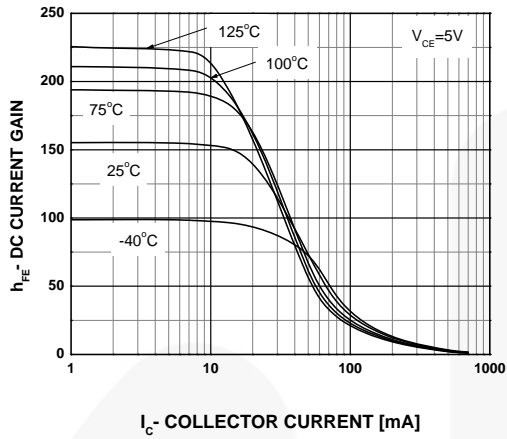


Figure 1. Typical Pulsed Current Gain vs. Collector Current

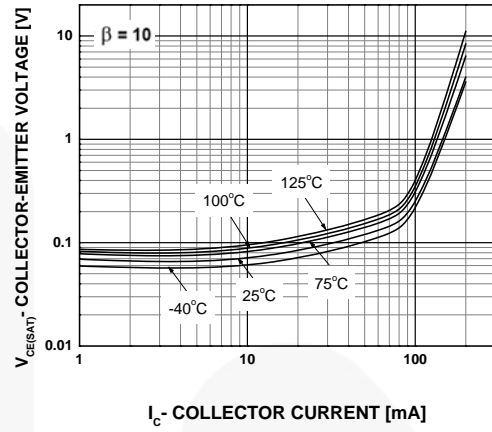


Figure 2. Collector-Emitter Saturation Voltage vs. Collector Current

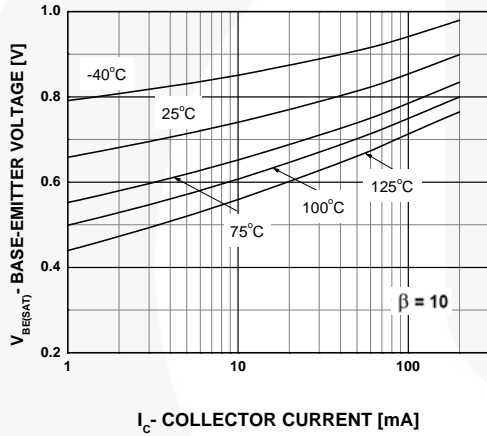


Figure 3. Base-Emitter Saturation Voltage vs. Collector Current

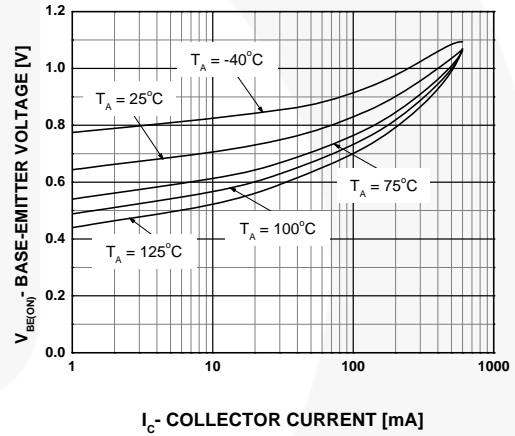


Figure 4. Base-Emitter On Voltage vs. Collector Current

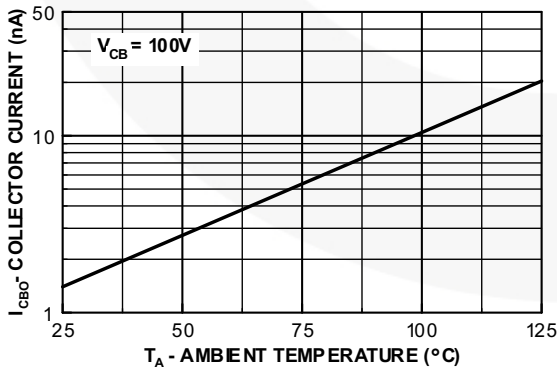


Figure 5. Collector Cut-Off Current vs. Ambient Temperature

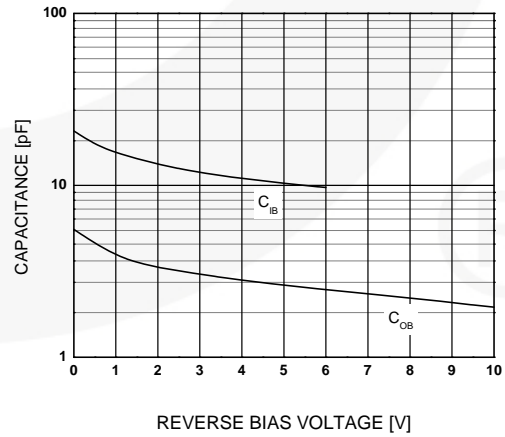


Figure 6. Input and Output Capacitance vs. Reverse Voltage

Typical Performance Characteristics (Continued)

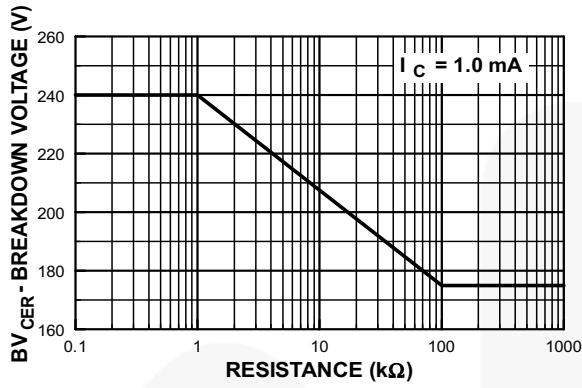


Figure 7. Collector- Emitter Breakdown Voltage with Resistance between Emitter-Base

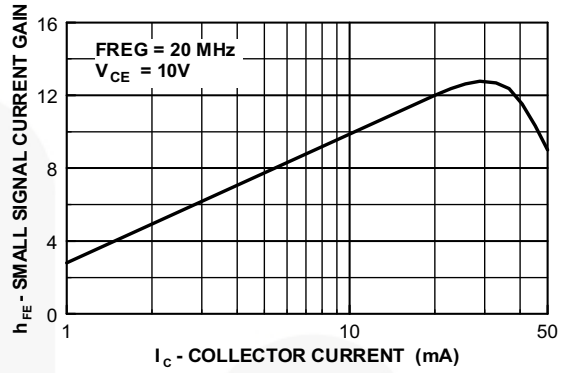


Figure 8. Small Signal Current Gain vs. Collector Current

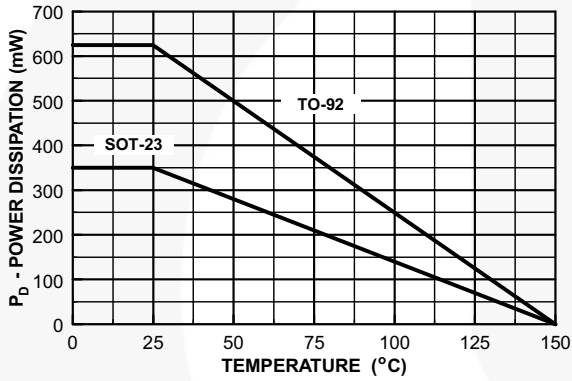
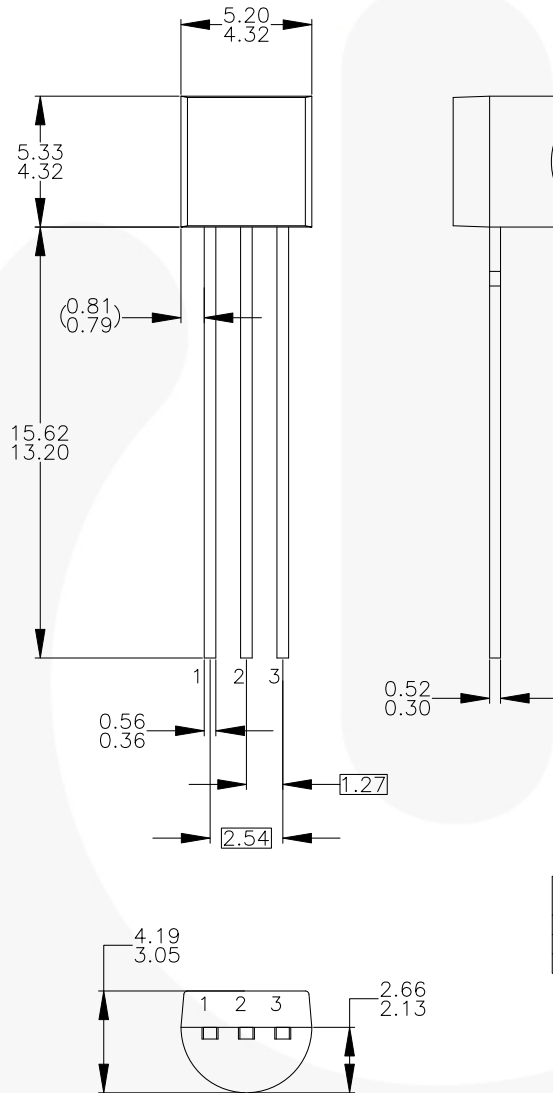


Figure 9. Power Dissipation vs. Ambient Temperature

Physical Dimensions

TO-92 (Bulk)



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DRAWING WITH REFERENCE TO JEDEC TO-92 RECOMMENDATIONS.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:

P - BIPOLAR E - EMITTER D - DRAIN
 F - JFET B - BASE S - SOURCE
 M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03DREV3.

Figure 10. 3-LEAD, TO92, JEDEC TO-92 COMPLIANT STRAIGHT LEAD CONFIGURATION (OLD TO92AM3) (ACTIVE)

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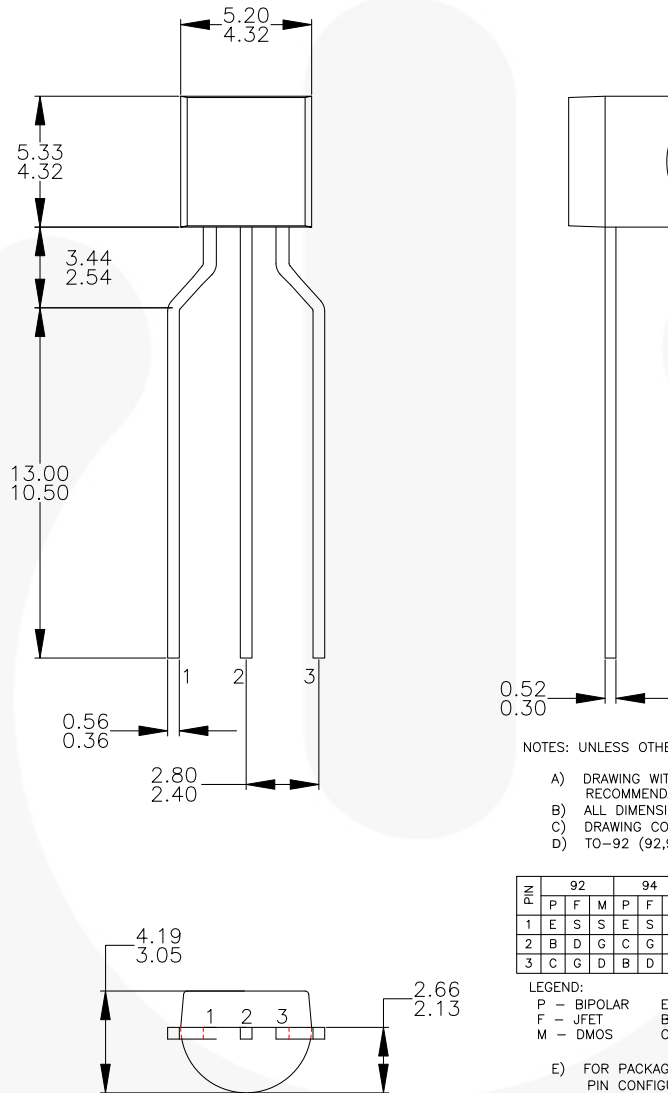
<http://www.fairchildsemi.com/packaging/>

For current tape and reel specifications, visit Fairchild Semiconductor's online packaging area:

http://www.fairchildsemi.com/packaging/tr/to92pdd_tr.pdf

Physical Dimensions (Continued)

TO-92 (Tape and Reel, Ammo)



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- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DRAWING CONFORMS TO ASME Y14.5M-1994.
- D) TO-92 (92,94,96,97,98) PIN CONFIGURATION:

PIN	92			94			96			97			98		
	P	F	M	P	F	M	B	F	M	P	F	M	P	F	M
1	E	S	S	E	S	S	B	D	G	C	G	D	C	G	D
2	B	D	G	C	G	D	E	S	S	B	D	G	E	S	S
3	C	G	D	B	D	G	C	G	D	E	S	S	B	D	G

LEGEND:
P - BIPOLAR E - EMITTER D - DRAIN
F - JFET B - BASE S - SOURCE
M - DMOS C - COLLECTOR G - GATE

- E) FOR PACKAGE 92, 94, 96, 97 AND 98: PIN CONFIGURATION DRAIN "D" AND SOURCE "S" ARE INTERCHANGEABLE AT JFET "F" OPTION.
- F) DRAWING FILENAME: MKT-ZA03FREV2.

Figure 11. 3-LEAD, TO92, MOLDED, 0.200 IN-LINE SPACING LD FORM(J62Z OPTION) (ACTIVE)

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Physical Dimensions (Continued)

SOT-23

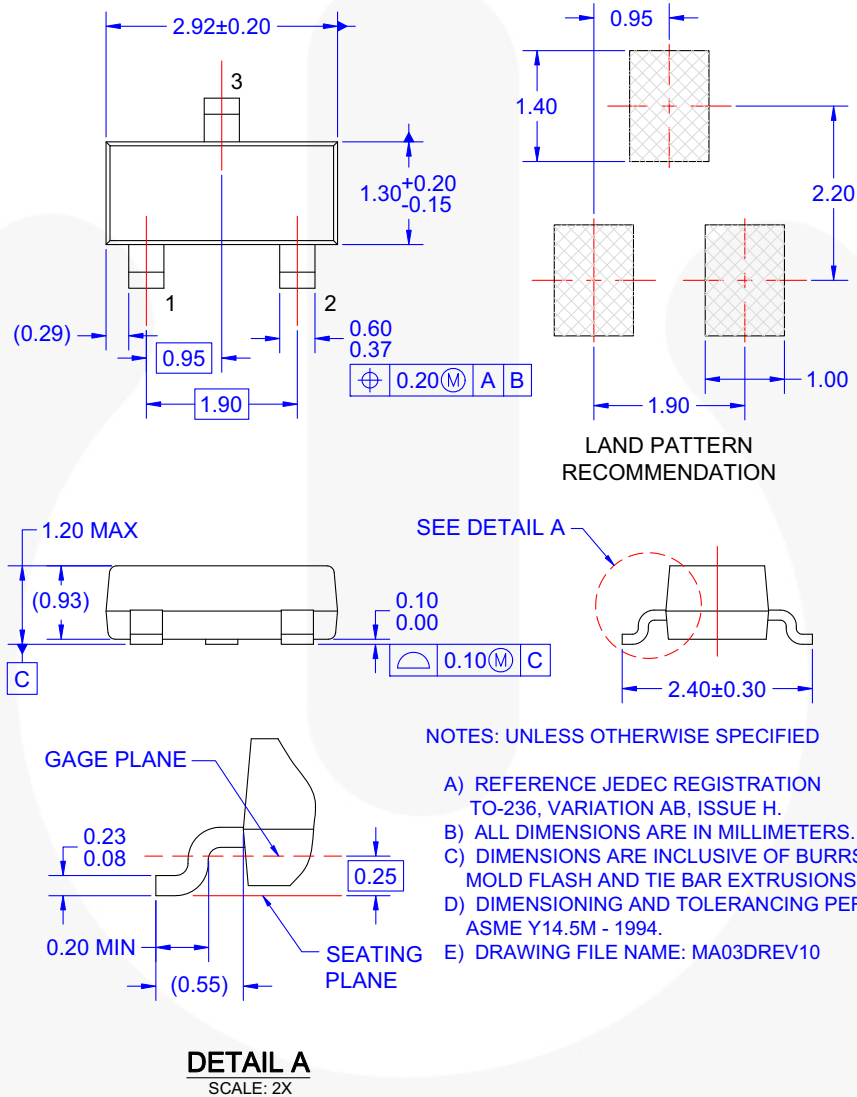


Figure 12. 3-LEAD, SOT23, JEDEC TO-236, LOW PROFILE (ACTIVE)

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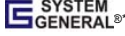



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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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