# CD54HC4094, CD74HC4094, CD74HCT4094

Data sheet acquired from Harris Semiconductor
SCHS211E

## High−Speed CMOS Logic 8−Stage Shift and Store Bus Register, Three−State

November 1997 − Revised December 2010

### Features

- Buffered Inputs
- Separate Serial Outputs Synchronous to Both Positive and Negative Clock Edges For Cascading
- Fanout (Over Temperature Range)
  - Standard Outputs . . . . . 10 LSTTL Loads
  - Bus Driver Outputs . . . . . 15 LSTTL Loads
- Wide Operating Temperature Range . . . −55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
  - 2V to 6V Operation
  - High Noise Immunity: $N_{IL}$ = 30%, $N_{IH}$ = 30% of $V_{CC}$ at $V_{CC}$ = 5V
- HCT Types
  - 4.5V to 5.5V Operation
  - Direct LSTTL Input Logic Compatibility, $V_{IL}$ = 0.8V (Max), $V_{IH}$ = 2V (Min)
  - CMOS Input Compatibility, $I_I \leq 1\mu A$ at $V_{OL}$, $V_{OH}$

### Description

The ÕHC4094and CD74HCT4094 are 8−stage serial shift registers having a storage latch associated with each stage for strobing data from the serial input to parallel buffered three−state outputs. The parallel outputs may be connected directly to common bus lines. Data is shifted on positive clock transitions. The data in each shift register stage is transferred to the storage register when the Strobe input is high. Data in the storage register appears at the outputs whenever the Output−Enable signal is high.

Two serial outputs are available for cascading a number of these devices. Data is available at the $QS_1$ serial output terminal on positive clock edges to allow for high−speed operation in cascaded system in which the clock rise time is fast. The same serial information, available at the $QS_2$ terminal on the next negative clock edge, provides a means for cascading these devices when the clock rise time is slow.

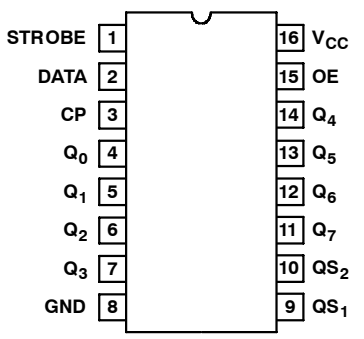
### Ordering Information

| PART NUMBER | TEMP. RANGE (°C) | PACKAGE |
|---|---|---|
| CD54HC4094F3A | −55 to 125 | 16 Ld CERDIP |
| CD74HC4094E | −55 to 125 | 16 Ld PDIP |
| CD74HC4094M | −55 to 125 | 16 Ld SOIC |
| CD74HC4094MT | −55 to 125 | 16 Ld SOIC |
| CD74HC4094M96G3 | −55 to 125 | 16 Ld SOIC |
| CD74HC4094NSR | −55 to 125 | 16 Ld SOP |
| CD74HC4094PW | −55 to 125 | 16 Ld TSSOP |
| CD74HC4094PWR | −55 to 125 | 16 Ld TSSOP |
| CD74HC4094PWT | −55 to 125 | 16 Ld TSSOP |
| CD74HCT4094E | −55 to 125 | 16 Ld PDIP |
| CD74HCT4094M | −55 to 125 | 16 Ld SOIC |
| CD74HCT4094MT | −55 to 125 | 16 Ld SOIC |
| CD74HCT4094M96 | −55 to 125 | 16 Ld SOIC |

NOTE: When ordering, use the entire part number. The suffixes 96 and R denote tape and reel. The suffix T denotes a small−quantity reel of 250.

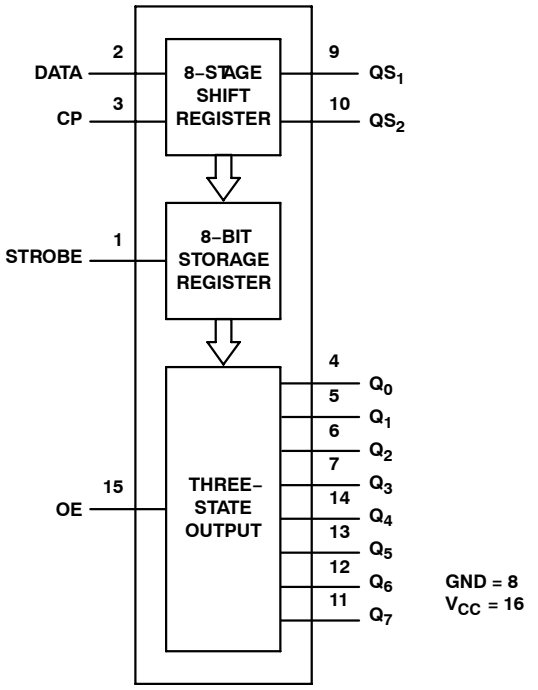
### Pinout

**CD54HC4094 (CERDIP)**
**CD74HC4094 (PDIP, SOIC, SOP, TSSOP)**
**CD74HCT4094 (PDIP, SOIC)**
TOP VIEW




CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

## Functional Diagram



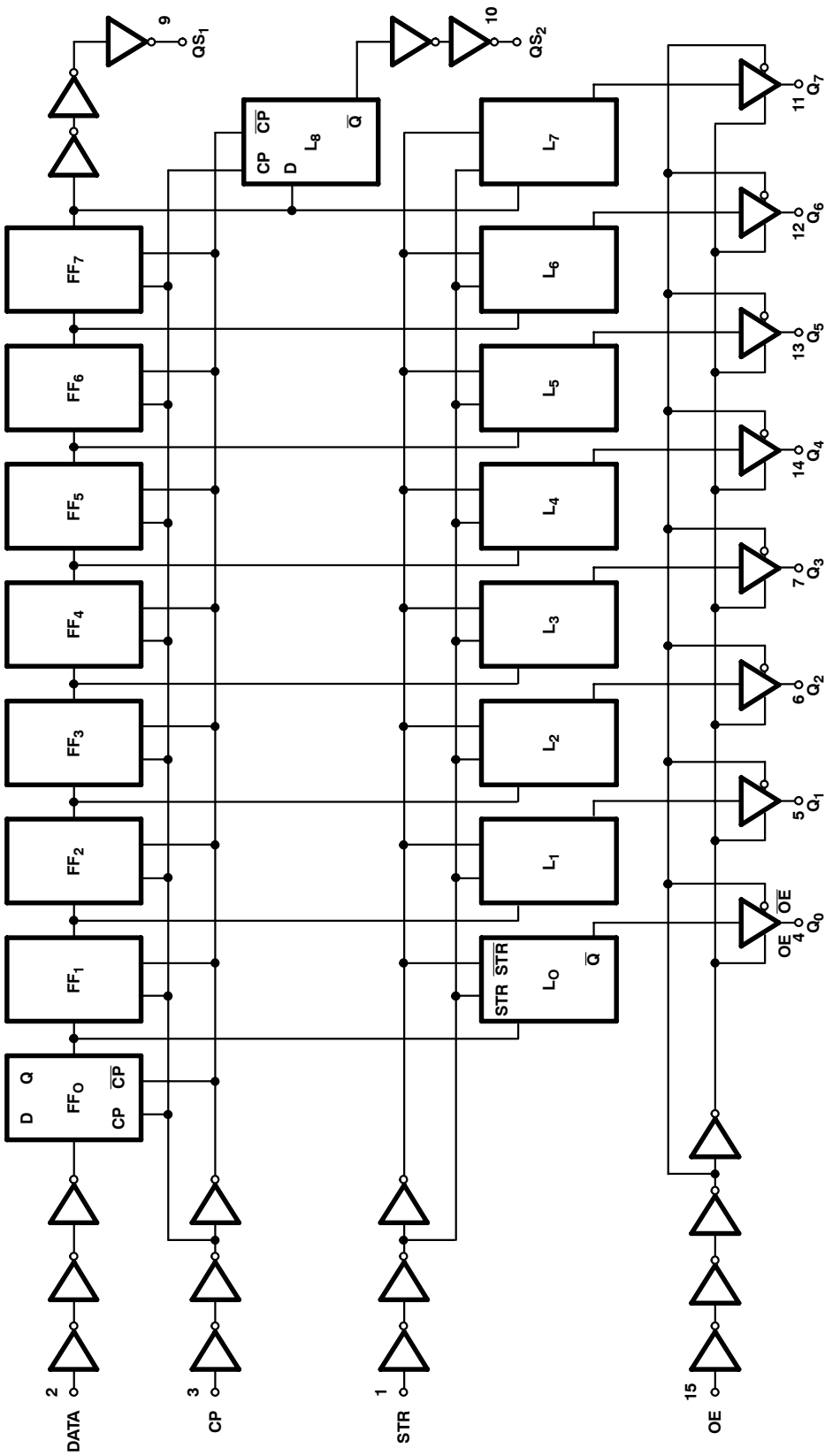

**TRUTH TABLE**

| INPUTS | | | | PARALLEL OUTPUTS | | SERIAL OUTPUTS | |
|---|---|---|---|---|---|---|---|
| **CP** | **OE** | **STR** | **D** | **$Q_0$** | **$Q_n$** | **$QS_1$** (NOTE 1) | **$QS_2$** |
| ↑ | L | X | X | Z | Z | QÕ6 | NC |
| ↓ | L | X | X | Z | Z | NC | $Q_7$ |
| ↑ | H | L | X | NC | NC | QÕ6 | NC |
| ↑ | H | H | L | L | $Q_n$ –1 | QÕ6 | NC |
| ↑ | H | H | H | H | $Q_n$ –1 | QÕ6 | NC |
| ↓ | H | H | H | NC | NC | NC | $Q_7$ |

H = High Voltage Level, L = Low Voltage Level, X = DonÕt Care, NC = No charge, Z = High Impedance Off–state,
↑ = Transition from Low to High Level, ↓ = Transition from High to Low.
NOTE:

1. At the positive clock edge the information in the seventh register stage is transferred to the 8th register stage and QS1 output.

## Logic Diagram



## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ . . . . . −0.5V to 7V
DC Input Diode Current, $I_{IK}$
For $V_I$ < −0.5V or $V_I$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Diode Current, $I_{OK}$
For $V_O$ < −0.5V or $V_O$ > $V_{CC}$ + 0.5V . . . . . ±20mA
DC Output Source or Sink Current per Output Pin, $I_O$
For $V_O$ > −0.5V or $V_O$ < $V_{CC}$ + 0.5V . . . . . ±25mA
DC $V_{CC}$ or Ground Current, $I_{CC}$ . . . . . ±50mA

## Operating Conditions

Temperature Range ($T_A$) . . . . . −55°C to 125°C
Supply Voltage Range, $V_{CC}$
HC Types . . . . . 2V to 6V
HCT Types . . . . . 4.5V to 5.5V
DC Input or Output Voltage, $V_I$, $V_O$ . . . . . 0V to $V_{CC}$
Input Rise and Fall Time
2V . . . . . 1000ns (Max)
4.5V. . . . . 500ns (Max)
6V . . . . . 400ns (Max)

## Thermal Information

Package Thermal Impedance, $\theta_{JA}$ (see Note 2):
E (PDIP) Package . . . . . 67°C/W
M (SOIC) Package . . . . . 73°C/W
NS (SOP) Package . . . . . 64oC/W
PW (TSSOP) Package. . . . . 108°C/W
Maximum Junction Temperature (Plastic Package) . . . . . 150°
Maximum Storage Temperature Range . . . . . −65°C to 150°
Maximum Lead Temperature (Soldering 10s) . . . . . 300°
SOIC − Lead Tips Only)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

2. The package thermal impedance is calculated in accordance with JESD 51−7.

## DC Electrical Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | TEST CONDITIONS $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | −40°C TO 85°C MIN | −40°C TO 85°C MAX | −55°C TO 125°C MIN | −55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | − | − | 2 | 1.5 | − | − | 1.5 | − | 1.5 | − | V |
| | | | | 4.5 | 3.15 | − | − | 3.15 | − | 3.15 | − | V |
| | | | | 6 | 4.2 | − | − | 4.2 | − | 4.2 | − | V |
| Low Level Input Voltage | $V_{IL}$ | − | − | 2 | − | − | 0.5 | − | 0.5 | − | 0.5 | V |
| | | | | 4.5 | − | − | 1.35 | − | 1.35 | − | 1.35 | V |
| | | | | 6 | − | − | 1.8 | − | 1.8 | − | 1.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | −0.02 | 2 | 1.9 | − | − | 1.9 | − | 1.9 | − | V |
| | | | −0.02 | 4.5 | 4.4 | − | − | 4.4 | − | 4.4 | − | V |
| | | | −0.02 | 6 | 5.9 | − | − | 5.9 | − | 5.9 | − | V |
| High Level Output Voltage TTL Loads | | | − | − | − | − | − | − | − | − | − | V |
| | | | −4 | 4.5 | 3.98 | − | − | 3.84 | − | 3.7 | − | V |
| | | | −5.2 | 6 | 5.48 | − | − | 5.34 | − | 5.2 | − | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 2 | − | − | 0.1 | − | 0.1 | − | 0.1 | V |
| | | | 0.02 | 4.5 | − | − | 0.1 | − | 0.1 | − | 0.1 | V |
| | | | 0.02 | 6 | − | − | 0.1 | − | 0.1 | − | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | − | − | − | − | − | − | − | − | − | V |
| | | | 4 | 4.5 | − | − | 0.26 | − | 0.33 | − | 0.4 | V |
| | | | 5.2 | 6 | − | − | 0.26 | − | 0.33 | − | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ or GND | − | 6 | − | − | ±0.1 | − | ±1 | − | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 6 | − | − | 8 | − | 80 | − | 160 | µA |

## DC Electrical Specifications (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS $V_I$ (V) | TEST CONDITIONS $I_O$ (mA) | $V_{CC}$ (V) | 25°C MIN | 25°C TYP | 25°C MAX | −40°C TO 85°C MIN | −40°C TO 85°C MAX | −55°C TO 125°C MIN | −55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **HCT TYPES** | | | | | | | | | | | | |
| High Level Input Voltage | $V_{IH}$ | – | – | 4.5 to 5.5 | 2 | – | – | 2 | – | 2 | – | V |
| Low Level Input Voltage | $V_{IL}$ | – | – | 4.5 to 5.5 | – | – | 0.8 | – | 0.8 | – | 0.8 | V |
| High Level Output Voltage CMOS Loads | $V_{OH}$ | $V_{IH}$ or $V_{IL}$ | −0.02 | 4.5 | 4.4 | – | – | 4.4 | – | 4.4 | – | V |
| High Level Output Voltage TTL Loads | | | −4 | 4.5 | 3.98 | – | – | 3.84 | – | 3.7 | – | V |
| Low Level Output Voltage CMOS Loads | $V_{OL}$ | $V_{IH}$ or $V_{IL}$ | 0.02 | 4.5 | – | – | 0.1 | – | 0.1 | – | 0.1 | V |
| Low Level Output Voltage TTL Loads | | | 4 | 4.5 | – | – | 0.26 | – | 0.33 | – | 0.4 | V |
| Input Leakage Current | $I_I$ | $V_{CC}$ and GND | 0 | 5.5 | – | – | ±0.1 | – | ±1 | – | ±1 | µA |
| Quiescent Device Current | $I_{CC}$ | $V_{CC}$ or GND | 0 | 5.5 | – | – | 8 | – | 80 | – | 160 | µA |
| Additional Quiescent Device Current Per Input Pin: 1 Unit Load | $\Delta I_{CC}$ (Note 3) | $V_{CC}$ −2.1 | – | 4.5 to 5.5 | – | 100 | 360 | – | 450 | – | 490 | µA |

NOTE:

3. For dual−supply systems theoretical worst case ($V_I$ = 2.4V, $V_{CC}$ = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

| INPUT | UNIT LOADS |
|---|---|
| D | 0.4 |
| CP, OE | 1.5 |
| STR | 1.0 |

NOTE: Unit Load is $\Delta I_{CC}$ limit specified in DC Electrical Table, e.g., 360µA max at 25°C.

### Prerequisite for Switching Specifications

| CHARACTERISTIC | SYMBOL | $V_{CC}$ (V) | 25°C MIN | 25°C MAX | −40°C TO 85°C MIN | −40°C TO 85°C MAX | −55°C TO 125°C MIN | −55°C TO 125°C MAX | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| **HC TYPES** | | | | | | | | | |
| CP Pulse Width | $t_W$ | 2 | 80 | – | 100 | – | 120 | – | ns |
| | | 4.5 | 16 | – | 20 | – | 24 | – | ns |
| | | 6 | 14 | – | 17 | – | 20 | – | ns |
| STR Pulse Width | $t_{WH}$ | 2 | 80 | – | 100 | – | 120 | – | ns |
| | | 4.5 | 16 | – | 20 | – | 24 | – | ns |
| | | 6 | 14 | – | 17 | – | 20 | – | ns |

**Prerequisite for Switching Specifications** **(Continued)**

| CHARACTERISTIC | SYMBOL | $V_{CC}$ (V) | 25°C | | −40°C TO 85°C | | −55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | |
| Data Set−up Time | $t_{SU}$ | 2 | 50 | – | 65 | – | 75 | – | ns |
| | | 4.5 | 10 | – | 13 | – | 15 | – | ns |
| | | 6 | 9 | – | 11 | – | 13 | – | ns |
| Data Hold Time | $t_H$ | 2 | 3 | – | 3 | – | 3 | – | ns |
| | | 4.5 | 3 | – | 3 | – | 3 | – | ns |
| | | 6 | 3 | – | 3 | – | 3 | – | ns |
| STR Set−up Time | $t_{SU}$ | 2 | 100 | – | 125 | – | 150 | – | ns |
| | | 4.5 | 20 | – | 25 | – | 30 | – | ns |
| | | 6 | 17 | – | 21 | – | 26 | – | ns |
| STR Hold Time | $t_H$ | 2 | 0 | – | 0 | – | 0 | – | ns |
| | | 4.5 | 0 | – | 0 | – | 0 | – | ns |
| | | 6 | 0 | – | 0 | – | 0 | – | ns |
| Maximum CP Frequency | $f_{CL\ (MAX)}$ | 2 | 6 | – | 5 | – | 4 | – | MHz |
| | | 4.5 | 30 | – | 24 | – | 20 | – | MHz |
| | | 6 | 35 | – | 28 | – | 24 | – | MHz |
| **HCT TYPES** | | | | | | | | | |
| CP Pulse Width | $t_W$ | 4.5 | 16 | – | 20 | – | 24 | – | ns |
| STR Pulse Width | $t_{WH}$ | 4.5 | 16 | – | 20 | – | 24 | – | ns |
| Data Set−up Time | $t_{SU}$ | 4.5 | 10 | – | 13 | – | 15 | – | ns |
| Data Hold Time | $t_H$ | 4.5 | 4 | – | 4 | – | 4 | – | ns |
| STR Set−up Time | $t_{SU}$ | 4.5 | 20 | – | 25 | – | 30 | – | ns |
| STR Hold Time | $t_H$ | 4.5 | 0 | – | 0 | – | 0 | – | ns |
| Maximum CP Frequency | $f_{CL\ (MAX)}$ | 4.5 | 30 | – | 24 | – | 20 | – | MHz |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | −40°C TO 85°C | | −55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| **HC TYPES** | | | | | | | | | | | |
| Propagation Delay Time (Figure 1) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | – | – | 150 | – | 190 | – | 225 | ns |
| CP to $QS_1$ | | | 4.5 | – | – | 30 | – | 38 | – | 45 | ns |
| | | $C_L$ =15pF | 5 | – | 12 | – | – | – | – | – | ns |
| | | $C_L$ = 50pF | 6 | – | – | 26 | – | 33 | – | 38 | ns |
| CP to $QS_2$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | – | – | 135 | – | 170 | – | 205 | ns |
| | | | 4.5 | – | – | 27 | – | 34 | – | 41 | ns |
| | | $C_L$ =15pF | 5 | – | 11 | – | – | – | – | – | ns |
| | | $C_L$ = 50pF | 6 | – | – | 23 | – | 29 | – | 35 | ns |
| CP to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | – | – | 195 | – | 245 | – | 295 | ns |
| | | | 4.5 | – | – | 39 | – | 49 | – | 59 | ns |
| | | | 5 | – | 16 | – | – | – | – | – | ns |
| | | | 6 | – | – | 33 | – | 42 | – | 50 | ns |
| STR to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 2 | – | – | 180 | – | 225 | – | 270 | ns |
| | | | 4.5 | – | – | 36 | – | 45 | – | 54 | ns |
| | | | 6 | – | – | 31 | – | 38 | – | 46 | ns |

**Switching Specifications** Input $t_r$, $t_f$ = 6ns **(Continued)**

| PARAMETER | SYMBOL | TEST CONDITIONS | $V_{CC}$ (V) | 25°C | | | −40°C TO 85°C | | −55°C TO 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| Output Enable to $Q_n$ | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 2 | – | – | 175 | – | 220 | – | 265 | ns |
| | | | 4.5 | – | – | 35 | – | 44 | – | 53 | ns |
| | | | 6 | – | – | 30 | – | 37 | – | 45 | ns |
| Output Disable to $Q_n$ | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 2 | – | – | 125 | – | 155 | – | 190 | ns |
| | | | 4.5 | – | – | 25 | – | 31 | – | 38 | ns |
| | | | 6 | – | – | 21 | – | 26 | – | 32 | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 2 | – | – | 75 | – | 95 | – | 110 | ns |
| | | | 4.5 | – | – | 15 | – | 19 | – | 22 | ns |
| | | | 6 | – | – | 13 | – | 16 | – | 19 | ns |
| Output Disabling Time | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ =15pF | 5 | – | 10 | – | – | – | – | – | ns |
| Maximum CP Frequency | $f_{MAX}$ | $C_L$ =15pF | 5 | – | 60 | – | – | – | – | – | MHz |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | – | – | – | 10 | – | 10 | – | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | $C_{PD}$ | $C_L$ =15pF | 5 | – | 90 | – | – | – | – | – | pF |
| Three−State Output Capacitance | $C_O$ | $C_L$ = 50pF | – | – | – | 15 | – | 15 | – | 15 | pF |
| **HCT TYPES** | | | | | | | | | | | |
| Propagation Delay Time (Figure 1) | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | – | – | 39 | – | – | – | – | ns |
| CP to $QS_1$ | | $C_L$ =15pF | 5 | – | 16 | – | – | – | – | – | ns |
| CP to $QS_2$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | – | – | 36 | – | – | – | – | ns |
| | | $C_L$ =15pF | 5 | – | 15 | – | – | – | – | – | ns |
| CP to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | – | – | 43 | – | – | – | – | ns |
| | | $C_L$ =15pF | 5 | – | 18 | – | – | – | – | – | ns |
| STR to $Q_n$ | $t_{PLH}$, $t_{PHL}$ | $C_L$ = 50pF | 4.5 | – | – | 39 | – | – | – | – | ns |
| Output Enable to $Q_n$ | $t_{PZH}$, $t_{PZL}$ | $C_L$ = 50pF | 4.5 | – | – | 35 | – | – | – | – | ns |
| Output Disable to $Q_n$ | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ = 50pF | 4.5 | – | – | 35 | – | – | – | – | ns |
| Output Transition Time | $t_{TLH}$, $t_{THL}$ | $C_L$ = 50pF | 4.5 | – | – | 15 | – | – | – | – | ns |
| Output Disabling Time | $t_{PHZ}$, $t_{PLZ}$ | $C_L$ =15pF | 5 | – | 14 | – | – | – | – | – | ns |
| Maximum CP Frequency | $f_{MAX}$ | $C_L$ =15pF | 5 | – | 60 | – | – | – | – | – | MHz |
| Input Capacitance | $C_{IN}$ | $C_L$ = 50pF | – | – | – | 10 | – | 10 | – | 10 | pF |
| Power Dissipation Capacitance (Notes 4, 5) | $C_{PD}$ | $C_L$ =15pF | 5 | – | 110 | – | – | – | – | – | pF |
| Three−State Output Capacitance | $C_O$ | $C_L$ = 50pF | – | – | – | 15 | – | 15 | – | 15 | pF |

NOTES:

4. $C_{PD}$ is used to determine the dynamic power consumption, per register.
5. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where $f_i$ = Input Frequency, $C_L$ = Output Load Capacitance, $V_{CC}$ = Supply Voltage.

## Test Circuits and Waveforms

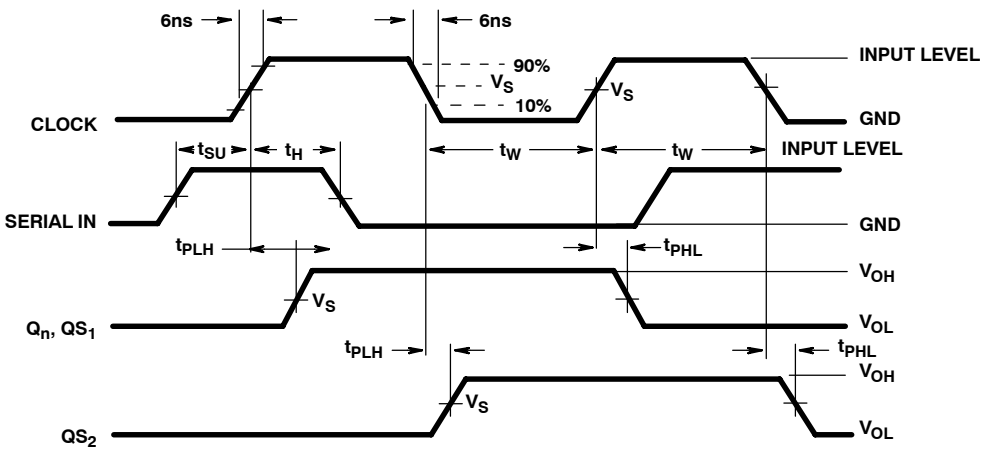



**FIGURE 1. DATA PROPAGATION DELAYS, SET–UP AND HOLD TIMES**

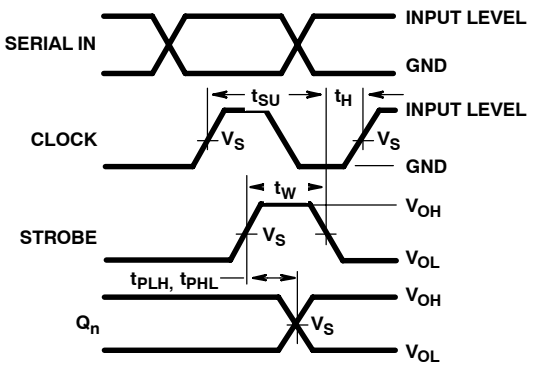



**FIGURE 2. STROBE PROPAGATION DELAYS AND SET–UP AND HOLD TIMES**

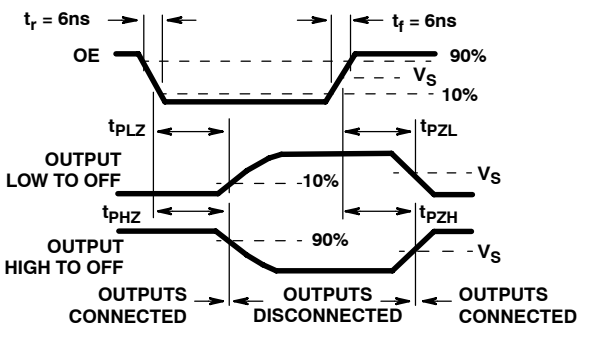



**FIGURE 3. ENABLE AND DISABLE TIMES**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CD54HC4094F3A | ACTIVE | CDIP | J | 16 | 1 | Non-RoHS & Green | SNPB | N / A for Pkg Type | -55 to 125 | CD54HC4094F3A | Samples |
| CD74HC4094E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HC4094E | Samples |
| CD74HC4094M | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094M96G3 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | SN | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094M96G4 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094MT | ACTIVE | SOIC | D | 16 | 250 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094NSR | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094NSRE4 | ACTIVE | SO | NS | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HC4094M | Samples |
| CD74HC4094PW | ACTIVE | TSSOP | PW | 16 | 90 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4094 | Samples |
| CD74HC4094PWR | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HJ4094 | Samples |
| CD74HC4094PWRE4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4094 | Samples |
| CD74HC4094PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HJ4094 | Samples |
| CD74HCT4094E | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT4094E | Samples |
| CD74HCT4094EE4 | ACTIVE | PDIP | N | 16 | 25 | RoHS & Green | NIPDAU | N / A for Pkg Type | -55 to 125 | CD74HCT4094E | Samples |
| CD74HCT4094M | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4094M | Samples |
| CD74HCT4094M96 | ACTIVE | SOIC | D | 16 | 2500 | RoHS & Green | NIPDAU \| SN | Level-1-260C-UNLIM | -55 to 125 | HCT4094M | Samples |
| CD74HCT4094ME4 | ACTIVE | SOIC | D | 16 | 40 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -55 to 125 | HCT4094M | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2) RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF CD54HC4094, CD74HC4094 :**

- Catalog: CD74HC4094
- Military: CD54HC4094

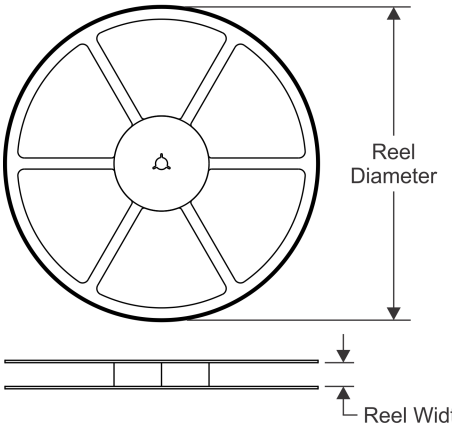
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

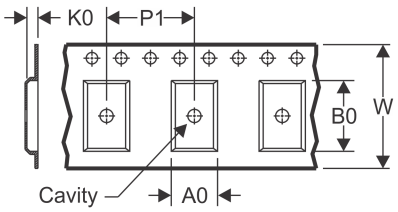
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

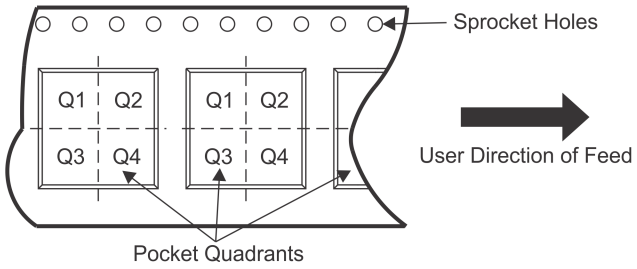



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

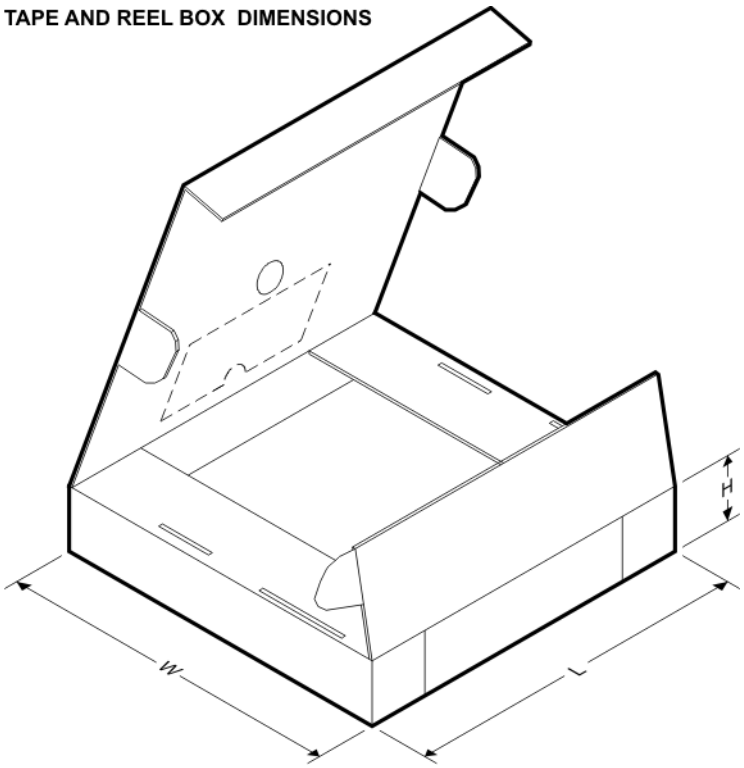
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CD74HC4094M96 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC4094M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC4094M96G3 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC4094M96G4 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HC4094NSR | SO | NS | 16 | 2000 | 330.0 | 16.4 | 8.2 | 10.5 | 2.5 | 12.0 | 16.0 | Q1 |
| CD74HC4094PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC4094PWR | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HC4094PWRG4 | TSSOP | PW | 16 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| CD74HCT4094M96 | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |
| CD74HCT4094M96 | SOIC | D | 16 | 2500 | 330.0 | 16.8 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

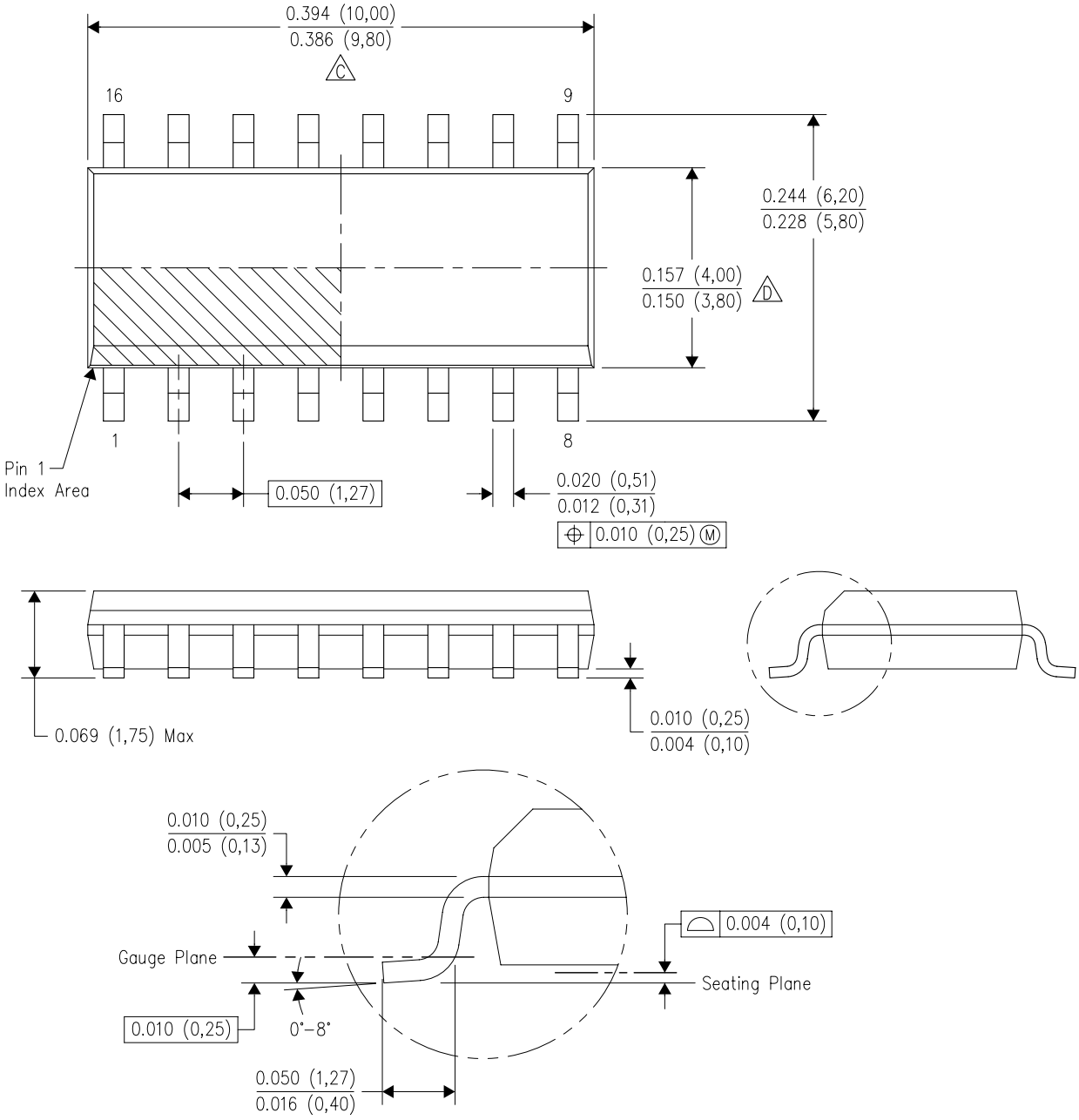
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

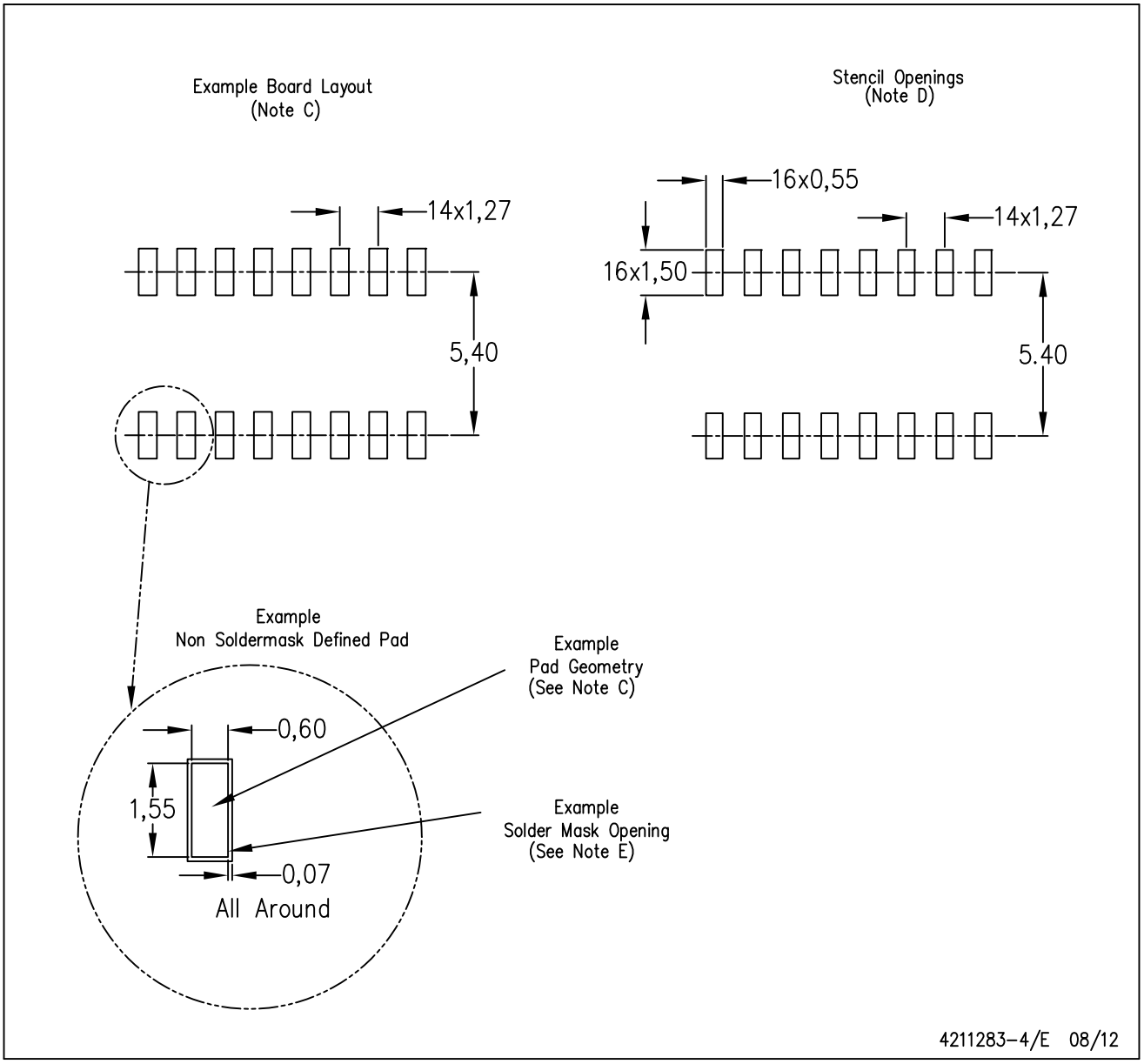
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CD74HC4094M96 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| CD74HC4094M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC4094M96G3 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |
| CD74HC4094M96G4 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HC4094NSR | SO | NS | 16 | 2000 | 853.0 | 449.0 | 35.0 |
| CD74HC4094PWR | TSSOP | PW | 16 | 2000 | 853.0 | 449.0 | 35.0 |
| CD74HC4094PWR | TSSOP | PW | 16 | 2000 | 364.0 | 364.0 | 27.0 |
| CD74HC4094PWRG4 | TSSOP | PW | 16 | 2000 | 853.0 | 449.0 | 35.0 |
| CD74HCT4094M96 | SOIC | D | 16 | 2500 | 333.2 | 345.9 | 28.6 |
| CD74HCT4094M96 | SOIC | D | 16 | 2500 | 364.0 | 364.0 | 27.0 |

D (R–PDSO–G16) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



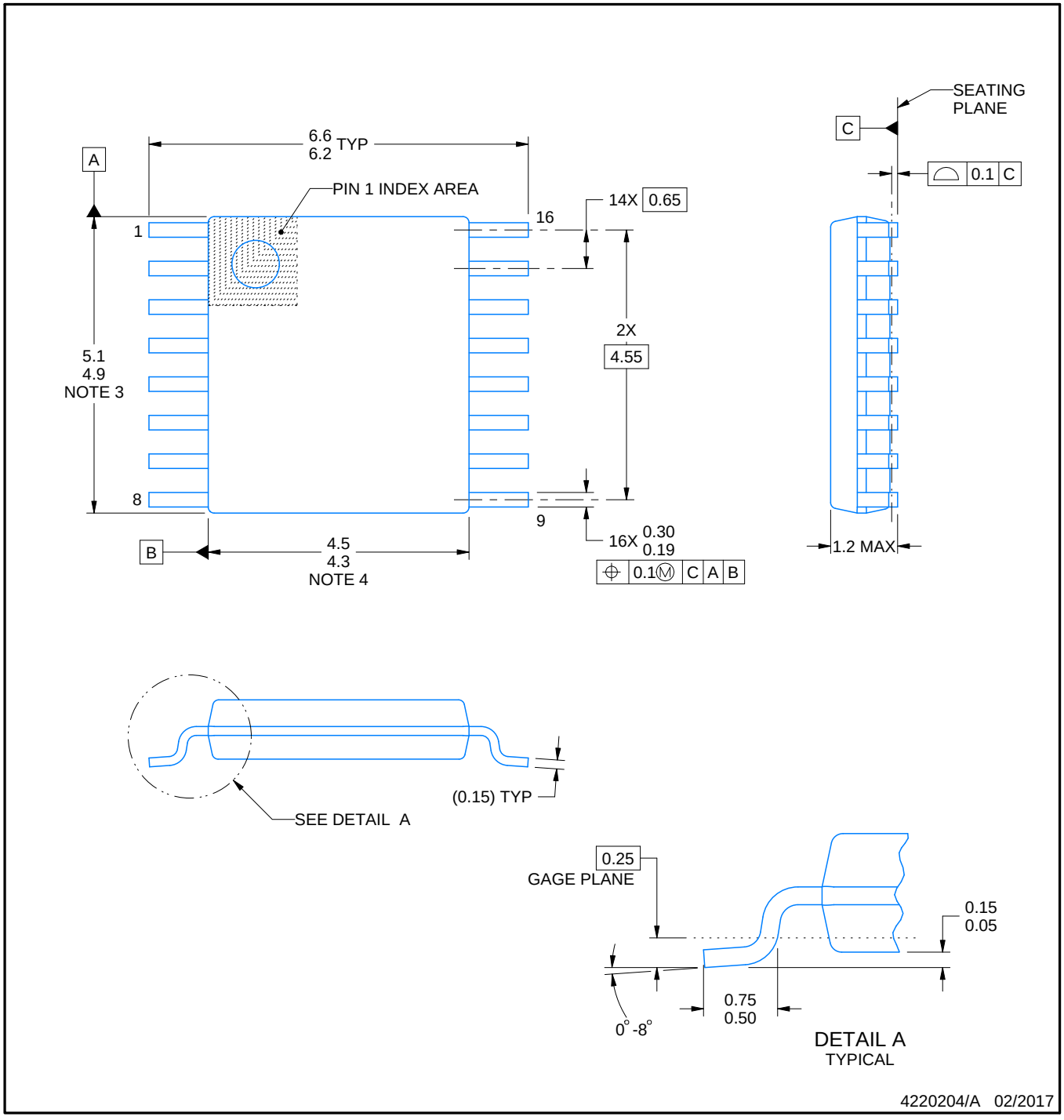

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

# PACKAGE OUTLINE

## PW0016A

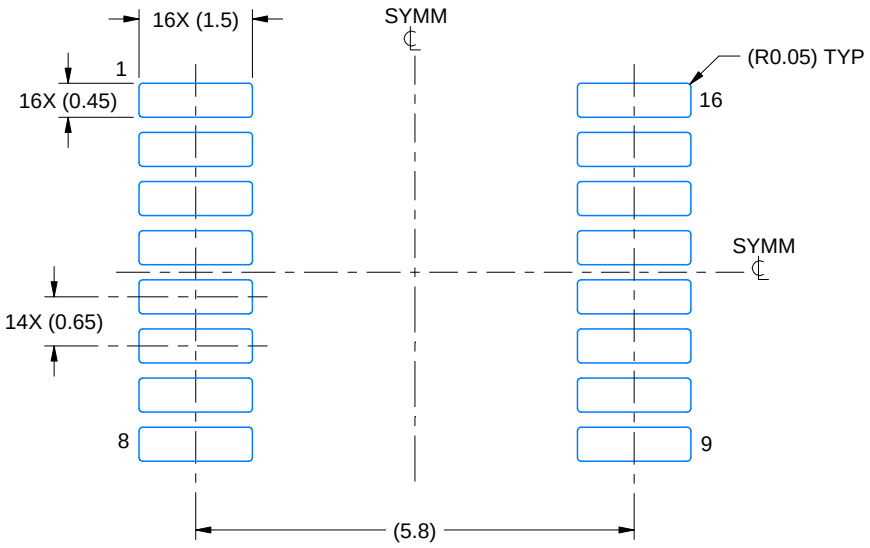
## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

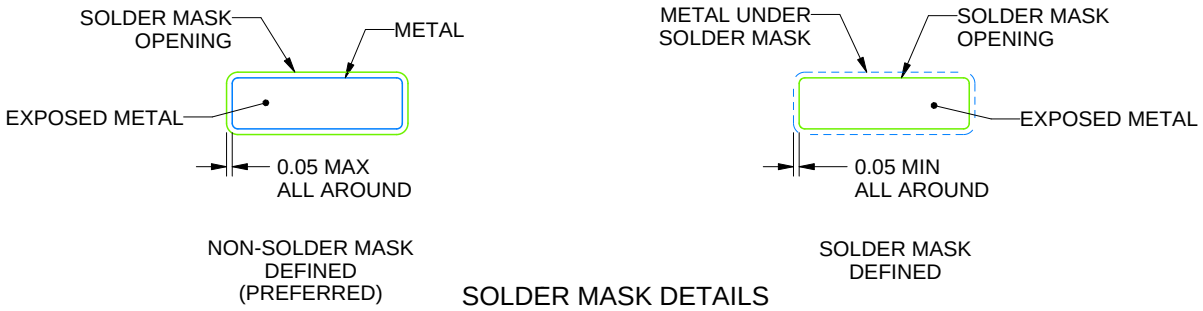



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

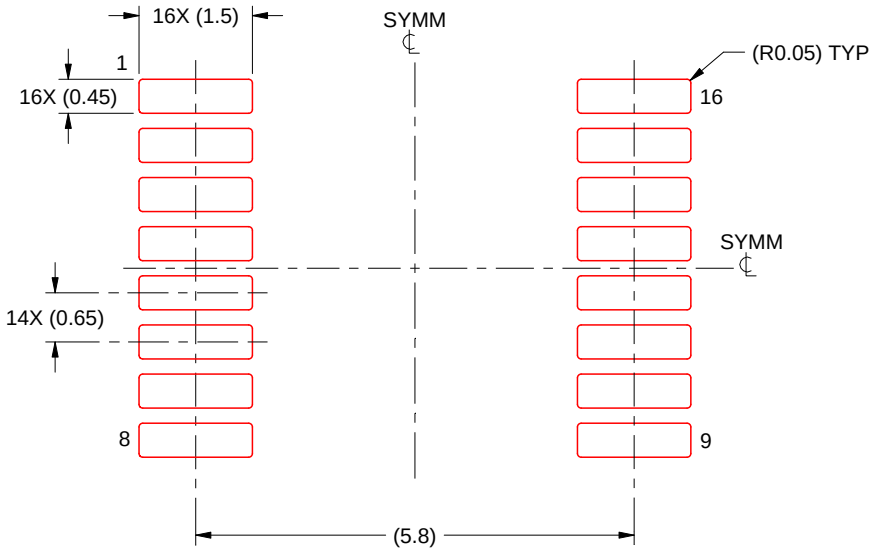



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

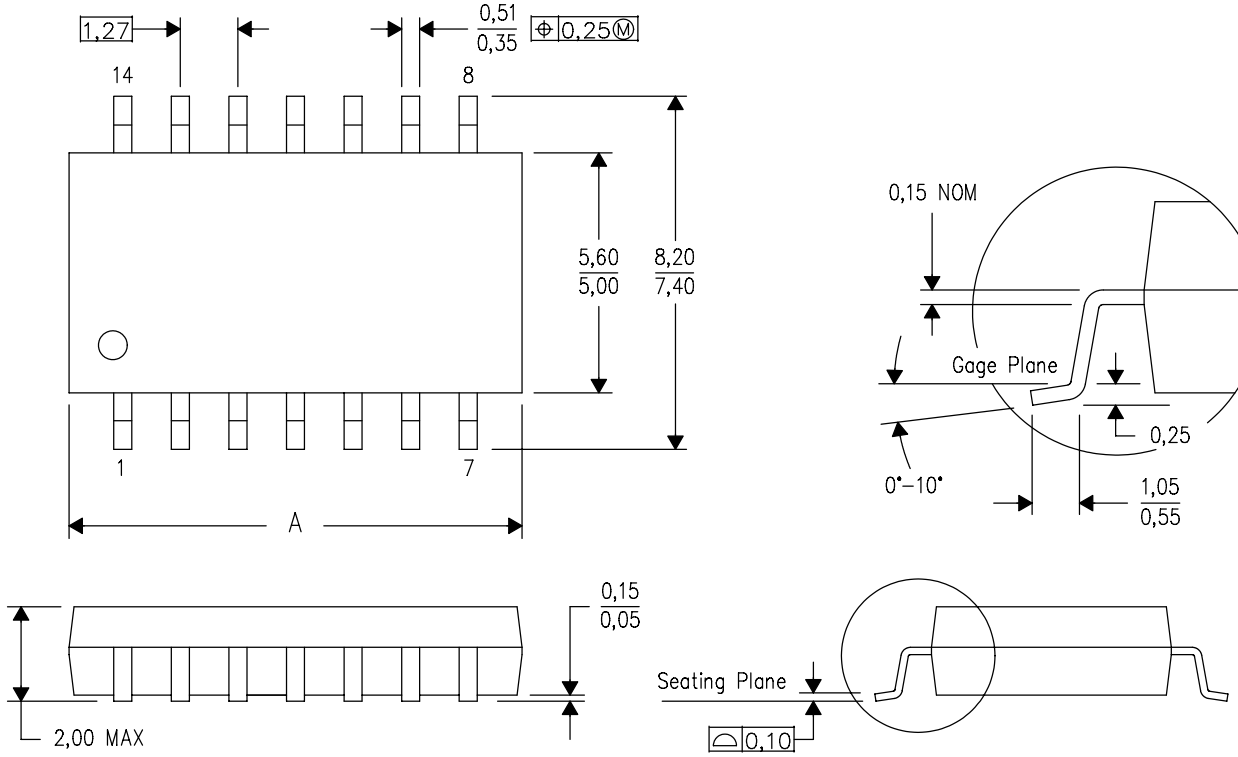
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

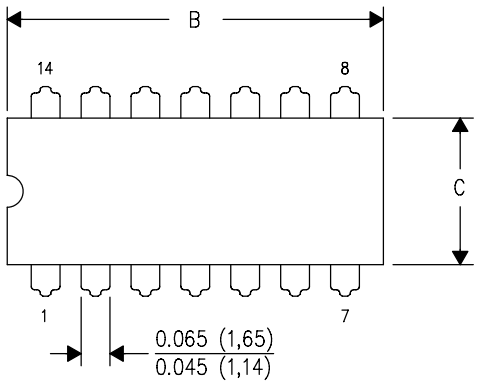
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

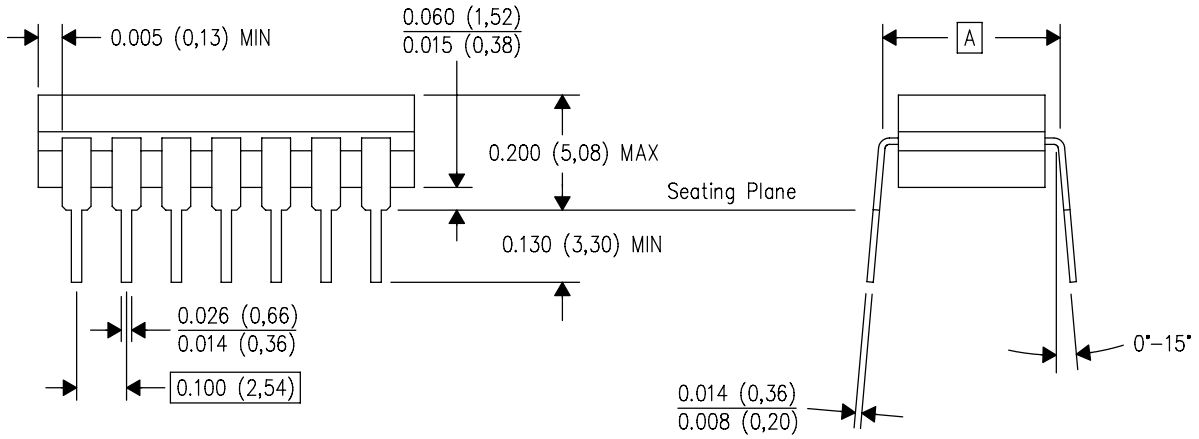
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



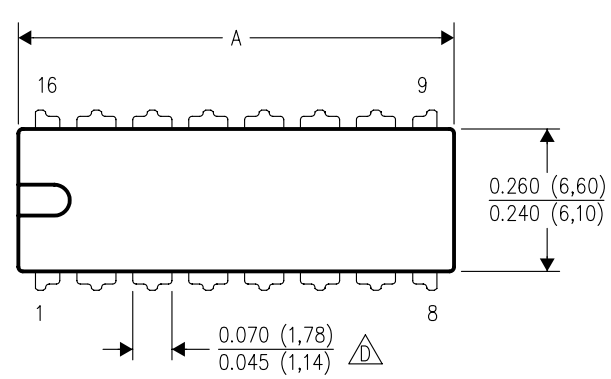

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

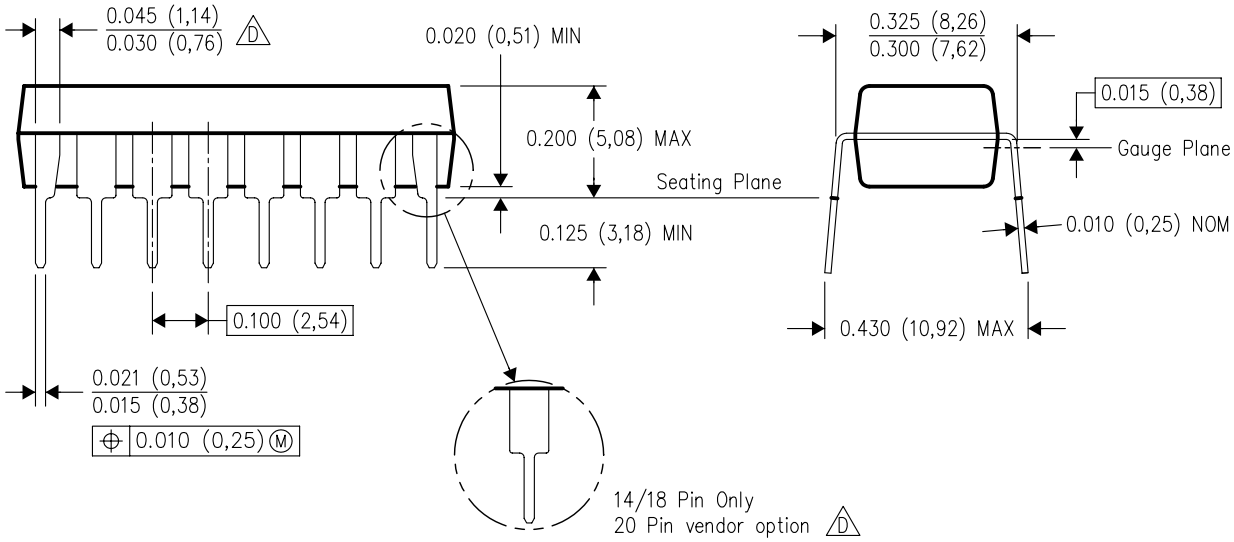
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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