SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

- Operation from Very Slow Edges
- Improved Line-Receiving Characteristics
- High Noise Immunity

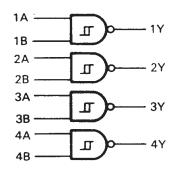
description

Each circuit functions as a 2-input NAND gate, but because of the Schmitt action, it has different input threshold levels for positive (V_{T+}) and for negative going (V_{T-}) signals.

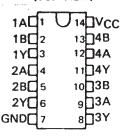
These circuits are temperature-compensated and can be triggered from the slowest of input ramps and still give clear, jitter-free output signals.

The SN54132, SN54LS132, and SN54S132 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74132, SN74LS132, and SN74S132 are characterized for operation from 0°C to 70°C.

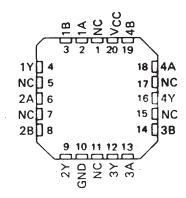
logic diagram (positive logic)



SN54132, SN54LS132, SN54S132 . . . J OR W PACKAGE SN74132 . . . N PACKAGE SN74LS132, SN74S132 . . . D OR N PACKAGE (TOP VIEW)

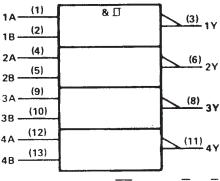


SN54LS132, SN54S132 . . . FK PACKAGE (TOP VIEW)



NC-No internal connection

logic symbol†



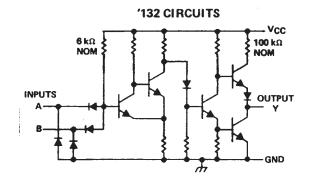
positive logic: $Y = \overline{AB}$ or $Y = \overline{A} + \overline{B}$

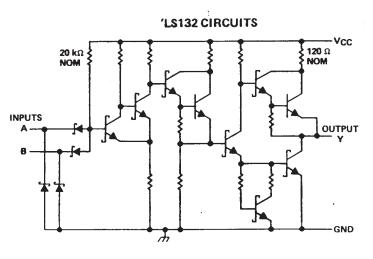
Pin numbers shown are for D, J, N, and W packages.

[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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schematics





'S132 CIRCUITS -vcc 2.8 kΩ NOM **50** Ω NOM **INPUTS** OUTPUT **GND**

Resistor values shown are nominal.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, VCC (see Note	-1)	7 V
Input voltage: '132, 'S132		5.5 V
Operating free-air temperature	: SN54'	55°C to 125°C
	SN74'	\dots 0°C to 70°C
Storage temperature range		-65° C to 150° C

NOTE 1: Voltages values are with respect to network ground terminal.



recommended operating conditions

			SN54132			SN74132			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	٧	
Іон	High-level output current			- 0.8			- 0.8	mA	
IOL	Low-level output current			16			16	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	rions†	MIN	TYP‡	MAX	UNIT
V _{T+}	V _{CC} = 5 V			1.5	1.7	2	V
v _{T-}	V _{CC} = 5 V			0.6	0.9	1.1	V
V _{hys} (V _{T+} -V _{T-})	V _{CC} = 5 V			0.4	0.8		V
ViK	V _{CC} = MIN,	I _I = - 12 mA				- 1.5	V
VOH	V _{CC} = MIN,	V ₁ = 0.6 V,	t _{OH} = - 0.8 mA	2.4	3.4		V
VOL	V _{CC} = MIN,	V ₁ = 2 V,	IOL = 16 mA		0.2	0.4	V
I _{T+}	V _{CC} = 5 V,	V ₁ = V _{T+}			- 0.43		mΑ
1 _T _	V _{CC} = 5 V,	Λ1 = Λ ^L			- 0.56		mA
l ₁	V _{CC} = MAX,	V ₁ = 5.5 V				1	mA
ΊΗ	V _{CC} = MAX,	V ₁ = 2.4 V			-	40	μА
li L	V _{CC} = MAX,	V _{IL} = 0.4 V			- 0.8	- 1.2	mA
los§	V _{CC} = MAX			- 18	•	- 55	mA
ГССН	V _{CC} = MAX				15	24	mA
ICCL	V _{CC} = MAX				26	40	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, V_{CC} = 5 V, T_A = 25°C (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
^t PLH	Any		$R_1 = 400 \Omega_s$	C ₁ = 15 pF		15	22	ns
^t PHL	Atty		11 - 400 38,			15	22	ns

[‡] All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$. § Not more than one output should be shorted at a time.

SN54LS132, SN74LS132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

recommended operating conditions

		S	SN54LS132			SN74LS132			
		MIN	NOM	MAX	MIN	MOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
ЮН	High-level output current			- 0.4			-0.4	mA	
IOL	Low-level output current		***	4			8	mA	
TA	Operating free-air temperature	55		125	0		70	°c	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	riouet	S	N54LS1	32	S	N74LS1	32	UNIT
FANAMETER		TEST CONDI	TIONS	MIN	TYP‡	MAX	MIN	TYP#	MAX	UNIT
V _{T+}	V _{CC} = 5 V			1.4	1.6	1.9	1.4	1.6	1.9	V
∨ _{T−}	V _{CC} = 5 V			0.5	0.8	1	0.5	8.0	1	V
V _{hγs} (V _{T +} -V _{T -})	V _{CC} = 5 V			0.4	0.8		0.4	8.0		V
VIK	V _{CC} = MIN,	I _I = - 18 mA				- 1.5			- 1.5	V
Voн	V _{CC} = MIN,	V ₁ = 0.5 V,	IOH = - 0.4 mA	2.5	3.4		2.7	3.4		٧
VOL	V _{CC} = MIN,	V _I = 1.9 V	IOL = 4 mA		0.25	0.4		0.25	0.4	V
VOL	v CC = 141114,	V1 - 1.5 V	IOL = 8 mA					0.35	0.5]
1 _{T+}	V _{CC} = 5 V,	V _I = V _{T+}		_	- 0.14		-	- 0.14		mA
IT-	V _{CC} = 5 V,	VI = VT_		-	- 0.18		-	- 0.18		mA
l _l	V _{CC} = MAX,	V _I = 7 V			-	0.1			0.1	mA
ЧН	V _{CC} = MAX,	V ₁ = 2.7 V				20			20	μА
11L	V _{CC} = MAX,	V _{IL} = 0.4 V				- 0.4			- 0.4	mA
os §	V _{CC} = MAX		· · · · · · · · · · · · · · · · · · ·	- 20		- 100	- 20		- 100	mA
Iссн	V _{CC} = MAX				5.9	11		5.9	11	mA
¹ CCL	V _{CC} = MAX				8.2	14		8.2	14	mA

[†] For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions,

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see figure 1)

	PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST COM	NDITIONS	MIN	TYP	MAX	UNIT
	^t PLH	Anv	_	$R_1 = 2 k\Omega$,	C ₁ = 15 pF		15	22	ns
1	^t PHL_	,,	'	11, 2 11, 2	OL = 13 b1		15	22	ns

[‡] All typical values are at V_{CC} = 5 V, T_A = 25° C.

[§] Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second

SN54S132, SN74S132 QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

SDLS047 - DECEMBER 1983 - REVISED MARCH 1988

recommended operating conditions

			SN54S132			SN74S132			
		MIN	NOM	MAX	MIN	NOM	MAX	UNIT	
Vcc	Supply voltage	4.5	5	5.5	4.75	5	5.25	V	
Іон	High-level output current			– 1			– 1	mA	
IOL	Low-level output current			20			20	mA	
TA	Operating free-air temperature	- 55		125	0		70	°C	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDIT	uovet		SN54S1	32	:	SN74S1	32	UNIT
PARAMETER		TEST CONDIT	ION2.	MIN	TYP‡	MAX	MIN	TYP‡	MAX	ONT
V _{T+}	V _{CC} = 5 V			1.6	1.77	1.9	1.6	1.77	1.9	٧
V _T _	V _{CC} = 5 V			1.1	1.22	1.4	1.1	1.22	1.4	٧
V _{hys} (V _{T +} -V _{T -})	V _{CC} = 5 V			0.2	0.55		0.2	0.55		٧
VIK	V _{CC} = MIN,	I ₁ = - 18 mA				- 1.2			- 1.2	V
Voн	V _{CC} = MIN,	V ₁ = 1.1 V,	IOH = - 1 mA	2.5	3.4		2.7	3.4		٧
VOL	V _{CC} = MIN,	$V_1 = 1.9 V$,	IOL = 20 mA			0.5			0.5	V
I _{T+}	V _{CC} = 5 V,	V1 = VT+			- 0.9			- 0.9		mA
1T_	V _{CC} = 5 V,	VI = VT_			- 1.1			- 1.1		mA
lį	V _{CC} = MAX,	V _I = 5.5 V				1			1	mA
ЧН	V _{CC} = MAX,	V ₁ = 2.7 V				50			50	, μΑ
115	V _{CC} = MAX,	V _{1L} = 0.5 V				- 2			- 2	mΑ
los§	V _{CC} = MAX			- 40		- 100	- 40		– 100	mΑ
ССН	V _{CC} = MAX				28	44		28	44	mA
ICCL	V _{CC} = MAX				44	68		44	68	mA

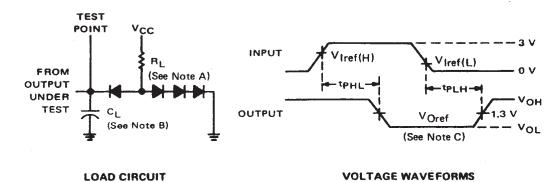
 $^{^\}dagger$ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

switching characteristics, $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$ (see figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CON	DITIONS	MIN	TYP	MAX	UNIT
t _{PLH}	A or B	V	$R_1 = 280 \Omega_s$	C ₁ = 15 pF		7	10.5	ns
tPHL	70,0	'	11 - 200 14,	O[- 13 br		8.5	13	nis

[‡] All typical values are at V_{CC} = 5 V, T_A = 25°C. § Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

PARAMETER MEASUREMENT INFORMATION



NOTES: A. All diodes are 1N3064 or equivalent.

B. C_L includes probe and jig capacitance.

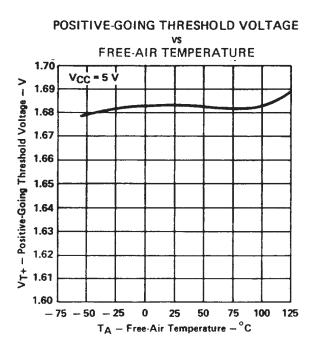
C. Generator characteristics and reference voltages are:

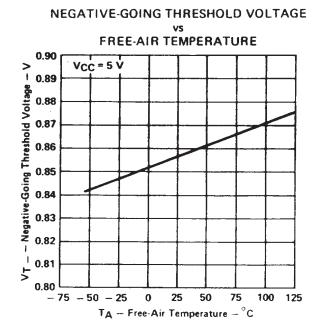
	G	enerator C	haracteris	tics	Reference Voltages					
	Zout	PRR	tr	tf	VI ref(H)	VI ref(L)	VO ref			
SN54'/SN74'	50	1 MHz	10 ns	10 ns	1.7 V	0.9 V	1.5 V			
SN54LS'/SN74LS'	50	1 MHz	15 ns	6 ns	1.6 V	0.8 V	1.3 V			
'S132	50	1 MHz	2.5 ns	2.5 ns	1.8 V	1.2 V	1.5 V			

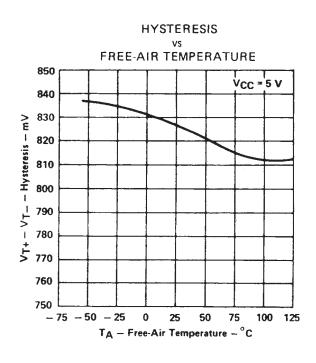
FIGURE 1

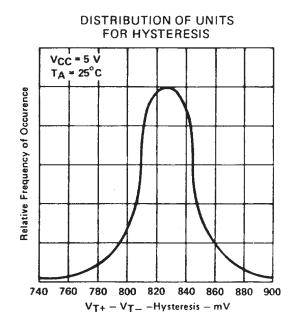


TYPICAL CHARACTERISTICS OF '132 CIRCUITS

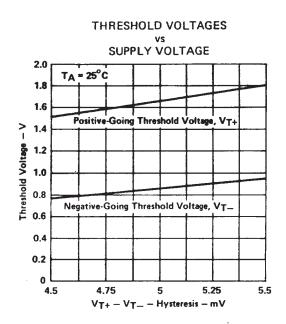


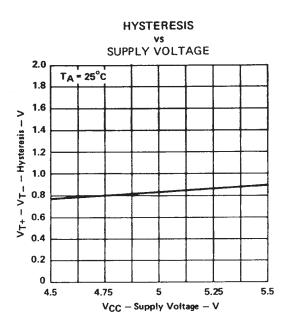


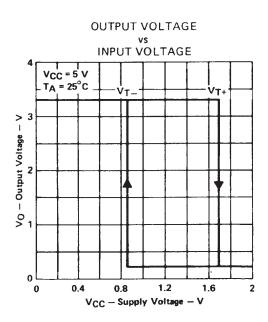




TYPICAL CHARACTERISTICS OF '132 CIRCUITS





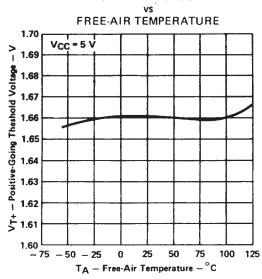


[†] Data for temperatures below 0° C and 70° C and supply below 4.75 V and above 5.25 V are applicable for SN54132 only.

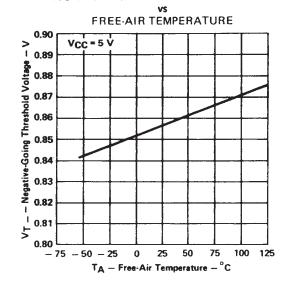


TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS

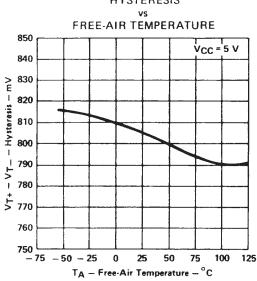
POSITIVE-GOING THRESHOLD VOLTAGE



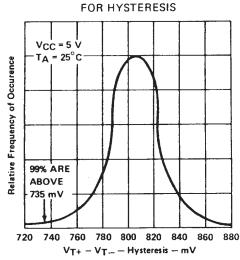
NEGATIVE-GOING THRESHOLD VOLTAGE



HYSTERESIS

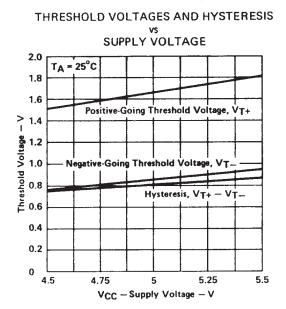


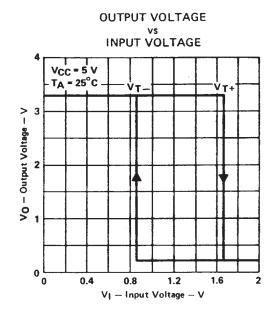
DISTRIBUTION OF UNITS



Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS132 only.

TYPICAL CHARACTERISTICS OF 'LS132 CIRCUITS

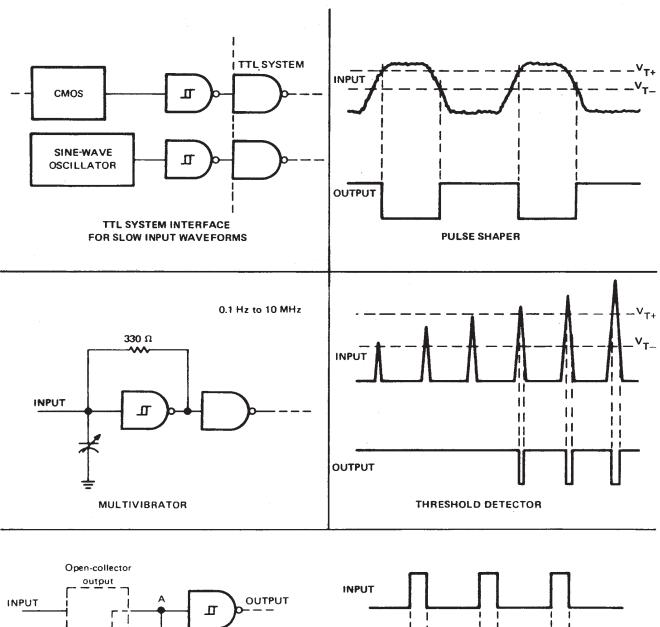


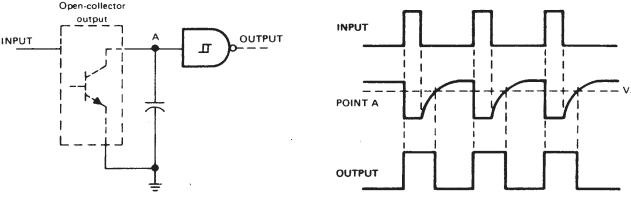


[†] Data for temperatures below 0°C and above 70°C and supply voltages below 4.75 V and above 5.25 V are applicable for SN54LS132 only.



TYPICAL APPLICATION DATA













9-Oct-2020

PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
7600401CA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401CA SNJ54LS132J	Samples
7600401DA	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
7600401DA	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
JM38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Sample
JM38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Sample
M38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Sample
M38510/31303BCA	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	JM38510/ 31303BCA	Sample
SN54LS132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54LS132J	Sample
SN54LS132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54LS132J	Sample
SN54S132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54S132J	Sample
SN54S132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SN54S132J	Sample
SN74LS132D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Sample
SN74LS132D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Sample
SN74LS132DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Sample
SN74LS132DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	LS132	Sample
SN74LS132N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS132N	Sample
SN74LS132N	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	0 to 70	SN74LS132N	Sample





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Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LS132NSR	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS132	Samples
SN74LS132NSR	ACTIVE	so	NS	14	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	0 to 70	74LS132	Samples
SNJ54LS132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 132FK	Samples
SNJ54LS132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54LS 132FK	Samples
SNJ54LS132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401CA SNJ54LS132J	Samples
SNJ54LS132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401CA SNJ54LS132J	Samples
SNJ54LS132W	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
SNJ54LS132W	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	7600401DA SNJ54LS132W	Samples
SNJ54S132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 132FK	Samples
SNJ54S132FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 125	SNJ54S 132FK	Samples
SNJ54S132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S132J	Samples
SNJ54S132J	ACTIVE	CDIP	J	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S132J	Samples
SNJ54S132W	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S132W	Samples
SNJ54S132W	ACTIVE	CFP	W	14	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	SNJ54S132W	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.



PACKAGE OPTION ADDENDUM

9-Oct-2020

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN54LS132. SN74LS132:

Catalog: SN74LS132

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Military: SN54LS132

NOTE: Qualified Version Definitions:

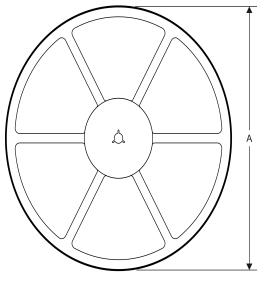
- Catalog TI's standard catalog product
- Military QML certified for Military and Defense Applications

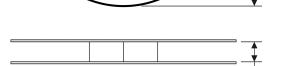
PACKAGE MATERIALS INFORMATION

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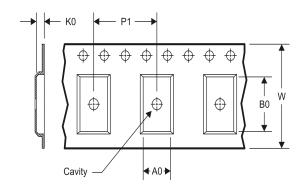
TAPE AND REEL INFORMATION

REEL DIMENSIONS





TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
В0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing		SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS132DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LS132NSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

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*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LS132DR	SOIC	D	14	2500	367.0	367.0	38.0
SN74LS132NSR	SO	NS	14	2000	367.0	367.0	38.0

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a metal lid.
- D. Falls within JEDEC MS-004



MECHANICAL DATA

NS (R-PDSO-G**)

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. This package can be hermetically sealed with a ceramic lid using glass frit.
- D. Index point is provided on cap for terminal identification only.
- E. Falls within MIL STD 1835 GDFP1-F14



CERAMIC DUAL IN LINE PACKAGE



Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.

4040083-5/G





CERAMIC DUAL IN LINE PACKAGE



- 1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. This package is hermitically sealed with a ceramic lid using glass frit.
- His package is remitted by sealed with a ceramic its using glass mit.
 Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
 Falls within MIL-STD-1835 and GDIP1-T14.



CERAMIC DUAL IN LINE PACKAGE



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.



D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC-7351 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
- The 20 pin end lead shoulder width is a vendor option, either half or full width.



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