

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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Not recommended  
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# HD74LS390

## Dual Decade Counters

REJ03D0485-0400  
Rev.4.00  
May 10, 2006

This circuit contains eight master-slave flip-flops and additional gating to implement two individual four-bit counters. The HD74LS390 incorporates dual divide-by-two and divide-by-five counters, which can be used to implement cycle lengths equal to any whole and / or cumulative multiples of 2 and / or 5 up to divide-by-100. When connected as a binary counter, the separate divide-by-two circuit can be used to provide symmetry (a square wave) at the final output stage.

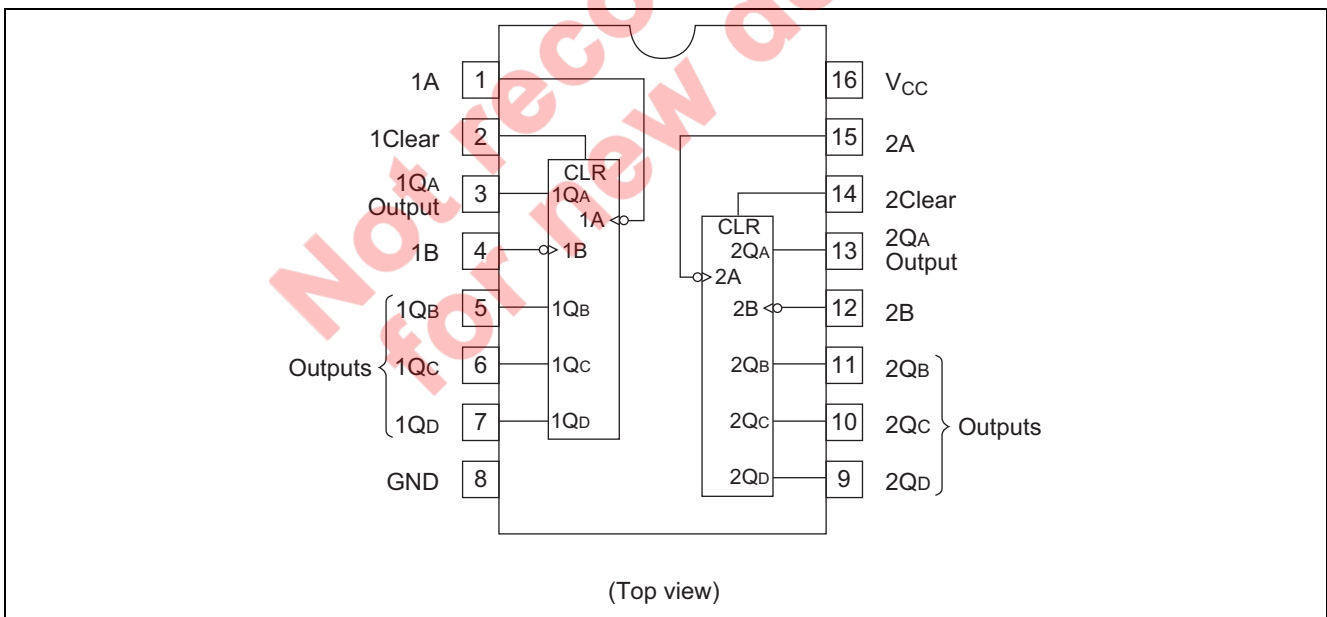
### Features

- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74LS390P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74LS390FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

### Pin Arrangement



## Function Table

### BCD Count Sequence (Notes 1)

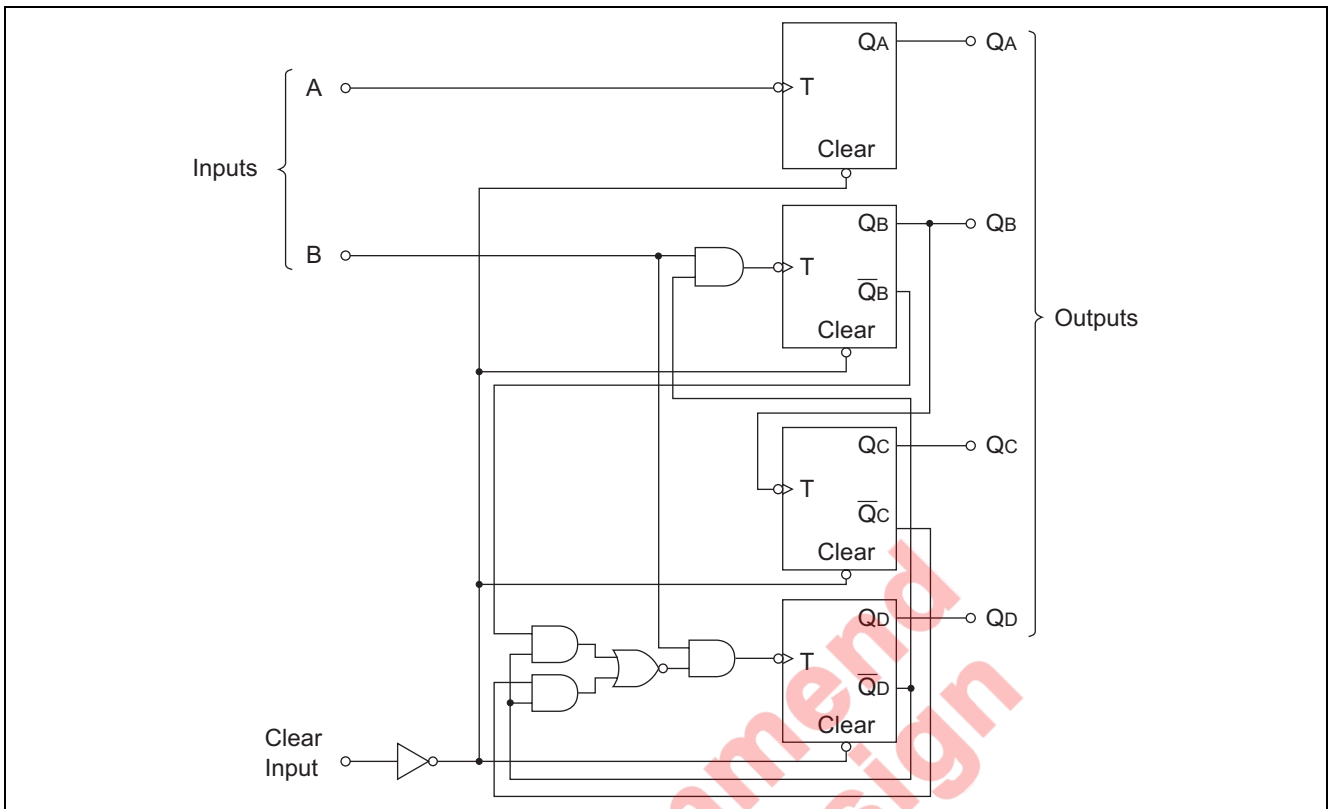
Count	Outputs			
	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>	Q <sub>A</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

### Bi-quinary (Notes 2)

Count	Outputs			
	Q <sub>A</sub>	Q <sub>D</sub>	Q <sub>C</sub>	Q <sub>B</sub>
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

- Notes: 1. Output Q<sub>A</sub> is connected to input B for BCD count.  
 2. Output Q<sub>D</sub> is connected to input A for bi-quinary count.  
 3. H; high level, L; low level, X; irrelevant

Block Diagram (1/2)



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	$V_{CC}$	7	V
Input voltage	Clear	$V_{IN}$	7
	A, B	$V_{IN}$	5.5
Power dissipation	$P_T$	400	mW
Storage temperature	$T_{stg}$	-65 to +150	°C
Operating temperature	$T_{opr}$	-20 to +75	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.75	5.00	5.25	V
Output current	$I_{OH}$	—	—	-400	$\mu A$
	$I_{OL}$	—	—	8	mA
Operating temperature	$T_{opr}$	-20	25	75	°C
Count frequency	A input	0	—	25	MHz
	B input	0	—	20	
Pulse width	A input	20	—	—	ns
	B input	25	—	—	
	Clear	20	—	—	
Clear setup time	$t_{su}$	25↓	—	—	ns

**Electrical Characteristics**

(Ta = -20 to +75 °C)

Item		Symbol	min.	typ.*	max.	Unit	Condition	
Input voltage		V <sub>IH</sub>	2.0	—	—	V		
		V <sub>IL</sub>	—	—	0.7	V		
Output voltage		V <sub>OH</sub>	2.7	—	—	V	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.7 V, I <sub>OH</sub> = -400 μA	
		V <sub>OL</sub>	—	—	0.4	V	I <sub>OL</sub> = 4 mA	V <sub>CC</sub> = 4.75 V, V <sub>IH</sub> = 2 V, V <sub>IL</sub> = 0.7 V
—	—		0.5	I <sub>OL</sub> = 8 mA				
Input current	Clear	I <sub>IH</sub>	—	—	20	μA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 2.7 V	
	Input A		—	—	100			
	Input B		—	—	200			
	Clear	I <sub>IL</sub>	—	—	-0.4	mA	V <sub>CC</sub> = 5.25 V, V <sub>I</sub> = 0.4 V	
	Input A		—	—	-1.6			
	Input B		—	—	-2.4			
	Clear	I <sub>I</sub>	—	—	0.1	mA	V <sub>I</sub> = 7 V	V <sub>CC</sub> = 5.25 V
	Input A		—	—	0.2		V <sub>I</sub> = 5.5 V	
Input B	—		—	0.4				
Short-circuit output current		I <sub>OS</sub>	-20	—	-100	mA	V <sub>CC</sub> = 5.25 V	
Supply current		I <sub>CC</sub>	—	15	26	mA	V <sub>CC</sub> = 5.25 V	
Input clamp voltage		V <sub>IK</sub>	—	—	-1.5	V	V <sub>CC</sub> = 4.75 V, I <sub>IN</sub> = -18 mA	

Notes: \* V<sub>CC</sub> = 5 V, Ta = 25°C

\*\* I<sub>CC</sub> is measured with all outputs open, both Clear inputs grounded following momentary connection to 4.5 V, and all other inputs grounded.

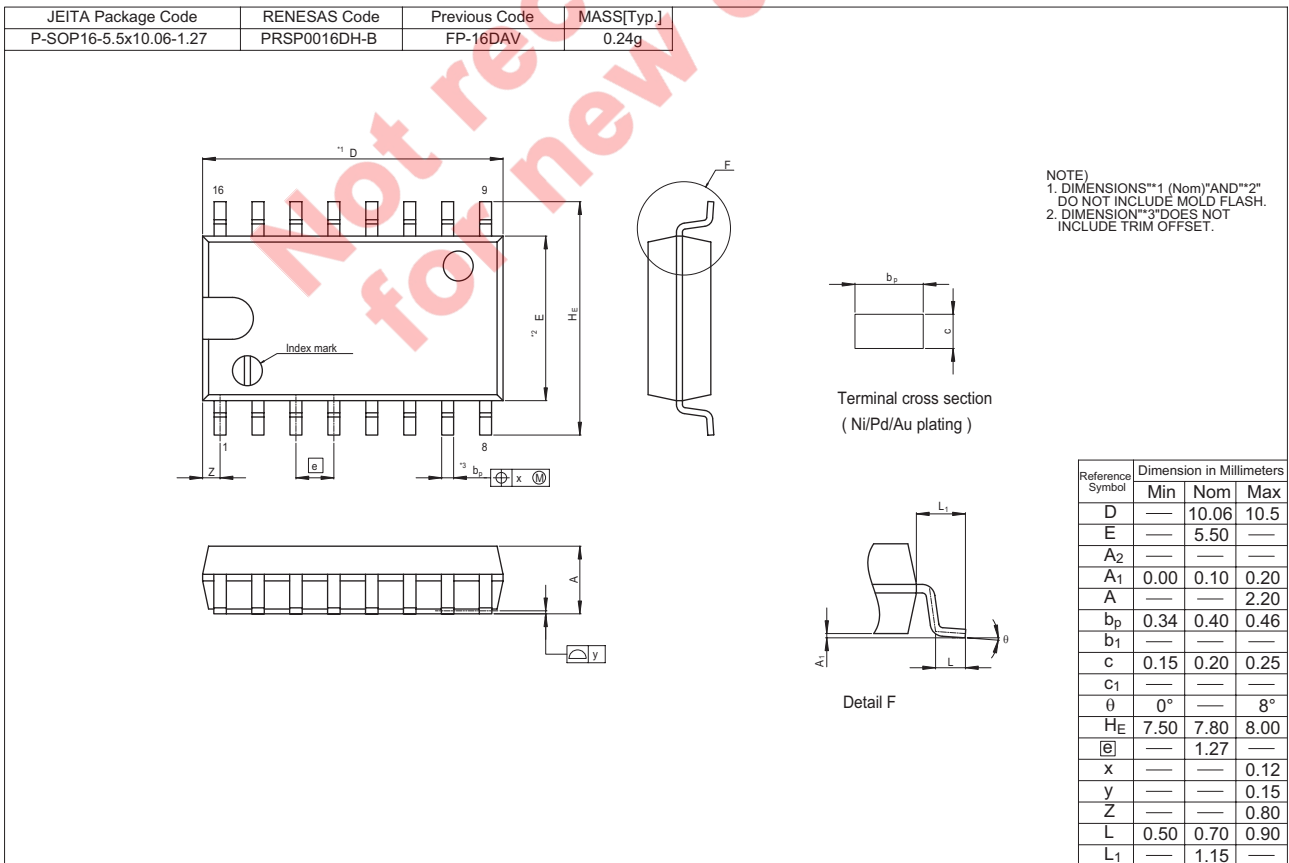
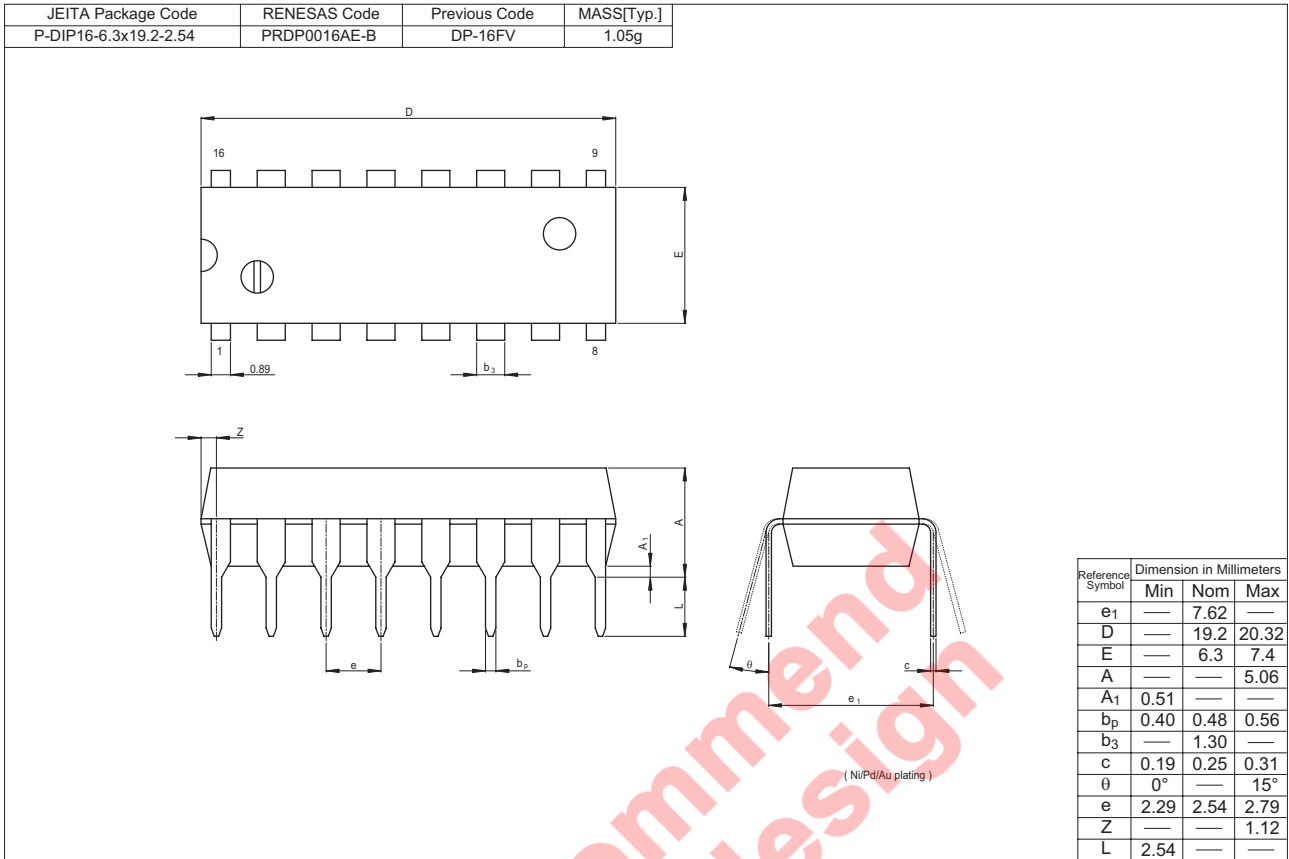
**Switching Characteristics**

(V<sub>CC</sub> = 5 V, Ta = 25°C)

Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
Maximum count frequency	f <sub>max</sub>	A	Q <sub>A</sub>	25	35	—	MHz	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 2 kΩ
		B	Q <sub>B</sub>	20	30	—		
Propagation delay time	t <sub>PLH</sub>	A	Q <sub>A</sub>	—	12	20	ns	
	t <sub>PHL</sub>			—	13	20		
	t <sub>PLH</sub>	A	Q <sub>C</sub>	—	37	60	ns	
	t <sub>PHL</sub>			—	39	60		
	t <sub>PLH</sub>	B	Q <sub>B</sub>	—	13	21	ns	
	t <sub>PHL</sub>			—	14	21		
	t <sub>PLH</sub>	B	Q <sub>C</sub>	—	24	39	ns	
	t <sub>PHL</sub>			—	26	39		
	t <sub>PLH</sub>	B	Q <sub>D</sub>	—	13	21	ns	
	t <sub>PHL</sub>			—	14	21		
t <sub>PHL</sub>	Clear	Any	Any	—	24	39	ns	

Note: Refer to Test Circuit and Waveform of the Common Item "TTL Common Matter (Document No.: REJ27D0005-0100)".

Package Dimensions



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