TEXAS INSTRUMENTS
SN65176B, SN75176B
SLLS101H – JULY 1985 – REVISED DECEMBER 2021

SNx5176B Differential Bus Transceivers

1 Features

- Bidirectional transceivers
- Meet or exceed the requirements of ANSI standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27
- Designed for multipoint transmission on long bus lines in noisy environments
- 3-State driver and receiver outputs
- Individual driver and receiver enables
- Wide positive and negative input/output bus voltage ranges
- ± 60-mA Maximum driver output capability
- Thermal shutdown protection
- Driver positive and negative current limiting
- 12-kΩ Minimum Receiver Input Impedance
- ± 200-mV Receiver input sensitivity
- 50-mV Typical receiver input hysteresis
- Operate from single 5-V supply

2 Applications

- Chemical and gas sensors
- Digital signage
- HMI (human machine interfaces)
- Motor controls: AC induction, brushed and brush-less dc, low- and high-voltage, stepper motors, and permanent magnets
- TETRA Base stations
- Telecom towers: remote electrical tilt units (ret) and tower mounted amplifiers (TMA)
- Weigh scales
- Wireless repeaters

3 Description

The SN65176B and SN75176B differential bus transceivers are designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

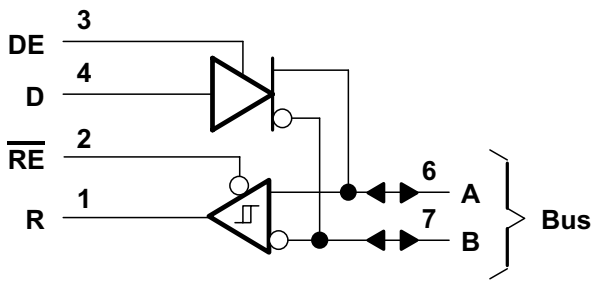
The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

Device Information

PART NUMBER	PACKAGE (PIN)(1)	BODY SIZE (NOM)
SNx5176	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm
	SOP (8)	6.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.



Simplified Schematic

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4 Revision History

Changes from Revision G (July 2021) to Revision H (December 2021) **Page**

- Changed ψ_{JT} From 78.8 to 8.8 for the D package in the *Thermal Information* table....4

Changes from Revision F (January 2015) to Revision G (July 2021) **Page**

- Changed the *Thermal Information* table....4
- Changed the V_O Output voltage MAX value from: 6 V to: V_{CC} in the *Electrical Characteristics – Driver*....5
- Changed the V_{ODI} Differential output voltage MAX value from: 6 V to: V_{CC} in the *Electrical Characteristics – Driver*....5

Changes from Revision E (January 2014) to Revision F (January 2015) **Page**

- Added *Applications*, *Device Information* table, *Pin Functions* table, *ESD Ratings* table, *Thermal Information* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section....1
- Moved *Typical Characteristics* inside of the *Specifications* section....7

Changes from Revision D (April 2003) to Revision E (January 2014) **Page**

- Updated document to new TI data sheet format - no specification changes....1
- Deleted *Ordering Information* table....1

5 Pin Configuration and Functions

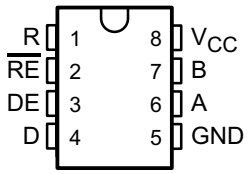


Figure 5-1. Top View

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
R	1	O	Logic Data Output from RS-485 Receiver
$\overline{RE}$	2	I	Receive Enable (active low)
DE	3	I	Driver Enable (active high)
D	4	I	Logic Data Input to RS-485 Driver
GND	5	—	Device Ground Pin
A	6	I/O	RS-422 or RS-485 Data Line
B	7	I/O	RS-422 or RS-485 Data Line
V_{CC}	8	—	Power Input. Connect to 5-V Power Source.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		7	V
	Voltage range at any bus terminal	–10	15	V
V_I	Enable input voltage		5.5	V
T_J	Operating virtual junction temperature		150	°C
T_{stg}	Storage temperature range	–65	150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		260	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Section 6.2* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential input/output bus voltage, are with respect to network ground terminal.

6.2 Recommended Operating Conditions

			MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		-7		12	V
V_{IH}	High-level input voltage	D, DE, and $\overline{RE}$	2			V
V_{IL}	Low-level input voltage	D, DE, and $\overline{RE}$			0.8	V
V_{ID}	Differential input voltage(1)				±12	V
I_{OH}	High-level output current	Driver			–60	mA
		Receiver			–400	µA
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
T_A	Operating free-air temperature	SN65176B	–40		105	°C
		SN75176B	0		70	

(1) Differential input/output bus voltage is measured at the non-inverting terminal A, with respect to the inverting terminal B.

6.3 Thermal Information

THERMAL METRIC(1)		SNx5176			UNIT
		D (SOIC)	PS (SO)	P (PDIP)	
		8 PINS			
$R_{\theta JA}$	Junction-to-ambient thermal resistance	114.4	113.2	88.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	55.1	57.9	65.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	61.6	69.0	69.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	14.6	35.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	60.8	68.1	64.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.4 Electrical Characteristics – Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP(2)	MAX	UNIT
V_{IK}	Input clamp voltage	I_I = –18 mA				–1.5	V
V_O	Output voltage	I_O = 0		0		Vcc	V
$\|V_{OD1}\|$	Differential output voltage	I_O = 0		1.5	3.6	Vcc	V
$\|V_{OD2}\|$	Differential output voltage	R_L = 100 Ω, see Figure 7-1		½ V_{OD1} or 2 (4)			V
		R_L = 54 Ω, see Figure 7-1		1.5	2.5	5	
V_{OD3}	Differential output voltage	See (5)		1.5		5	V
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage(3)	R_L = 54 Ω or 100 Ω, see Figure 7-1				±0.2	V
V_{OC}	Common-mode output voltage	R_L = 54 Ω or 100 Ω, see Figure 7-1		-1		+3	V
$\Delta\|V_{OC}\|$	Change in magnitude of common-mode output voltage(3)	R_L = 54 Ω or 100 Ω, see Figure 7-1				±0.2	V
I_O	Output current	Output disabled(6)	V_O = 12 V			1	mA
			V_O = –7 V			–0.8	
I_{IH}	High-level input current	V_I = 2.4 V				20	µA
I_{IL}	Low-level input current	V_I = 0.4 V				–400	µA
I_{OS}	Short-circuit output current	V_O = –7 V				–250	mA
		V_O = 0				–150	
		V_O = V_{CC}				250	
		V_O = 12 V				250	
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	70	mA
			Outputs disabled		26	35	

(1) The power-off measurement in ANSI Standard TIA/EIA-422-B applies to disabled outputs only and is not applied to combined inputs and outputs.
(2) All typical values are at V_{CC} = 5 V and T_A = 25°C.
(3) $\Delta|V_{OD}|$ and $\Delta|V_{OC}|$ are the changes in magnitude of V_{OD} and V_{OC}, respectively, that occur when the input is changed from a high level to a low level.
(4) The minimum V_{OD2} with a 100-Ω load is either ½ V_{OD1} or 2 V, whichever is greater.
(5) See ANSI Standard TIA/EIA-485-A, Figure 3.5, Test Termination Measurement 2.
(6) This applies for both power on and off; refer to ANSI Standard TIA/EIA-485-A for exact conditions. The TIA/EIA-422-B limit does not apply for a combined driver and receiver terminal.

6.5 Electrical Characteristics – Receiver

over recommended ranges of common-mode input voltage, supply voltage, and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	V_O = 2.7 V, I_O = –0.4 mA				0.2	V
$V_{IT–}$	Negative-going input threshold voltage	V_O = 0.5 V, I_O = 8 mA		–0.2(2)			V
V_{hys}	Input hysteresis voltage ($V_{IT+} – V_{IT–}$)				50		mV
V_{IK}	Enable Input clamp voltage	I_I = –18 mA				–1.5	V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –400 µA, see Figure 7-2		2.7			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, see Figure 7-2				0.45	V
I_{OZ}	High-impedance-state output current	V_O = 0.4 V to 2.4 V				±20	µA
I_I	Line input current	Other input = 0 V(3)	V_I = 12 V			1	mA
			V_I = –7 V			–0.8	
I_{IH}	High-level enable input current	V_{IH} = 2.7 V				20	µA
I_{IL}	Low-level enable input current	V_{IL} = 0.4 V				–100	µA
r_I	Input resistance	V_I = 12 V		12			kΩ
I_{OS}	Short-circuit output current			–15		–85	mA
I_{CC}	Supply current (total package)	No load	Outputs enabled		42	55	mA
			Outputs disabled		26	35	

(1) All typical values are at V_{CC} = 5 V, T_A = 25°C.
(2) The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for common-mode input voltage and threshold voltage levels only.
(3) This applies for both power on and power off. Refer to EIA Standard TIA/EIA-485-A for exact conditions.

6.6 Switching Characteristics – Driver

V_{CC} = 5 V, R_L = 110 Ω, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(OD)}$	Differential-output delay time	R_L = 54 Ω, see Figure 7-3		15	22	ns
$t_{t(OD)}$	Differential-output transition time	R_L = 54 Ω, see Figure 7-3		20	30	ns
t_{PZH}	Output enable time to high level	See Figure 7-4		85	120	ns
t_{PZL}	Output enable time to low level	See Figure 7-5		40	60	ns
t_{PHZ}	Output disable time from high level	See Figure 7-4		150	250	ns
t_{PLZ}	Output disable time from low level	See Figure 7-5		20	30	ns

6.7 Switching Characteristics – Receiver

V_{CC} = 5 V, C_L = 15 pF, T_A = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low- to high-level output	V_{ID} = 0 to 3 V, see Figure 7-6		21	35	ns
t_{PHL}	Propagation delay time, high- to low-level output			23	35	
t_{PZH}	Output enable time to high level	See Figure 7-7		10	20	ns
t_{PZL}	Output enable time to low level			12	20	
t_{PHZ}	Output disable time from high level	See Figure 7-7		20	35	ns
t_{PLZ}	Output disable time from low level			17	25	

6.8 Typical Characteristics

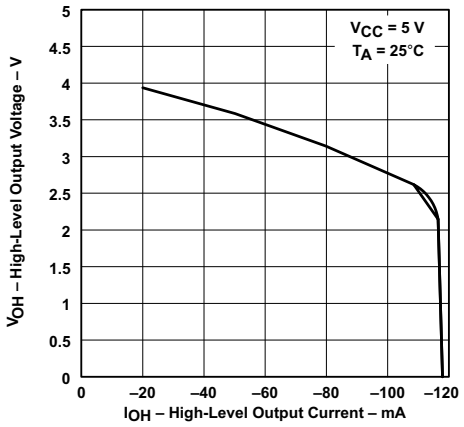


Figure 6-1. Driver High-Level Output Voltage vs High-Level Output Current

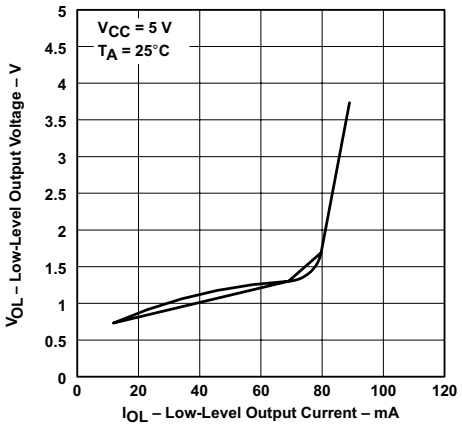


Figure 6-2. Driver Low-Level Output Voltage vs Low-Level Output Current

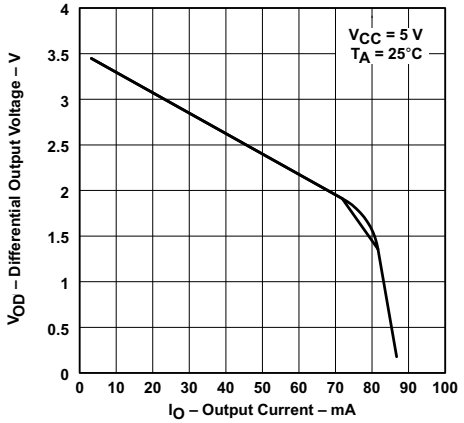


Figure 6-3. Driver Differential Output Voltage vs Output Current

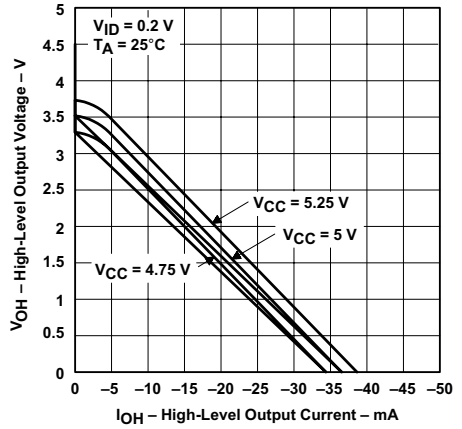
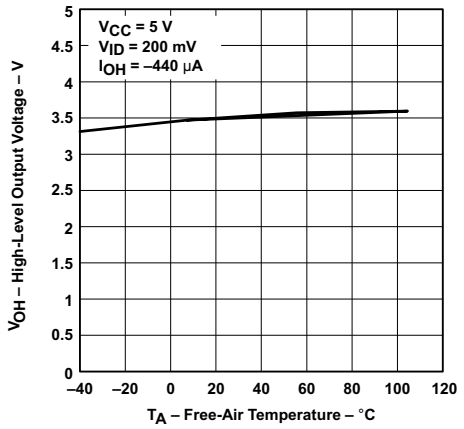


Figure 6-4. Receiver High-Level Output Voltage vs High-Level Output Current



Only the 0°C to 70°C portion of the curve applies to the SN75176B device.

Figure 6-5. Receiver High-Level Output Voltage vs Free-Air Temperature

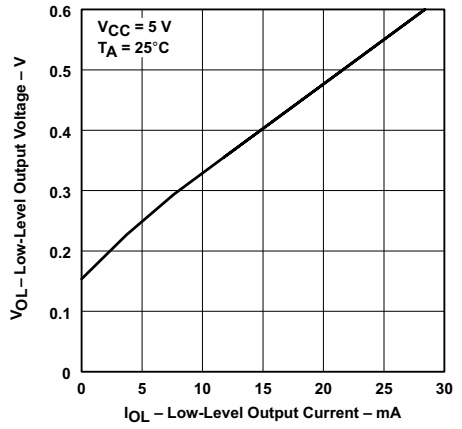


Figure 6-6. Receiver Low-Level Output Voltage vs Low-Level Output Current

6.8 Typical Characteristics (continued)

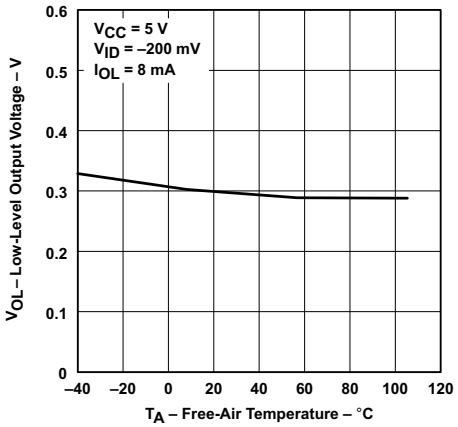


Figure 6-7. Receiver Low-Level Output Voltage vs Free-Air Temperature

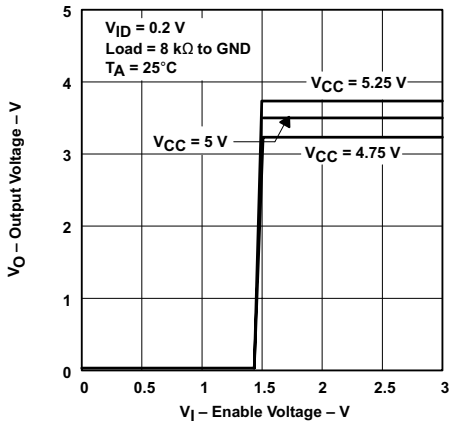


Figure 6-8. Receiver Output Voltage vs Enable Voltage

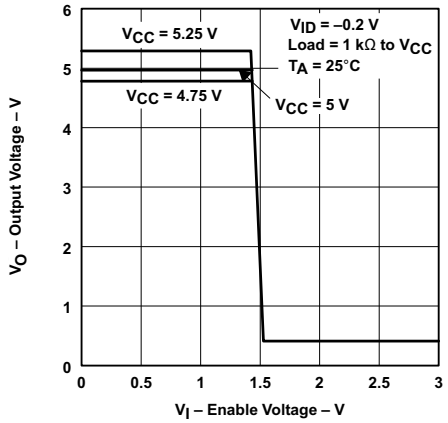


Figure 6-9. Receiver Output Voltage vs Enable Voltage

Parameter Measurement Information

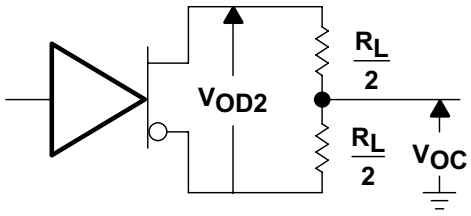


Figure 7-1. Driver V_{OD} and V_{OC}

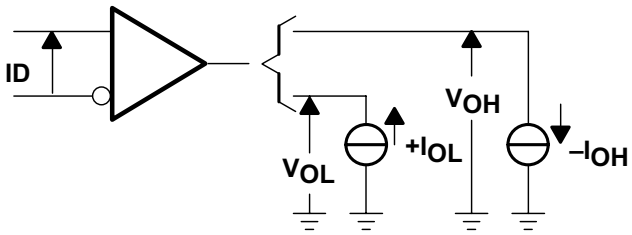
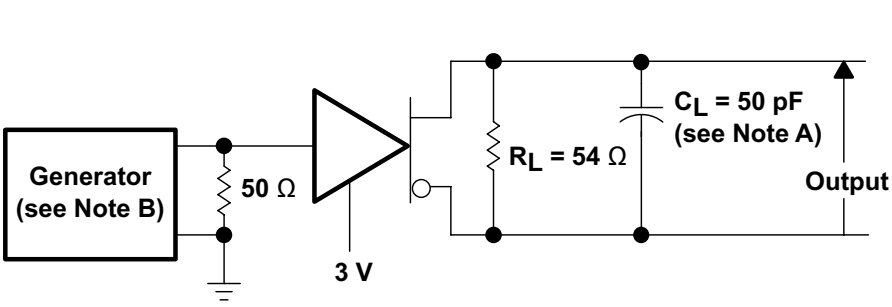
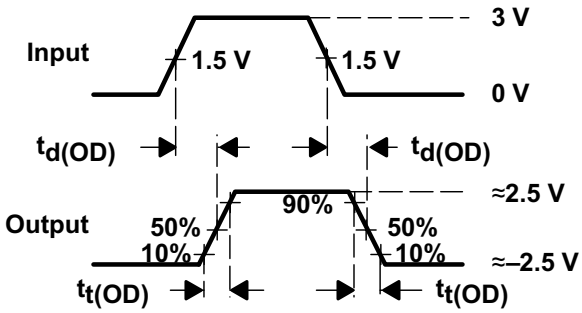


Figure 7-2. Receiver V_{OH} and V_{OL}



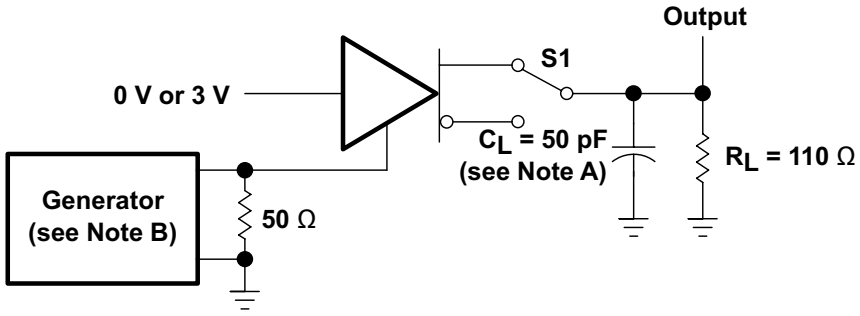
TEST CIRCUIT



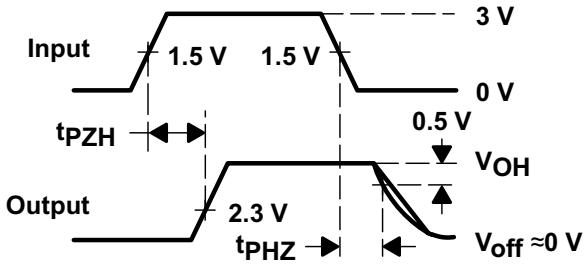
VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7-3. Driver Test Circuit and Voltage Waveforms



TEST CIRCUIT



VOLTAGE WAVEFORMS

A. C_L includes probe and jig capacitance.
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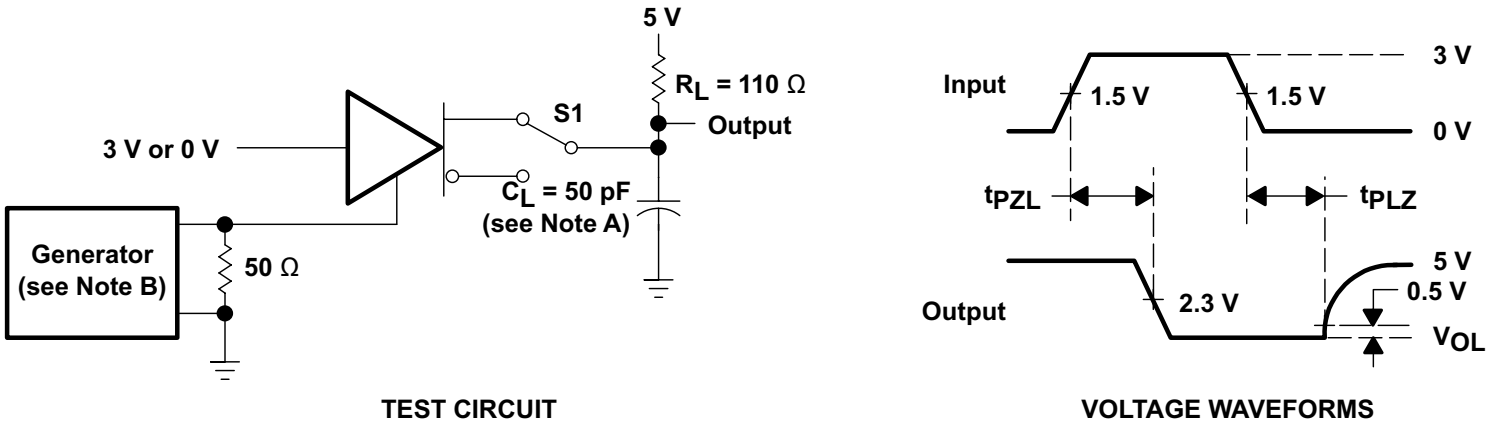

TEST CIRCUIT **VOLTAGE WAVEFORMS**

A. C_L includes probe and jig capacitance.
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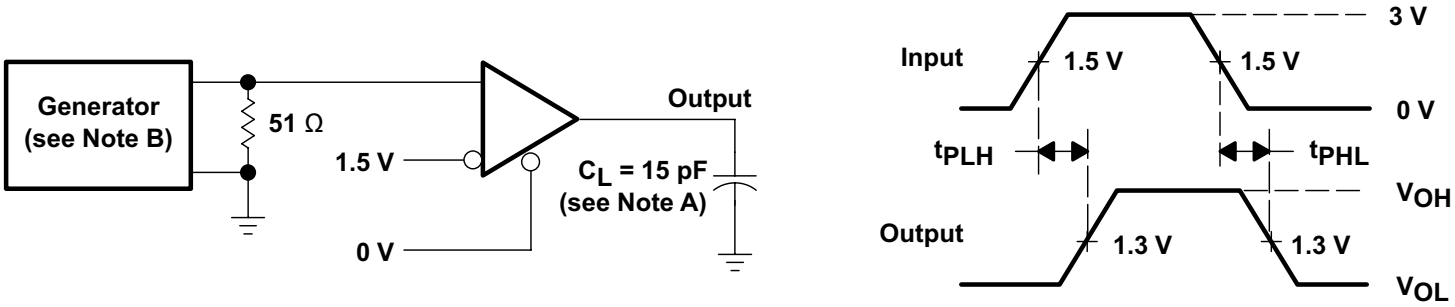
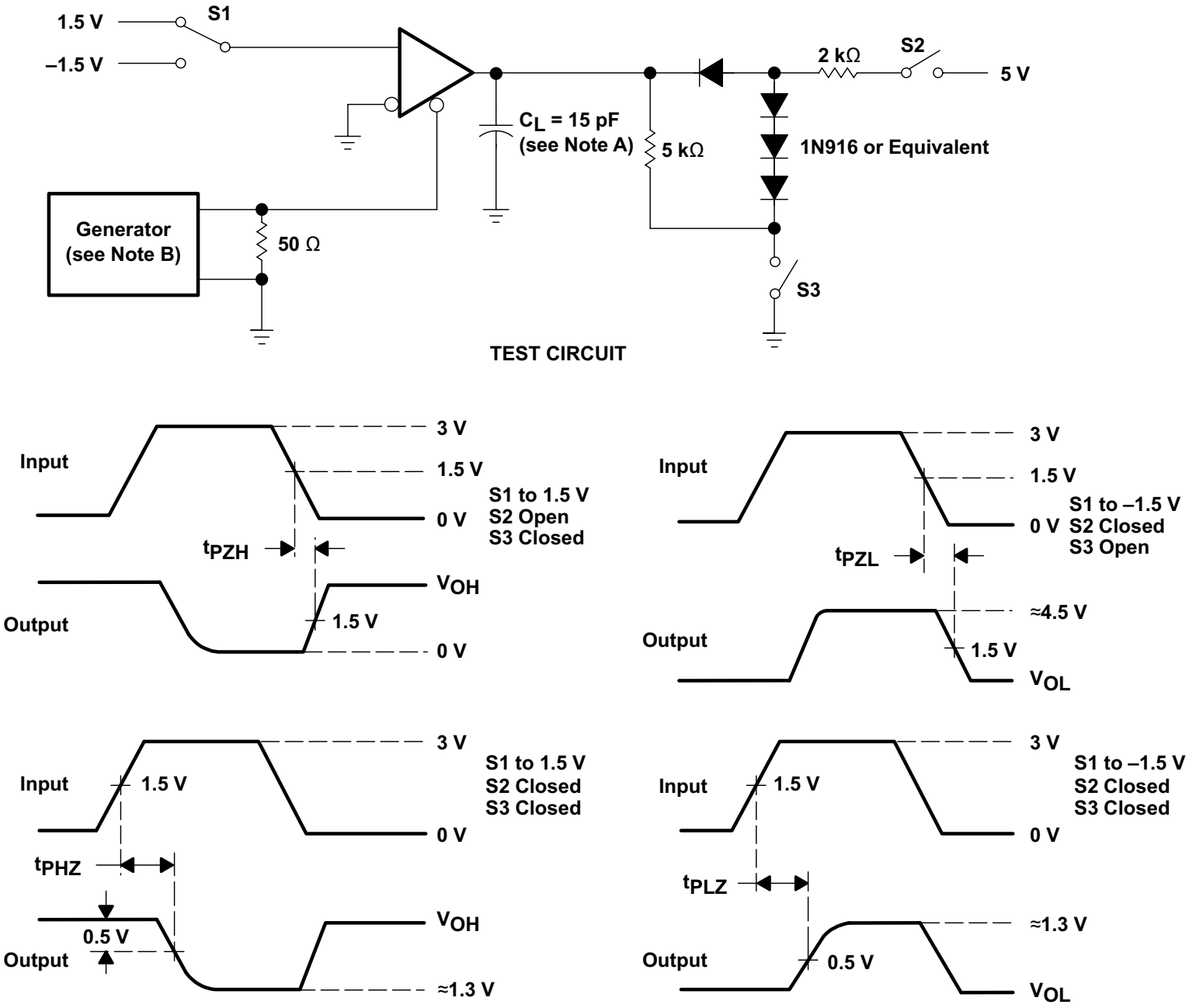


TEST CIRCUIT **VOLTAGE WAVEFORMS**

A. C_L includes probe and jig capacitance.
B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7-6. Receiver Test Circuit and Voltage Waveforms



A. C_L includes probe and jig capacitance.

B. The input pulse is supplied by a generator having the following characteristics: PRR ≤1 MHz, 50% duty cycle, t_r ≤ 6 ns, t_f ≤ 6 ns, Z_O = 50 Ω.

Figure 7-7. Receiver Test Circuit and Voltage Waveforms

7 Detailed Description

7.1 Overview

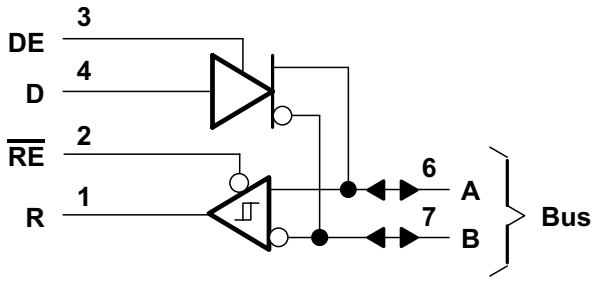
The SN65176B and SN75176B differential bus transceivers are integrated circuits designed for bidirectional data communication on multipoint bus transmission lines. They are designed for balanced transmission lines and meet ANSI Standards TIA/EIA-422-B and TIA/EIA-485-A and ITU Recommendations V.11 and X.27.

The SN65176B and SN75176B devices combine a 3-state differential line driver and a differential input line receiver, both of which operate from a single 5-V power supply. The driver and receiver have active-high and active-low enables, respectively, that can be connected together externally to function as a direction control. The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0. These ports feature wide positive and negative common-mode voltage ranges, making the device suitable for party-line applications.

The driver is designed for up to 60 mA of sink or source current. The driver features positive and negative current limiting and thermal shutdown for protection from line-fault conditions. Thermal shutdown is designed to occur at a junction temperature of approximately 150°C. The receiver features a minimum input impedance of 12 kΩ, an input sensitivity of ±200 mV, and a typical input hysteresis of 50 mV.

The SN65176B and SN75176B devices can be used in transmission-line applications employing the SN75172 and SN75174 quadruple differential line drivers and SN75173 and SN75175 quadruple differential line receivers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Driver

The driver converts a TTL logic signal level to RS-422 and RS-485 compliant differential output. The TTL logic input, DE pin, can be used to turn the driver on and off.

Table 7-1. Driver Function Table(1)

INPUT D	ENABLE DE	DIFFERENTIAL OUTPUTS	
		A	B
H	H	H	L
L	H	L	H
X	L	Z	Z

(1) H = high level,
L = low level,
X = irrelevant,
Z = high impedance (off)

7.3.2 Receiver

The receiver converts a RS-422 or RS-485 differential input voltage to a TTL logic level output. The TTL logic input, $\overline{RE}$ pin, can be used to turn the receiver logic output on and off.

Table 7-2. Receiver Function Table(1)

DIFFERENTIAL INPUTS A–B	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq 0.2$ V	L	H
–0.2 V < V_{ID} < 0.2 V	L	U
$V_{ID} \leq$ –0.2 V	L	L
X	H	Z
Open	L	U

(1) H = high level,
L = low level,
U = unknown,
Z = high impedance (off)

7.4 Device Functional Modes

7.4.1 Device Powered

Both the driver and receiver can be individually enabled or disabled in any combination. DE and $\overline{RE}$ can be connected together for a single port direction control bit.

7.4.2 Device Unpowered

The driver differential outputs and the receiver differential inputs are connected internally to form differential input/output (I/O) bus ports that are designed to offer minimum loading to the bus when the driver is disabled or V_{CC} = 0.

7.4.3 Symbol Cross Reference

Table 7-3. Symbol Equivalents

DATA SHEET PARAMETER	TIA/EIA-422-B	TIA/EIA-485-A
V_O	V_{oa}, V_{ob}	V_{oa}, V_{ob}
$\lvert V_{OD1}\rvert$	V_o	V_o
$\lvert V_{OD2}\rvert$	V_t ®$_L$ = 100 Ω)	V_t ®$_L$ = 54 Ω)
$\lvert V_{OD3}\rvert$		V_t (test termination measurement 2)
$\Delta\lvert V_{OD}\rvert$	$\lvert \lvert V_t\rvert - \lvert \overline{V}_t\rvert \rvert$	$\lvert \lvert V_t - \lvert \overline{V}_t\rvert \rvert$
V_{OC}	$\lvert V_{os}\rvert$	$\lvert V_{os}\rvert$
$\Delta\lvert V_{OC}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$	$\lvert V_{os} - \overline{V}_{os}\rvert$
I_{OS}	$\lvert I_{sa}\rvert$, $\lvert I_{sb}\rvert$	
I_O	$\lvert I_{xa}\rvert$, $\lvert I_{xb}\rvert$	I_{ia}, I_{ib}

8 Application and Implementation

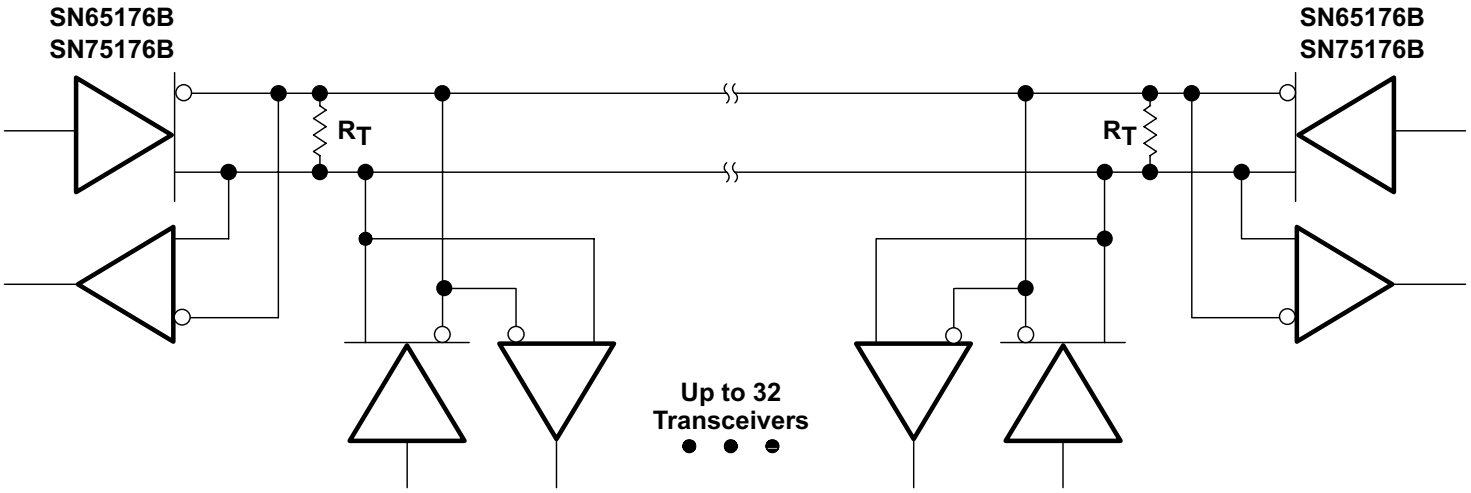
Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device can be used in RS-485 and RS-422 physical layer communications.

8.2 Typical Application



The line should be terminated at both ends in its characteristic impedance ($R_T = Z_O$). Stub lengths off the main line should be kept as short as possible.

Figure 8-1. Typical RS-485 Application Circuit

8.2.1 Design Requirements

- 5-V power source
- RS-485 bus operating at 10 Mbps or less
- Connector that ensures the correct polarity for port pins
- External fail safe implementation

8.2.2 Detailed Design Procedure

- Place the device close to bus connector to keep traces (stub) short to prevent adding reflections to the bus line
- If desired, add external fail-safe biasing to ensure +200 mV on the A-B port.

8.2.3 Application Curves

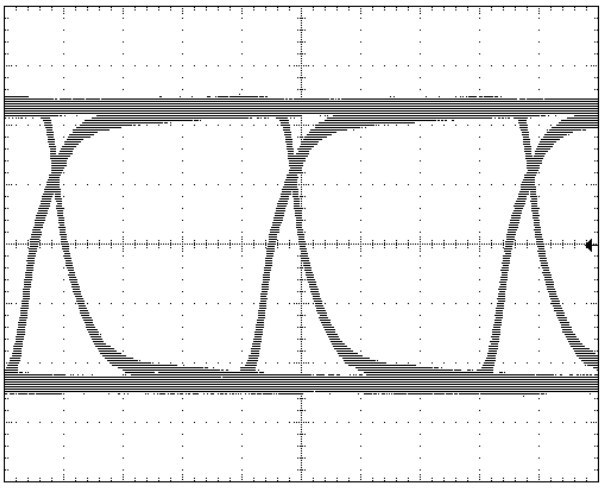


Figure 8-2. Eye Diagram for 10-Mbits/s over 100 feet of standard CAT-5E cable 120-Ω Termination at both ends. Scale is 1 V per division and 25 nS per division

8.3 System Examples

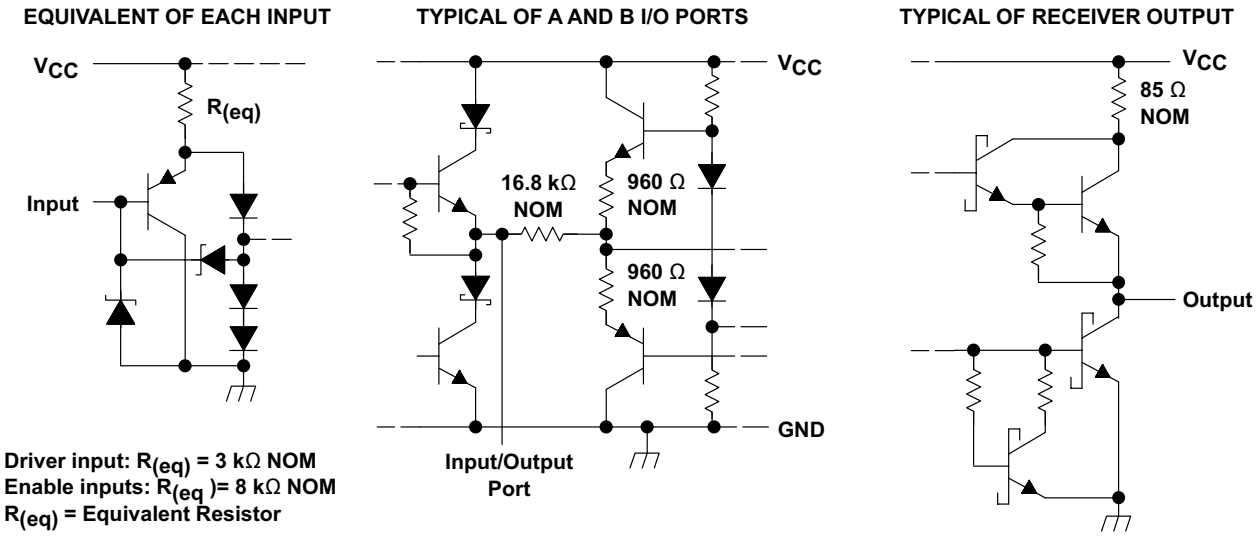


Figure 8-3. Schematics of Inputs and Outputs

9 Power Supply Recommendations

Power supply should be 5 V with a tolerance less than 10%

10 Layout

10.1 Layout Guidelines

Traces from device pins A and B to connector must be short and capable of 250 mA maximum current.

10.2 Layout Example

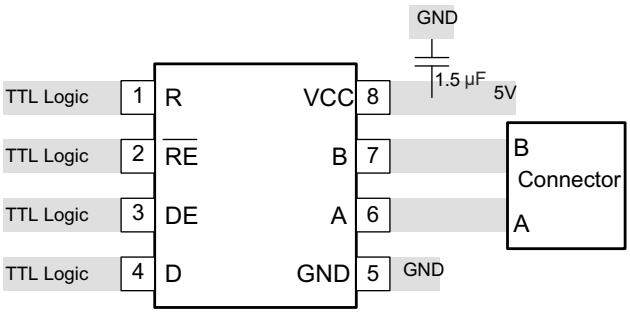


Figure 10-1. Layout Diagram

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65176B	Click here	Click here	Click here	Click here	Click here
SN75176B	Click here	Click here	Click here	Click here	Click here

11.2 Trademarks

All trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65176BD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	
SN65176BDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	
SN65176BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	Samples
SN65176BDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	Samples
SN65176BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	65176B	Samples
SN65176BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	-40 to 105	SN65176BP	Samples
SN75176BD	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	
SN75176BDE4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	
SN75176BDG4	NRND	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	
SN75176BDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	Samples
SN75176BDRE4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	Samples
SN75176BDRG4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	75176B	Samples
SN75176BP	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75176BP	Samples
SN75176BPE4	ACTIVE	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type	0 to 70	SN75176BP	Samples
SN75176BPSR	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B	Samples
SN75176BPSRG4	ACTIVE	SO	PS	8	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	A176B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

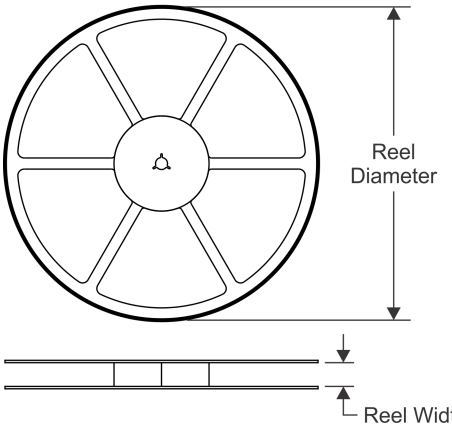
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

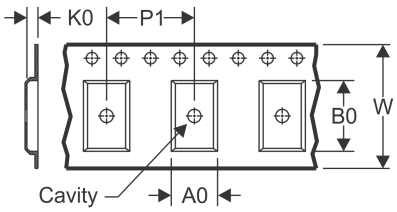
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

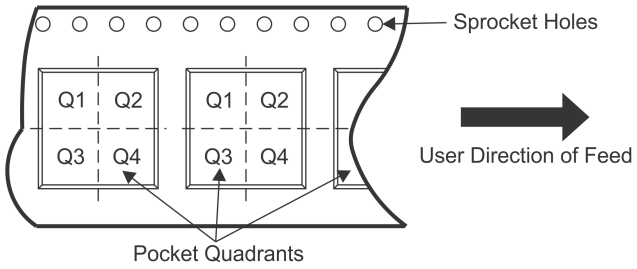


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

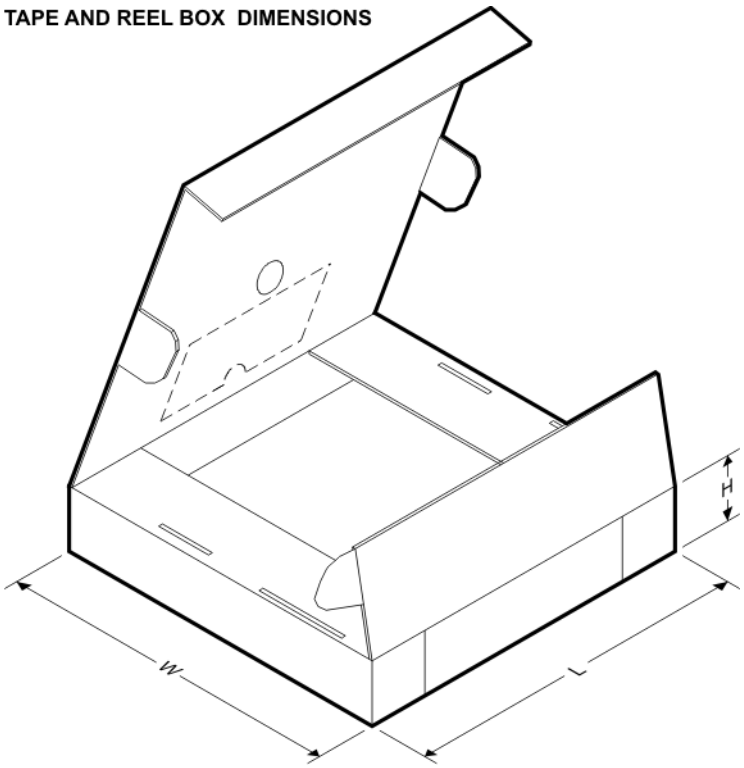
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN75176BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN75176BPSR	SO	PS	8	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1

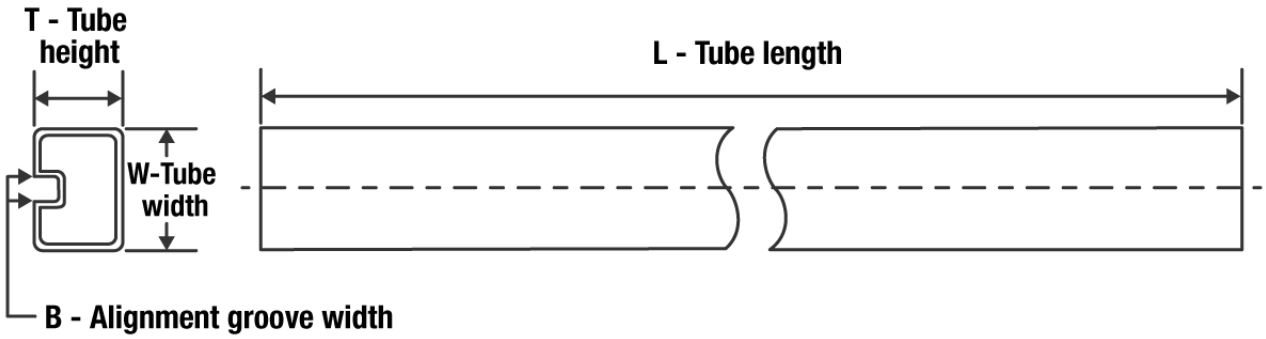
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

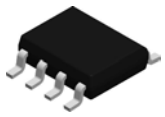
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65176BDR	SOIC	D	8	2500	367.0	367.0	35.0
SN65176BDR	SOIC	D	8	2500	340.5	336.1	25.0
SN65176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN65176BDRG4	SOIC	D	8	2500	367.0	367.0	35.0
SN65176BDRG4	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BDR	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BDR	SOIC	D	8	2500	367.0	367.0	35.0
SN75176BDR	SOIC	D	8	2500	340.5	338.1	20.6
SN75176BDRG4	SOIC	D	8	2500	367.0	367.0	35.0
SN75176BDRG4	SOIC	D	8	2500	340.5	336.1	25.0
SN75176BPSR	SO	PS	8	2000	853.0	449.0	35.0
SN75176BPSR	SO	PS	8	2000	367.0	367.0	38.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65176BD	D	SOIC	8	75	507	8	3940	4.32
SN65176BDG4	D	SOIC	8	75	507	8	3940	4.32
SN65176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BD	D	SOIC	8	75	507	8	3940	4.32
SN75176BDE4	D	SOIC	8	75	507	8	3940	4.32
SN75176BDG4	D	SOIC	8	75	507	8	3940	4.32
SN75176BP	P	PDIP	8	50	506	13.97	11230	4.32
SN75176BPE4	P	PDIP	8	50	506	13.97	11230	4.32

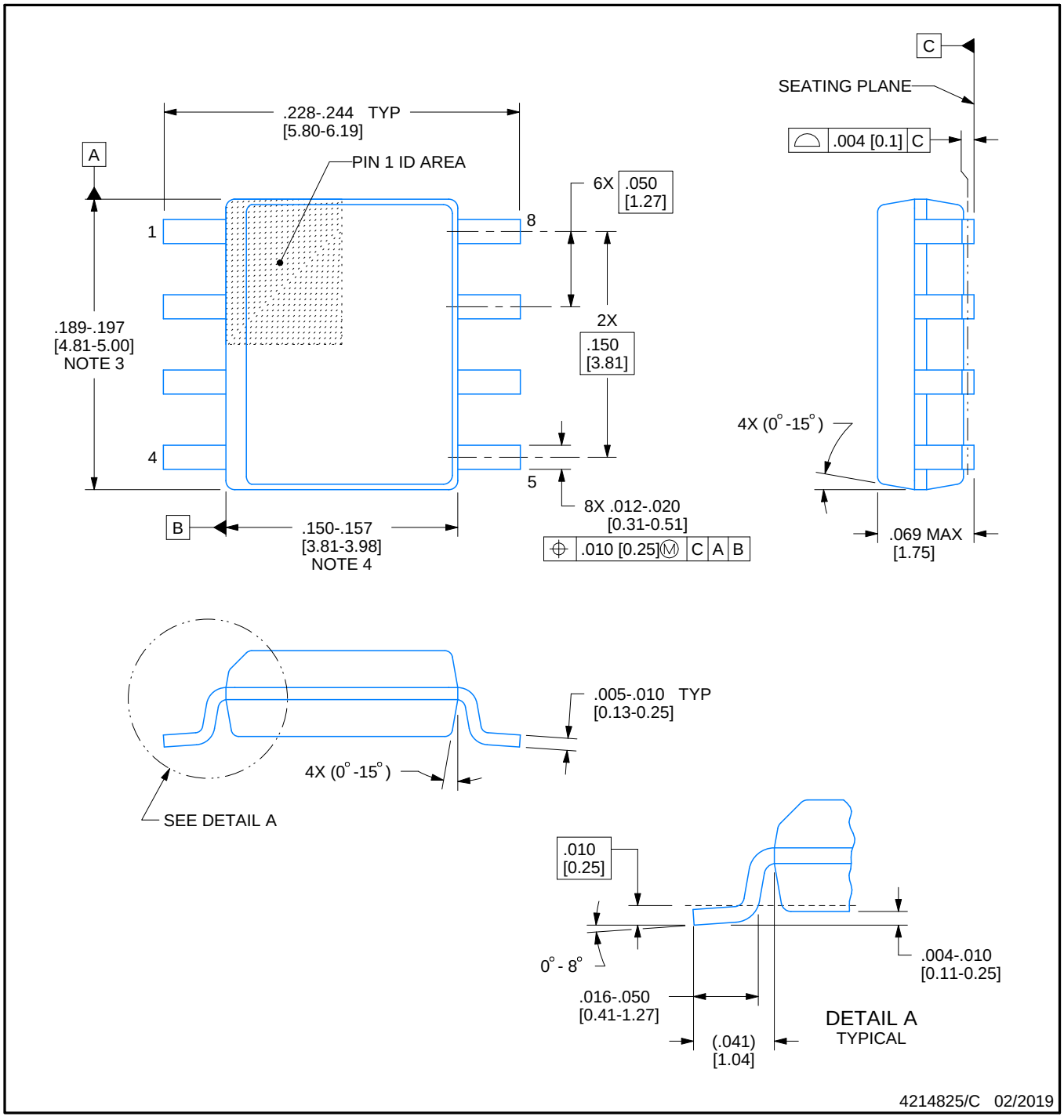


PACKAGE OUTLINE

D0008A

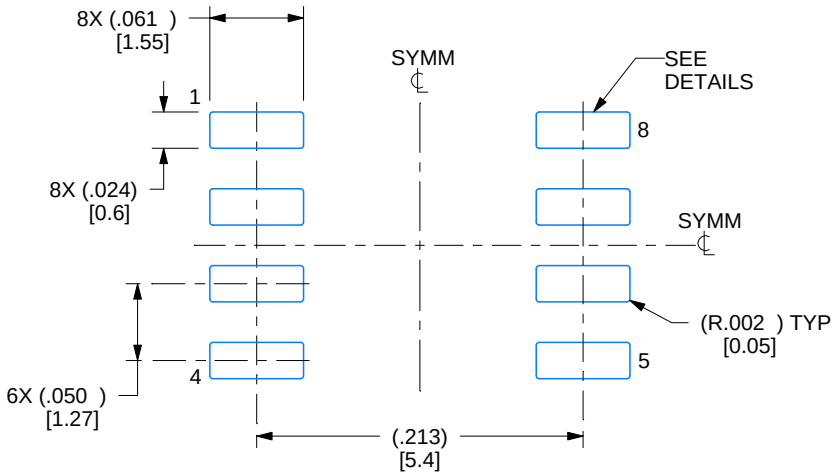
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

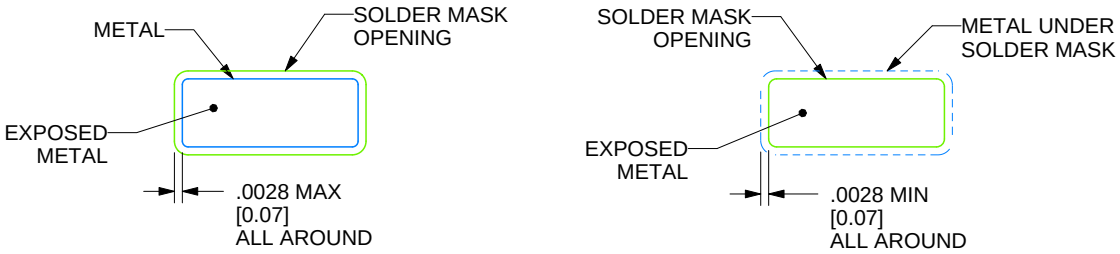


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

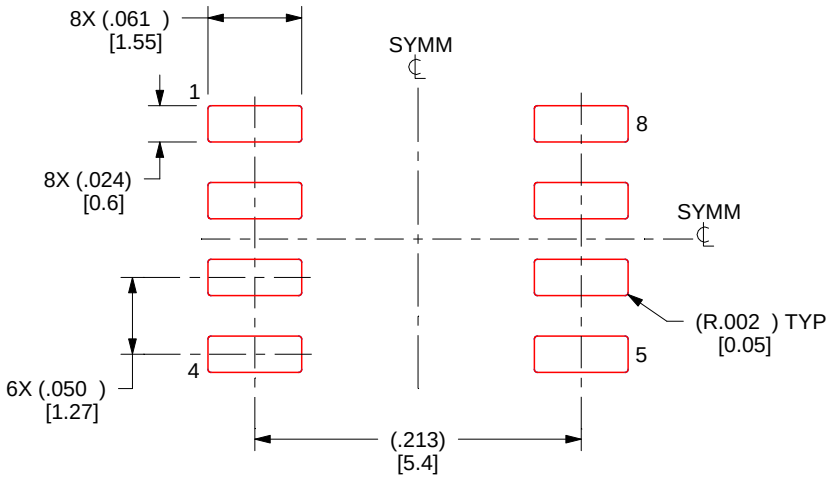
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

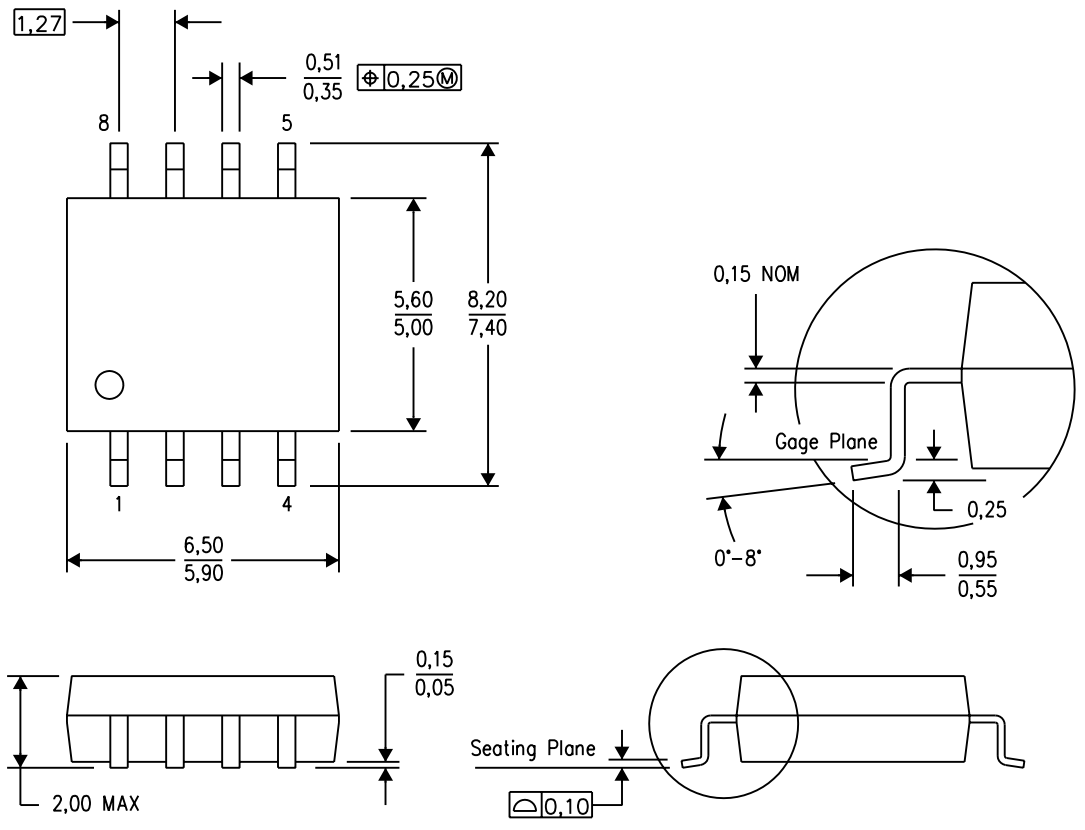
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

MECHANICAL DATA

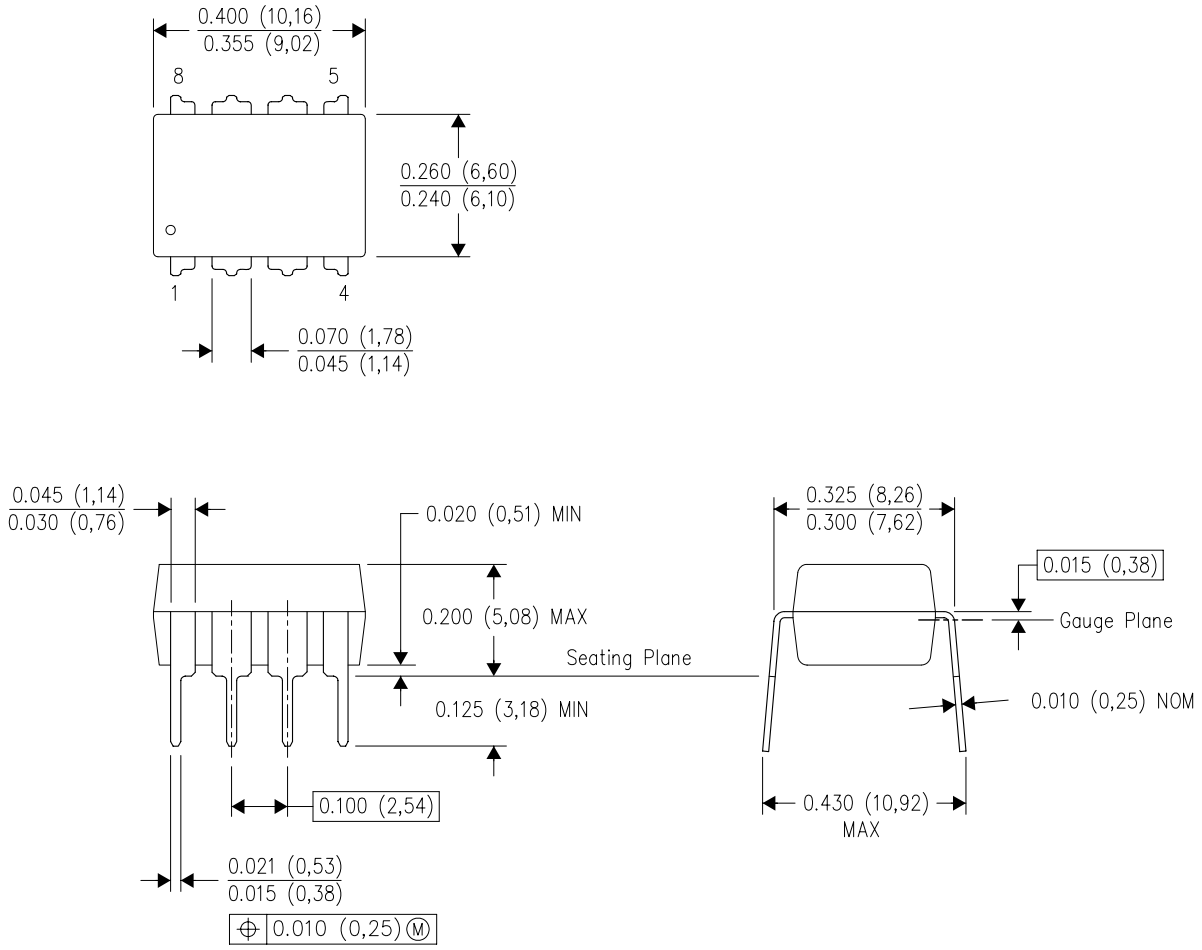
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



4040063/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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