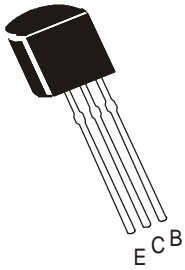


## SILICON PLANAR EPITAXIAL TRANSISTORS

**BC635, 637, 639 NPN**  
**BC636, 638, 640 PNP**

**TO-92**  
**Plastic Package**

For Lead Free Parts, Device Part #  
 will be Prefixed with "T"



High Current Transistor

### ABSOLUTE MAXIMUM RATINGS (T<sub>a</sub>=25°C)

DESCRIPTION	SYMBOL	BC635	BC637	BC639	UNIT
		BC636	BC638	BC640	
Collector Emitter Voltage	V <sub>CEO</sub>	45	60	80	V
Collector Base Voltage	V <sub>CBO</sub>	45	60	80	V
Emitter Base Voltage	V <sub>EBO</sub>	5.0			V
Collector Current Continuous	I <sub>C</sub>	1.0			A
Total Device Dissipation at T <sub>a</sub> =25°C	P <sub>D</sub>	800			mW
Derate Above 25°C		6.4			mW/°C
Total Device Dissipation at T <sub>a</sub> =25°C	**P <sub>D</sub>	1.0			W
Total Device Dissipation at T <sub>c</sub> =25°C	P <sub>D</sub>	2.75			W
Derate Above 25°C		22			mW/°C
Operating And Storage Junction Temperature Range	T <sub>j</sub> , T <sub>stg</sub>	- 55 to +150			°C

### THERMAL RESISTANCE

Junction to Case	R <sub>th(j-c)</sub>	45	°C/W
Junction to Ambient in free air	R <sub>th(j-a)</sub>	156	°C/W
Junction to Ambient	**R <sub>th(j-a)</sub>	125	°C/W

### ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=25°C unless specified otherwise)

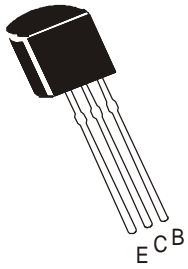
DESCRIPTION	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Collector Emitter Voltage	V <sub>CEO</sub>	I <sub>C</sub> =1mA, I <sub>B</sub> =0			
		<b>BC635/BC636</b>	45		V
		<b>BC637/BC638</b>	60		V
		<b>BC639/BC640</b>	80		V
Collector Base Voltage	V <sub>CBO</sub>	I <sub>C</sub> =100μA, I <sub>E</sub> =0			
		<b>BC635/BC636</b>	45		V
		<b>BC637/BC638</b>	60		V
		<b>BC639/BC640</b>	80		V
Emitter Base Voltage	V <sub>EBO</sub>	I <sub>E</sub> =10μA, I <sub>C</sub> =0	5.0		V
Collector Cut Off Current	I <sub>CBO</sub>	V <sub>CB</sub> =30V, I <sub>E</sub> =0		0.1	μA
		V <sub>CB</sub> =30V, I <sub>E</sub> =0, T <sub>a</sub> =125°C		10	μA
Base Emitter (On) Voltage	*V <sub>BE(on)</sub>	I <sub>C</sub> =500mA, V <sub>CE</sub> =2V		1.0	V
Collector Emitter Saturation Voltage	*V <sub>CE(sat)</sub>	I <sub>C</sub> =500mA, I <sub>B</sub> =50mA		0.5	V

\*Pulse Test: Pulse Width ≤ 300ms, Duty Cycle 2%

\*\*Transistors mounted on printed circuit board, max Lead Length 4mm, mounting pad for collector lead min 10mm x 10 mm

BC635\_BC640Rev\_5 180712E

# SILICON PLANAR EPITAXIAL TRANSISTORS



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## ELECTRICAL CHARACTERISTICS (T<sub>a</sub>=25°C unless specified otherwise)

DESCRIPTION	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
DC Current Gain	*h <sub>FE</sub>	V <sub>CE</sub> =2V, I <sub>C</sub> =5mA	25		
		V <sub>CE</sub> =2V, I <sub>C</sub> =150mA			
		<b>BC635/BC636</b>	40	250	
		<b>BC637/BC638</b>	40	<b>250</b>	
		<b>BC639/BC640</b>	40	<b>250</b>	
		<b>Group-10</b>	40	160	
		<b>Group-16</b>	100	250	
		V <sub>CE</sub> =2V, I <sub>C</sub> =500mA	25		

## DYNAMIC CHARACTERISTICS

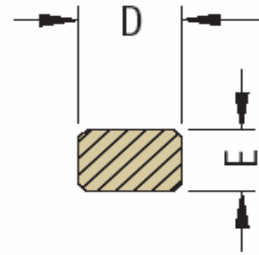
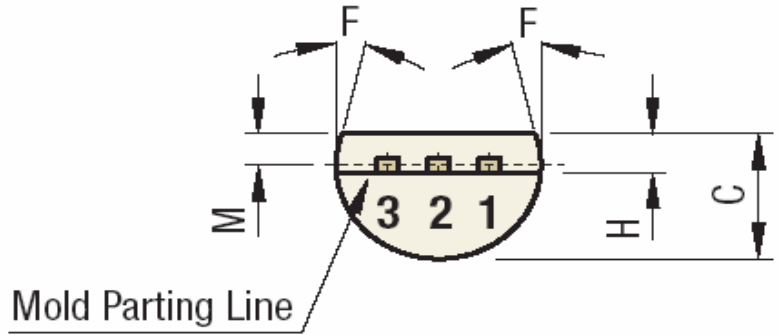
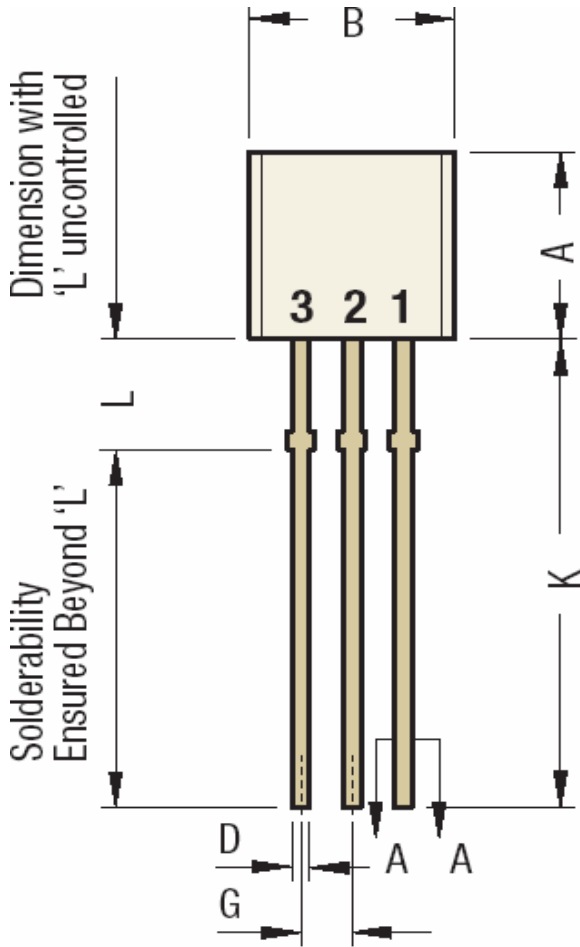
DESCRIPTION	SYMBOL	TEST CONDITION	TYP	UNIT	
Transistors Frequency	f <sub>T</sub>	I <sub>C</sub> =50mA, V <sub>CE</sub> =2V, f=100MHz			
			<b>NPN</b>	200	MHz
			<b>PNP</b>	150	MHz
Output Capacitance	C <sub>ob</sub>	I <sub>E</sub> =0, V <sub>CB</sub> =10V, f=1MHz			
			<b>NPN</b>	7	pF
			<b>PNP</b>	9	pF
Input Capacitance	C <sub>ib</sub>	V <sub>BE</sub> =0.5V, f=1MHz			
			<b>NPN</b>	50	pF
			<b>PNP</b>	110	pF

\*Pulse Test: Pulse Width ≤ 300ms, Duty Cycle 2%

BC635\_BC640Rev\_5 180712E

For Lead Free Parts, Device Part # will be Prefixed with "T"

TO-92 Leaded Plastic Package

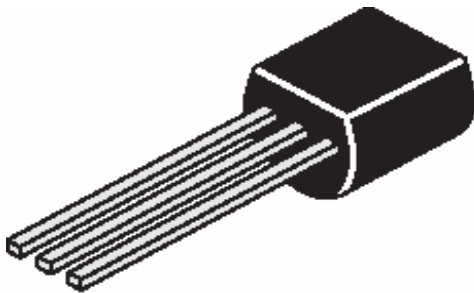


DIM	Min	Max
A	4.32	5.33
B	4.45	5.20
C	3.18	4.19
D	0.40	0.55
E	0.30	0.55
F	5°	

All Dimensions are in mm

DIM	Min	Max
G	1.14	1.40
H	1.20	1.80
K	12.5	
L	1.982	2.082
M	1.03	1.53

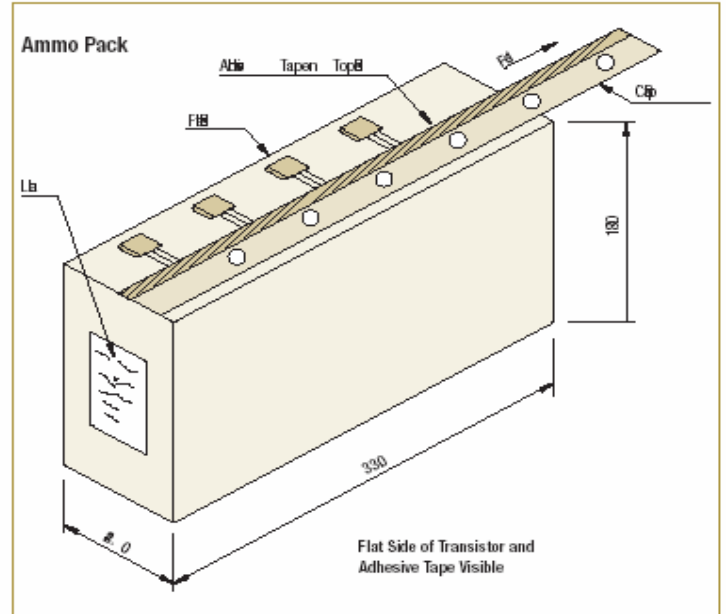
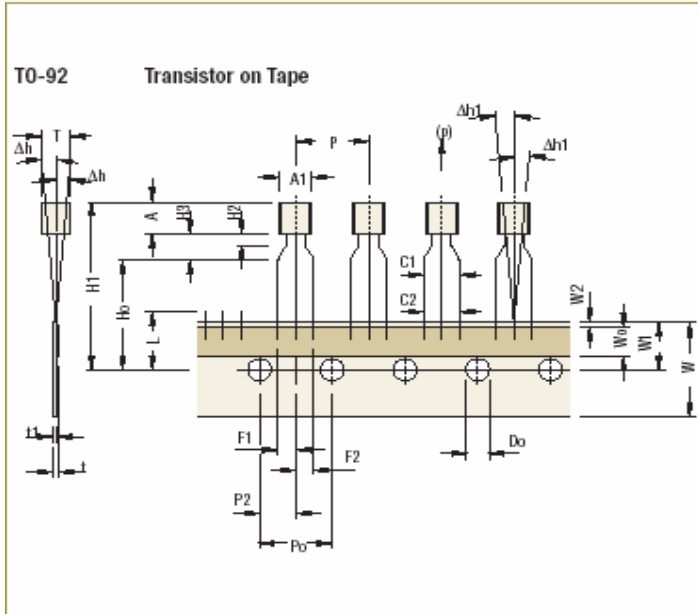
- Pin 1 Base
- Pin 2 Collector
- Pin 3 Emitter



TO-92  
Plastic Package

For Lead Free Parts, Device Part # will be Prefixed with "T"

TO-92 Tape and Ammo Packaging



All Dimensions are in mm

Tape Specifications

Item description	Symbol	TO-92			
		Min	Nom	Max	Tol
Body width	A1	4.45		5.20	
Body height	A	4.32		5.33	
Body thickness	T	3.18		4.19	
Pitch of component <sup>Cr</sup>	P		12.7		±1.0
Feed hole pitch <sup>S1</sup>	Po		12.7		±0.3
Feed hole center to component centre <sup>S2</sup>	P2		6.35		±0.4
Comp. alignment, Side view <sup>S3</sup>	Dh		0	1.0	
Comp. alignment, Front view <sup>S3</sup>	Dh1		0	1.3	
Tape width <sup>Cr</sup>	W		18		±0.5
Hold down tape width <sup>Cr</sup>	W0		6		±0.2
Hole position	W1		9		+0.7 -0.5
Hold-down tape position	W2	0.0		0.7	
Lead wire clinch height	Ho		16		±0.5
Component height	H1			24.0	
Length of clipped leads	L			11.0	
Feed hole diameter <sup>Cr</sup>	Do		4		±0.2
Total tape thickness <sup>S4</sup>	t			1.2	
Lead-to-lead distance <sup>Cr</sup>	F1, F2	2.4		2.7	
Stand off	H2	0.45		1.45	
Clinch height	H3			3.0	
Lead parallelism <sup>Cr</sup>	C1-C2			0.22	
Pull-out force	(p)	6N			

Taping Specification

- Maximum alignment deviation between leads not to be greater than 0.20 mm.
- Maximum non-cumulative variation between tape feed holes shall not exceed 1 mm in 20 pitches.
- Hold down tape not to exceed beyond the edge(s) carrier tape and there shall be no exposure of adhesive.
- No more than 3 consecutive missing components is permitted.
- A tape trailer, having at least three feed holes is required after the last component.
- Splices shall not interfere with the sprocket feed holes.

§1 Cumulative pitch error 1.0 mm/20 pitch.

§2 To be measured at bottom of clinch.

§3 At top of body.

§4 t1 = 0.3 – 0.6 mm

Cr Critical Dimension.

All Dimensions are in mm

**Packaging Information**

T & A: Tape and Ammo Pack; T & R: Tape and Red; Bulk: Loose in Poly bags; Tube: Tube and Ammo Pack; k: 1.000

Package/Case Type	Packaging Type	Std. Packing		Inner Carton		Outer Carton		
		Qty	Qty	Size L x W x H	Gross Weight	Qty	Size L x W x H	Gross Weight
				(cm)	(Kg)		(cm)	(Kg)
TO-92	Bulk	1,000	5K	19x19x8	1.10	80K	43x40x35	20.0
	T&A	2,000	2K	32x4.5x20	0.70	40K	43x40x35	15.20

**Component Disposal Instructions**

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

**Customer Notes**

**Disclaimer**

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s). CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.



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Page 5 of 5

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Data Sheet