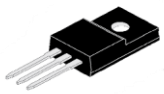
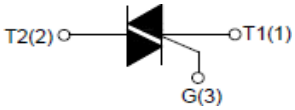
Continental Device India Pvt. Limited

16A TRIACs

BT139X



TO-220FP



TO-220F
Leaded Package
Plastic Insulated
RoHS compliant

DESCRIPTION

BT139 series triacs with low holding and latching current are especially recommended for use on current are especially recommended for use on middle and small resistance type power load.

MAIN FEATURES

Parameter	Symbol	Value	Unit
RMS on-state current	$I_{T(RMS)}$	16	A
Non repetitive surge peak Off-state voltage/ Repetitive peak reverse voltage(Tj=25℃)	V_{DRM} /V_{RRM}	600/800	V

ABSOLUTE MAXIMUM RATINGS

Parameter		Symbol	Value	Unit
Storage junction temperature range		Tstg	-40 ~ 150	℃
Operating junction temperature range		Tj	-40 ~ 125	℃
Repetitive peak off-state voltage(Tj=25℃)		V_{DRM}	600/800	V
Repetitive peak reverse voltage(Tj=25℃)		V_{RRM}	600/800	V
Non repetitive surge peak Off-state voltage		V_{DSM}	VDRM+100	V
Non repetitive peak reverse voltage		V_{RSM}	VRRM+100	V
RMS on-state current	(T_C=80℃)	$I_{T(RMS)}$	16	A
Non repetitive surge peak on-state current (full cycle, F=50Hz)		I_{TSM}	140	A
I^2t value for fusing (tp=10ms)		I^2t	98	A^2s
Critical rate of rise of on-state current(I_G=2×I_{GT})	I-II-III	dI/dt	50	A/μs
	IV		10	
Peak gate current		I_{GM}	2	A
Average gate power dissipation		$P_{G(AV)}$	0.5	W
Average gate power dissipation		P_{GM}	5	W

ELECTRICAL CHARACTERISTICS at T_a = 25 °C

Parameter	Symbol	Test Condition	Quadrant	Value				Unit
				D	E	F	...	
Triggering gate current	I_{GT} (Max)	VD=12V RL=33Ω	I-II-III	5	10	25	35	mA
			IV	10	25	70	70	
Triggering gate voltage	V_{GT} (Max)		ALL	1.3				V
Non-triggering gate voltage	V_{GD} (Min)	V_D=V_{DRM} T_j=125℃, R_L=3.3KΩ	ALL	0.2				V
Latching current	I_L (Max)	I_G=1.2I_{GT}	I- III	15	30	50	40	mA
			II- IV	20	40	100	60	
Holding current	I_H (Max)	I_T=100mA	ALL	10	25	40	30	mA
Critical rate of rise of off-state voltage	dV/dt (Min)	V_D=2/3V_{DRM} Gate Open T_j=125℃		20	50	100	100	V/µs

STATIC CHARACTERISTICS

Parameter	Symbol	Test Condition	Temp.	Value (Max)	Unit
Peak on-state voltage drop	V_{TM}	I_{TM}=20A tp=380µs	T_j=25℃	1.6	V
Max. Forward Current	I_{DRM}	V_D=V_{DRM} V_R=V_{RRM}	T_j=25℃	5	µA
Max. Reverse Current	I_{RRM}		T_j=125℃	1	mA

THERMAL RESISTANCES

Parameter	Symbol	Test Condition	Value (Max)	Unit
Junction to case thermal resistance	$R_{th(j-c)}$	Junction to case(AC)	2.3	℃/W

Typical Characteristic curves

FIG.1 Maximum power dissipation versus RMS on-state current

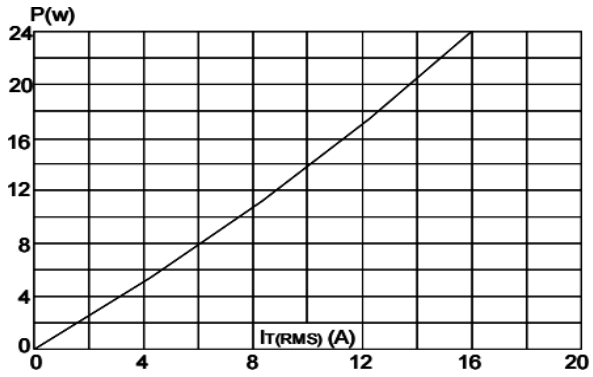


FIG.2: RMS on-state current versus case temperature

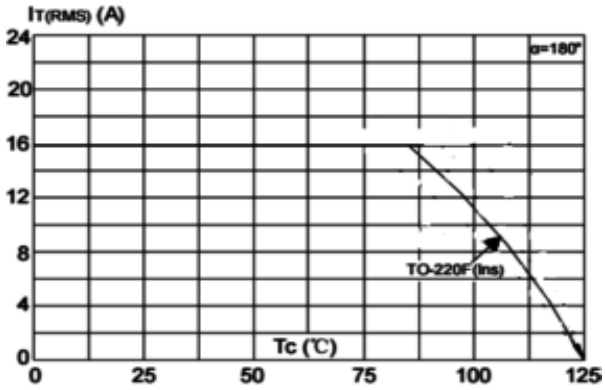


FIG.3: Surge peak on-state current versus number of cycles

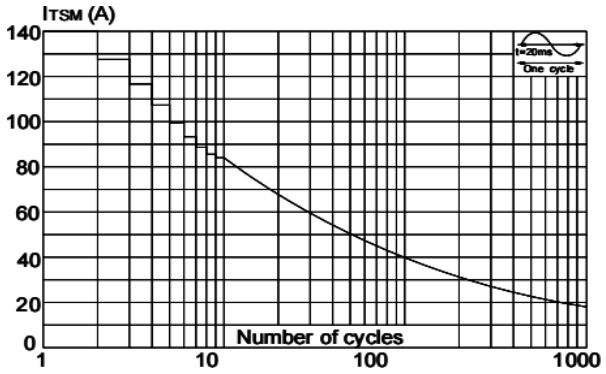
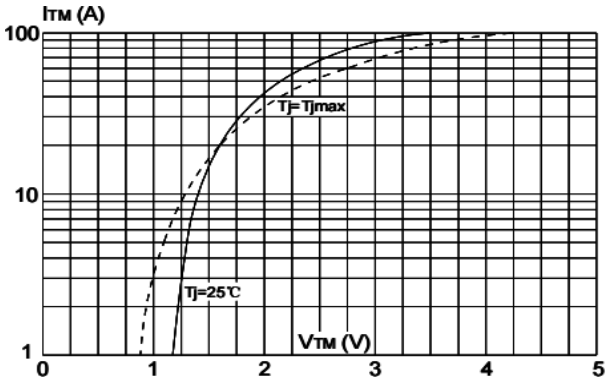


FIG.4: On-state characteristics (maximum values)



Typical Characteristic curves (continued…)

FIG.5: Non-repetitive surge peak on-state current for a sinusoidal pulse with width tp<20ms and corresponding value of I t (I-II-III:dI/dt < 50A/µs; IV:dI/dt < 10A/µs)

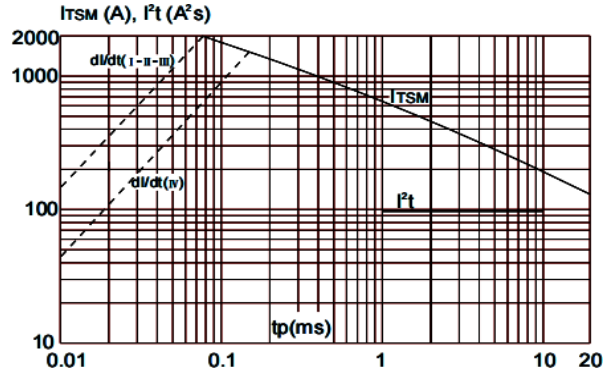


FIG.6: Relative variations of gate trigger current versus junction temperature

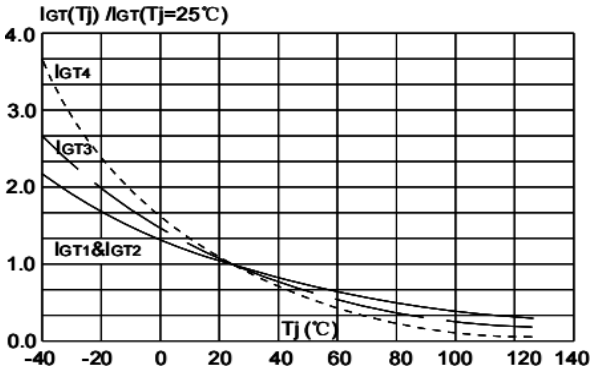


FIG.7: Relative variations of holding current versus junction temperature

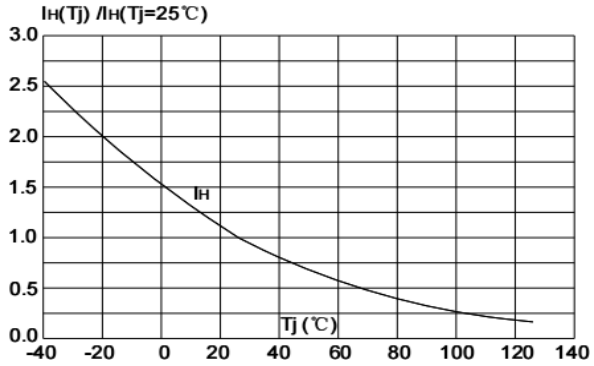
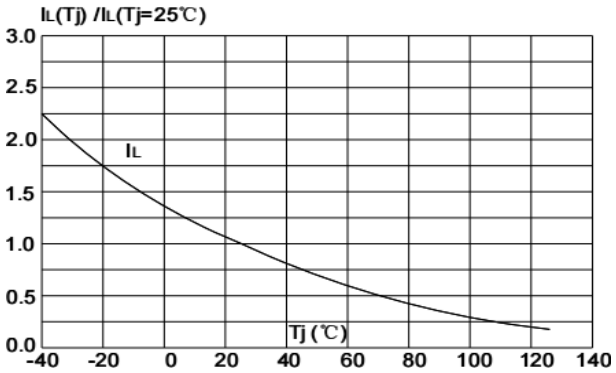
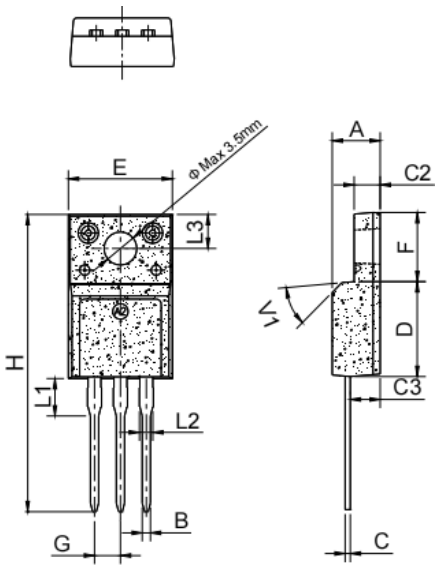


FIG.8: Relative variations of latching current versus junction temperature



Package Details

TO-220F Leaded Package



Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	4.50		4.90	0.177		0.193
B	0.74	0.80	0.83	0.029	0.031	0.033
C	0.47		0.65	0.019		0.026
C2	2.45		2.75	0.096		0.108
C3	2.60		3.00	0.102		0.118
D	8.80		9.30	0.346		0.366
E	9.80		10.4	0.386		0.410
F	6.40		6.80	0.252		0.268
G		2.54			0.1	
H	28.0		29.8	1.102		1.173
L1		3.63			0.143	
L2	1.14		1.70	0.045		0.067
L3		3.30			0.130	
V1		45°			45°	

Recommended Product Storage Environment for Discrete Semiconductor Devices

This storage environment assumes that the Diodes and transistors are packed properly inside the original packing supplied by CDIL.

- Temperature 5 °C to 30 °C
- Humidity between 40 to 70 %RH
- Air should be clean.
- Avoid harmful gas or dust.
- Avoid outdoor exposure or storage in areas subject to rain or water spraying .
- Avoid storage in areas subject to corrosive gas or dust. Product shall not be stored in areas exposed to direct sunlight.
- Avoid rapid change of temperature.
- Avoid condensation.
- Mechanical stress such as vibration and impact shall be avoided.
- The product shall not be placed directly on the floor.
- The product shall be stored on a plane area. They should not be turned upside down. They should not be placed against the wall.

Shelf Life of CDIL Products

The shelf life of products is the period from product manufacture to shipment to customers. The product can be

Floor Life of CDIL Products and MSL Level

When the products are opened from the original packing, the floor life will start.
For this, the following JEDEC table may be referred:

JEDEC MSL Level		
Level	**Time**	**Condition**
1	Unlimited	≤30 °C / 85% RH
2	1 Year	≤30 °C / 60% RH
2a	4 Weeks	≤30 °C / 60% RH
3	168 Hours	≤30 °C / 60% RH
4	72 Hours	≤30 °C / 60% RH
5	48 Hours	≤30 °C / 60% RH
5a	24 Hours	≤30 °C / 60% RH
6	Time on Label(TOL)	≤30 °C / 60% RH

Customer Notes

Component Disposal Instructions

1. CDIL Semiconductor Devices are RoHS compliant, customers are requested to please dispose as per prevailing Environmental Legislation of their Country.
2. In Europe, please dispose as per EU Directive 2002/96/EC on Waste Electrical and Electronic Equipment (WEEE).

Disclaimer

The product information and the selection guides facilitate selection of the CDIL's Semiconductor Device(s) best suited for application in your product(s) as per your requirement. It is recommended that you completely review our Data Sheet(s) so as to confirm that the Device(s) meet functionality parameters for your application. The information furnished in the Data Sheet and on the CDIL Web Site/CD are believed to be accurate and reliable. CDIL however, does not assume responsibility for inaccuracies or incomplete information. Furthermore, CDIL does not assume liability whatsoever, arising out of the application or use of any CDIL product; neither does it convey any license under its patent rights nor rights of others. These products are not designed for use in life saving/support appliances or systems. CDIL customers selling these products (either as individual Semiconductor Devices or incorporated in their end products), in any life saving/support appliances or systems or applications do so at their own risk and CDIL will not be responsible for any damages resulting from such sale(s).

CDIL strives for continuous improvement and reserves the right to change the specifications of its products without prior notice.