CMOSTEK

CMT2160A

27 - 960 MHz OOK/(G)FSK Transmitter SoC

MCU Features

- High-performance 8051
  - Single instruction cycle (1T-8051)
  - Up to 24 MIPS
  - 8 kB RAM / 8 kB OTP
  - Built-in 512 bits EEPROM
  - 12 kB ROM (API function library)
  - 1-Wire simulation debugging interface
- Digital peripherals
  - Built-in AES-128 acceleration engine
  - True random number generator (TRNG)
  - 1x UART
  - 1x SPI
  - 1x WDT
  - 1x RTC (internal 32 kHz only)
  - 2x 16-bit multifunction timer (supports PWM/CCP)
  - 9x GPIO, all supporting interrupt-on-change and wake-up
- Analog peripherals
  - Sub-1G transmitter module
  - 12-bit SAR-ADC, 100 ksps, 4-ch
  - Built-in high-speed 3 / 12 / 24 MHz RC oscillator
  - Built-in low-power 32 kHz RC oscillator
- Code security
  - Built-in multi-level program protection achieving high security
  - Serial port (S3S interface) for programming with lock function

Application

- Garage door remote control
- Remote access control system
- Consumer wireless remote control
- Smart home
- Home security
- Active RFID tags
- Wireless sensor network
- WM-Bus T1 mode

Sub-1G Transmitter Features

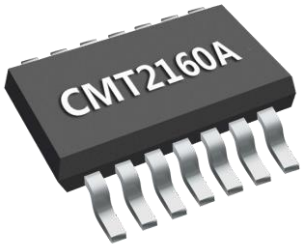
- Operating frequency range : 27 - 960 MHz
- Modulation mode : OOK, G/FSK
- Data rate
  - 0.5 - 40 kbps (OOK)
  - 0.5 - 200 kbps (G/FSK)
- Output power : +10 dBm (Max.)
- Operating current: 13mA @+10 dBm, 433.92 MHz FSK
- Transmission differential PA, supporting automatic antenna tuning
- PA ramping configurability according to rate

Low-power Features

- Operating temperature : - 40 ºC ~ + 85 ºC
- Operating voltage : 2.0 - 3.6 V
- Shutdown current : 300 nA
- RTC mode current : 800 nA

Ordering Information

Product Model	Package	Min. Ordering Quantity
CMT2160A-ESR	SOP14 T&R	2500 pcs
CMT2160A-ESB	SOP14 Tube	1,000 pcs



SOP14

8.65 x 6.00 x 1.75 mm

Description

Embedded with a 1T-8051 core, the CMT2160A is a low-power SoC RF transmitter enriched with below features.

1. The chip series supports wireless transmission @ 27 - 960 MHz with OOK or (G)FSK modulation.
2. Its differential PA supports automatic antenna tuning, fit for miniaturized PCB-onboard micro-strip antenna design.
3. 8 kB OTP program bank and 12 kB ROM (for API library storage).
4. With 1-Wire simulation function, users can download the target debugging code directly to the on-chip PRAM through the dedicated 1-Wire debugger, achieving more convenient debugging comparing with the troublesome debugging of traditional OTP chip with no online simulation supporting and a specific simulator required.
5. Supporting built-in AES-128 accelerator, true random number generator (TRNG), and 32-bit serial number (UUID), fit for remote or active RFID applications requiring encrypted transmission.
6. Supporting dual-clock operating architecture, namely, the system operating with the internal high-speed clock meanwhile the internal low-power RC oscillation operating for periodical wake-up from low-power mode.
7. Built-in 12-bit high-precision and high-speed SAR-ADC, fit for wireless sensor acquisition scenarios.

Table of Contents

1 Electrical Specifications

If nothing else stated, all measurement results are obtained using the evaluation board CMT216xA-EM Rev001 under the conditions of VDD= 3.3 V，T_{OP}= 25°C，F_{RF} = 433.92 MHz, matching to 50 Ω impedance and +10 dBm output power.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VDD	Temperature range is -40℃ ~ +85℃	2.0		3.6	V
Operating temperature	T_{OP}		- 40		+ 85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Ratings

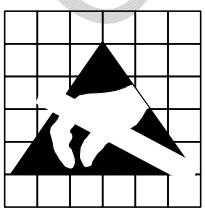
Table 2. Absolute Maximum Ratings [1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	VDD		-0.3	3.6	V
Interface voltage	VIN		-0.3	VDD + 0.3	V
Junction temperature	TJ		-40	125	℃
Storage temperature	TSTG		-50	150	℃
Soldering temperature	TSDR	Lasts for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT216xA is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed with good ESD protection.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

1.3 Transmitter Specifications

Table 3. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	HXOSC connecting 26 MHz crystal oscillator	27		480	MHz
			630		960	MHz
Data rate	DR	OOK	0.5		40	kbps
		(G)FSK	0.5		200	kbps
Output power range	P_{OUT}	Differential PA mode	0		+10	dBm
FSK frequency deviation range	F_{DEV}	630 ~ 960 MHz	1		300	kHz
		315 ~ 480 MHz	0.5		150	kHz
		210 ~ 320 MHz	0.33		100	kHz
		160 ~ 240 MHz	0.25		75	kHz
		105 ~ 160 MHz	0.17		50	kHz
Output power step	P_{STEP}			1		dB
Transmission startup time [1]	T_{PLL}	API tx_sym_prepare_for_transmission execution time		900		uS
FSK transmission current [2]	$I_{DD-315F}$	0dBm				mA
		+5dBm				mA
		+7dBm				mA
		+10dBm				mA
	$I_{DD-434F}$	0dBm		8.12		mA
		+5dBm		9.00		mA
		+7dBm		9.44		mA
		+10dBm		11.70		mA
	$I_{DD-868F}$	0dBm				mA
		+5dBm				mA
		+7dBm				mA
		+10dBm				mA
	$I_{DD-915F}$	0dBm				mA
		+5dBm				mA
		+7dBm				mA
		+10dBm				mA
OOK transmission current [3]	$I_{DD-434O}$	0dBm		5.06		mA
		+5dBm		5.50		mA
		+7dBm		5.80		mA
		+10dBm		6.80		mA
	$I_{DD-868O}$	0dBm				mA
		+5dBm				mA
		+7dBm				mA
		+10dBm				mA
Phase noise	PN_{434}	100kHz frequency deviation		80		dBc/Hz

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		200kHz frequency deviation		83		dBc/Hz
		400kHz frequency deviation		91		dBc/Hz
		600kHz frequency deviation		96		dBc/Hz
		1.2MHz frequency deviation		105		dBc/Hz
	PN_{868}	100kHz frequency deviation		-77		dBc/Hz
		200kHz frequency deviation		-79		dBc/Hz
		400kHz frequency deviation		-87		dBc/Hz
		600kHz frequency deviation		-91		dBc/Hz
		1.2MHz frequency deviation		-100		dBc/Hz
Harmonic output	$H2_{315}$	2^{nd} harmonic @630MHz, +13dBm				dBm
	$H3_{315}$	3^{nd} harmonic @945MHz, +13dBm				dBm
	$H2_{434}$	2^{nd} harmonic @867.84MHz, +13dBm				dBm
	$H3_{434}$	3^{nd} harmonic @1301.76MHz, +13dBm				dBm
	$H2_{868}$	2^{nd} harmonic @1736MHz，+13dBm				dBm
	$H3_{868}$	3^{nd} harmonic @2604MHz，+13dBm				dBm
	$H2_{915}$	2^{nd} harmonic @1830MHz，+13dBm				dBm
	$H3_{915}$	3^{nd} harmonic @2745MHz，+13dBm				dBm
OOK adjusted extinction ratio				60		dB
Occupied bandwidth	OBW_{315}	A bandwidth of -20 dBc, RBW = 1kHz，SR = 1.2kbps		6		kHz
	OBW_{434}	A bandwidth of -20 dBc, RBW = 1kHz，SR = 1.2kbps		7		kHz

Notes

[1]. This item already includes the crystal startup time.

[2]. It includes the 8051 core current. HFOSC uses the internal 24 MHz high-speed RC as the clock source.

[3]. A high/low duty cycle of 50% for baseband data.

1.4 Oscillator Specifications

Table 4. Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Parameter
High-speed oscillating frequency	Crystal frequency [1]	F_{HXOSC}			26		MHz
	Frequency precision [2]				±20		ppm
	Load capacitor	$C_{HX-LOAD}$			15		pF
	Equivalent resistance	R_{HX-ESR}				60	Ω
	Startup time [3]	t_{HXOSC}			400		us
32.768 KHz crystal oscillator	Crystal frequency [1]	F_{LXOSC}			32.768		KHz
	Frequency precision [2]						ppm
	Load capacitor	$C_{LX-LOAD}$			9	12.5	pF
	Equivalent resistance	R_{LX-ESR}			50	90	KΩ
	Startup time [3]	t_{LXOSC}			1		s
Internal high speed RC oscillator	RC oscillating frequency	F_{HF_RC}		3	24	24	MHz
	Frequency precision [4]				1		%
Internal 32 kHz RC oscillator	Oscillator frequency	F_{LP_RC}			32		kHz
	Frequency precision [4]				1		%

Notes:

[1]. An external reference clock can be used to drive the XTAL pin directly through a coupling capacitor. It's required the peak-to-peak level of the external reference clock is between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF error between the receiver and its paired transmitter.

[3]. This parameter is crystal dependent to a large degree.

[4]. Frequency precision is the value after calibration, which is related to environmental factors. Users can initiate calibration through calling the calibration API.

1.5 EEPROM Specifications

Table 5. EEPROM Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Re- writing time	t_{EE-WR}	Call eeprom_write_words for [1]		14		ms/unit
		Call eeprom_set_dec_count [2]		42		ms
Programming number of times		Call eeprom_write_words [1]	10,000	100,000		cycles
		Call eeprom_set_dec_count [2]		1,000,000		cycles

Notes:

[1]. The internal EEPROM is re-written by calling API eeprom_write_words for direct re-writing, and the operation address points to a 2-byte storage unit, namely, each unit is 2 bytes.

[2]. The internal EEPROM is re-written by calling API eeprom_set_dec_count for enhanced re-writing. By applying Balanced Gray Code algorithm, it can endure more than 1,000,000 writing operations. It should be noted that the function is fixed to operating 3 units, namely, this field occupies 6 bytes with only the lower 22 bits data valid in the written value and the read value.

1.6 High-precision ADC Performance

Table 6. High-precision ADC Performance

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	R_{ADC}			12		bit
Effective number of bits	NOEB			10		bit
Conversion input range	V_{AIN}		0		V_{REF}	V
ADC clock frequency	f_{ADC}		0.5	1.0	2.0	MHz
ADC total conversion time Sampling time [1] Successive approximation conversion time [2] Data update time	t_{CONV} t_{SAMP} t_{SAR} t_{UPDATE}		16 2 13 1	16 2 13 1	25 8 16 1	$1/F_{ADC}$
ADC data refresh rate	f_S	FADC = 1 MHz		62.5		kHz
Stabilization time [3]	t_{STAB}				10	uS
Offset error	E_{OS}	FADC = 1 MHz		±4		LSB
Gain error	E_G	FADC = 1 MHz		±4		LSB
Integral nonlinearity error	INL	FADC = 1 MHz		±3		LSB
Differential nonlinearity error	DNL	FADC = 1 MHz		±2		LSB
ADC reference voltage Regulator output Bandgap reference External input reference [4]	V_{REF}	 Input from B6 pin	 1.0	 V_{DDA} 1.2 	 V_{DDA}	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply voltage range	V_{BAT}		2.0		3.6	V
Operating voltage range	V_{DDA}		2.0	2.2	3.6	V
Operating current	I_{ADC}	V_{DDA} = 2.2 V		220		uA
Power efficiency	P_E			7.6		pJ/Conv
Leakage current	$I_{LEAKAGE}$			2.2		nA

Notes:

[1]. The sampling time can be configured by software. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

[2]. The successive approximation conversion time can be configured by software. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

[3]. The stabilization time refers to the analog circuit stabilization time after power-on, which depends on the system design.

[4]. The external input reference voltage must be at least 1.0 V, otherwise the circuit may not work properly.

1.7 Temperature Sensor Specifications

Table 7. Temperature Sensor Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Temperature measurement error [1]	T_{ERR}	VDD：2.2 ~ 3.6 V TOP：-20 ~ +70 ℃		TBD		℃
		VDD：2.2 ~ 3.6 V TOP：-40 ~ +125 ℃		TBD		
Temperature sensor circuit establishing time	t_{STAB}				5	uS

Notes:

[1]. Based on the average of two measurements.

1.8 Supply Voltage Detection Specifications

Table 8. Supply Voltage Detection Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Battery measuring error [1]	V_{ERR}		-50		+50	mV
Battery sensor circuit establishing time	t_{STAB}				5	uS

Notes:

[1]. Based on the average of two measurements.

1.9 DC Specifications

Table 9. DC Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Active mode operating current [1] (HFOSC = 24MHz)	I_{AM_24}	CLK_SYS_DIV=1, F_{SYSCLK}=24 MHz		2.05		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=12 MHz		1.41		mA
		CLK_SYS_DIV=4, F_{SYSCLK}=6 MHz		1.07		mA
		CLK_SYS_DIV=8, F_{SYSCLK}=3 MHz		0.9		mA
		CLK_SYS_DIV=16, F_{SYSCLK}=1.5 MHz		0.81		mA
Active mode operating current (HFOSC = 12MHz)	I_{AM_12}	CLK_SYS_DIV=1, F_{SYSCLK}=12 MHz		1.18		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=6 MHz		0.84		mA
		CLK_SYS_DIV=4, F_{SYSCLK}=3 MHz		0.67		mA
		CLK_SYS_DIV=8, F_{SYSCLK}=1.5 MHz		0.58		mA
Active mode operating current (HFOSC = 3MHz)	I_{AM_3}	CLK_SYS_DIV=1, F_{SYSCLK}=3 MHz		0.45		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=1.5 MHz		0.37		mA
Sleep mode (deep sleep)	I_{SDN}	Call sys_shutdown function, then LFOSC module is disabled		300		nA
Sleep mode (RTC)	I_{RTC}	Call sys_shutdown function, then the internal LFOSC module is enabled and the internal LPOSC (32 kHz) is selected.		800		nA
OTP code loading [2]	I_{LOAD}			4.6		mA

Notes:

[1]. The program runs the While(1) loop, and the GPIO has no load.

[2]. *Charge Pump* is enabled. See CUS_SYSCTL20 register description for details.

1.10 AC Specifications

Table 10. AC Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level output	V_{OH}	Load is 1 kΩ, VDD = 3.3V	VDD-0.4			V
Low level output	V_{OL}	Load is 1kΩ, VDD = 3.3V			0.4	V
High level input	VIH	VDD = 3.3V		0.7*VDD		V
		VDD = 2.0V		0.7*VDD		V
Low level input	V_{IL}	VDD = 3.3V		0.2*VDD		V
		VDD = 2.0V		0.2*VDD		V
Port leakage current	I_{LKG}	VDD = 2.0V - 3.6V		TBD		nA

1.11 Typical Performance of High-frequency Transmission

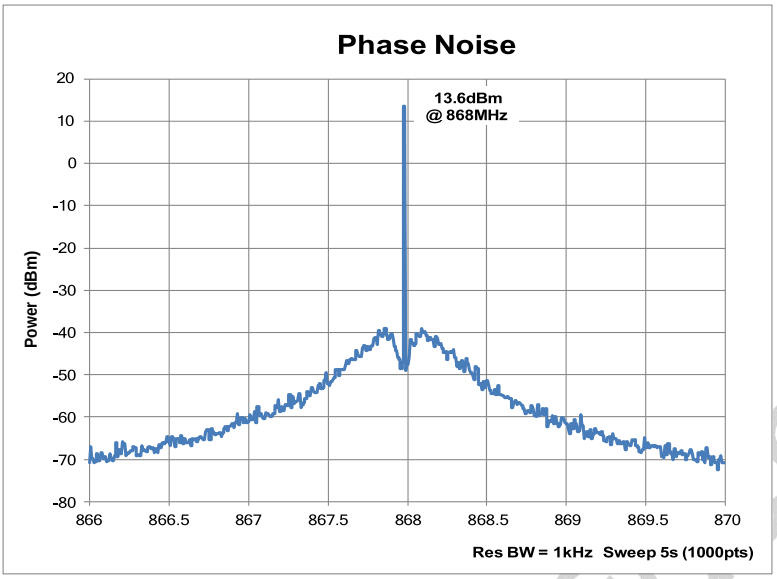


Figure 1. Phase Noise @ F_{RF} = 868 MHz, P_{OUT} = +13 dBm, un-modulated

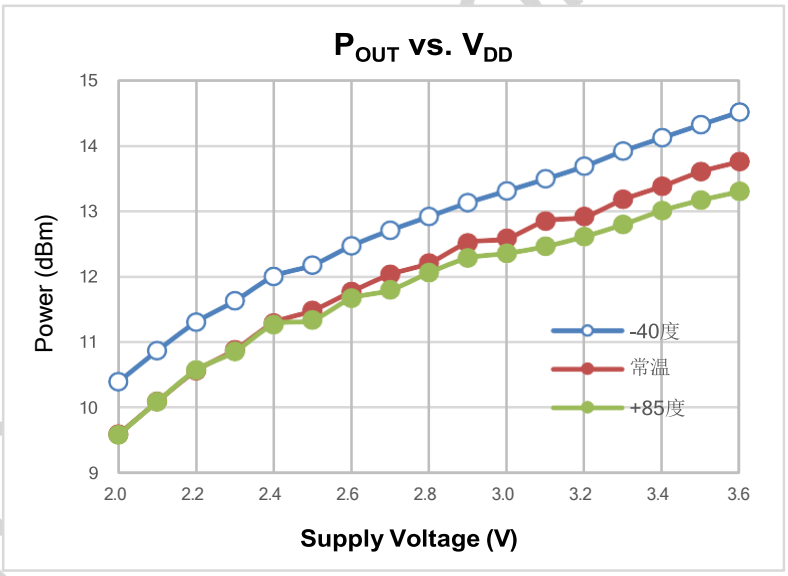


Figure 2. Output Power Vs. Supply Voltage

F_{RF} = 433.92 MHz, P_{OUT} = +13 dBm

2 Pin Description

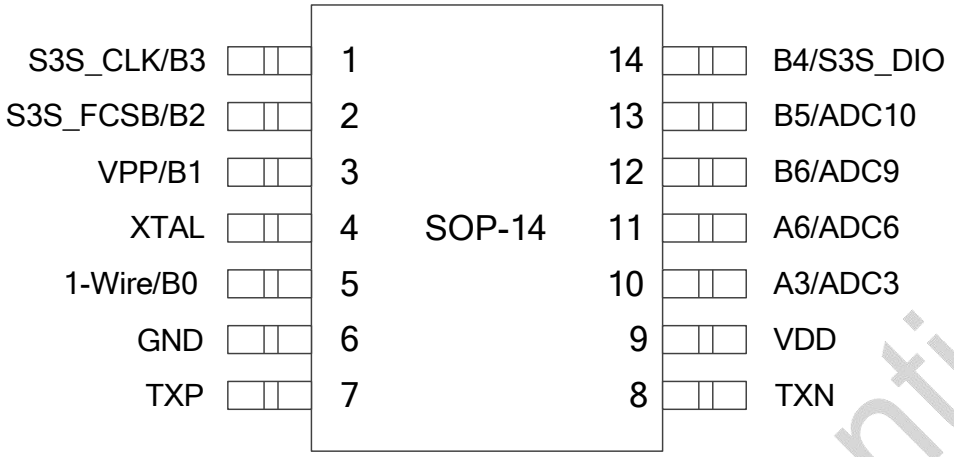


Figure 3. CMT2160A SOP14 Pin Arrangement

Table 11. CMT2160A Pin Description

Pin#	Name	Type		Description
1	S3S_CLK/B3	IO	B3	GPIO11, one of the general purpose GPIOs.
		IO	S3S_CLK	Chip programming bus S3S, programming clock line.
2	S3S_FCSB/B2	IO	B2	GPIO10, one of the general purpose GPIOs.
		IO	S3S_FCSB	Chip programming bus S3S, chip selection programming line.
3	VPP/B1	IO	B1	GPIO9, one of the general purpose GPIOs.
		A	VPP	Chip OTP programming VPP, 6.5 V voltage input pin.
4	XTAL	A		Crystal input pin, connect 26 MHz crystal to GND. See Section 1.4 Crystal Specifications for details.
5	1-Wire/B0	IO	B0	GPIO8, one of the general purpose GPIOs.
		IO	1-Wire	1-wire chip debugging line.
6	GND	A		Power supply - input pin.
7	TXP	A		High-frequency transmission differential PA+ output pin.
8	TXN	A		High-frequency transmission differential PA- output pin.
9	VDD	A		Power+ input pin.
10	A3/ADC3	IO	A3	GPIO3, one of the general purpose GPIOs.
		A	ADC3	ADC5, ADC sampling channel 3.
11	A6/ADC6	IO	A6	GPIO6, one of the general purpose GPIOs.
		A	ADC6	ADC6, ADC sampling channel 6.
12	B6/ADC9	IO	B6	GPIO14, one of the general purpose GPIOs.
		A	ADC9	ADC9, ADC sampling channel 9.
13	B5/ADC10	IO	B5	GPIO13, one of the general purpose GPIOs.
		A	ADC10	ADC10, ADC sampling channel 10.
14	S3S_DIO/B4	IO	B4	GPIO12, one of the general purpose GPIOs.
		IO	S3S_DIO	Chip programming bus S3S, data programming line.

3 Functional Description

Embedded with a Sub-1 GHz OOK / (G)FSK transmitter, the CMT2160A is a high-performance 8051 SoC, suitable for low-power wireless transmission applications in the 27 - 960 MHz band. The series chips integrate the below major modules [1].

- High-performance 8051 core with rich peripheral resources.
- Sub-1G OOK / (G) FSK transmission module.
- Multi-channel 12-bit high-precision successive approximation ADC

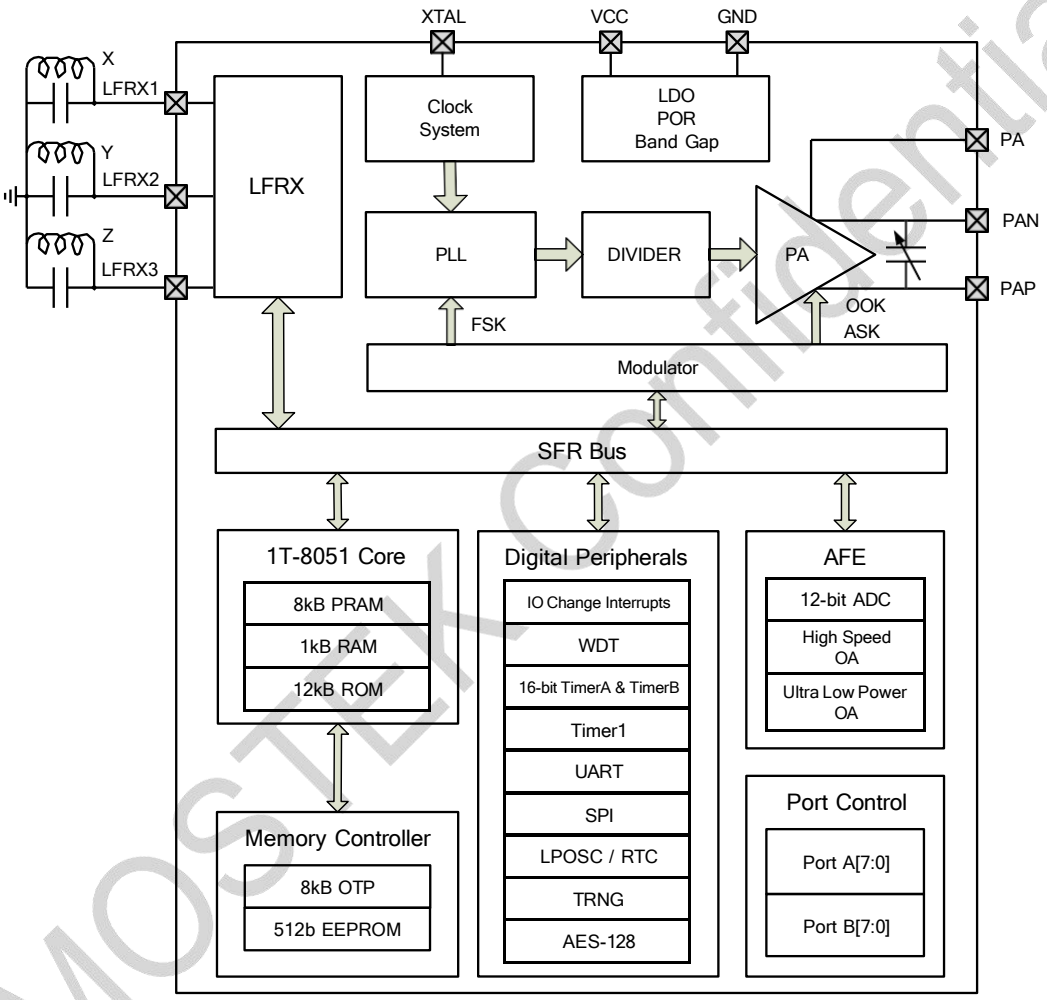


Figure 4. System Block Diagram

Notes:

[1]. This is the general block diagram for CMT216xA series. Different product models consist of different module combinations, namely not all models provide the full function modules.

3.1 High-performance 8051

Built-in with enhanced 1T-8051 and 24 MHz high-speed RC oscillator, the CMT2160A supports dual-clock operating mode. achieving 24 MIPS high-speed operating. Meanwhile, the low-speed clock is provided by the internal low-speed 32 kHz RC oscillator, serving as the clock source of the low-power RTC.

For memory architecture, the on-chip 8 kB OTP ROM is for code storage, 1 kB XRAM for data storage and 512 bits EEPROM for key data storage in case of power loss. Meanwhile, it integrates 12 kB MASK ROM for the storage of API library function of various chip modules.

For digital peripherals, it supports on-chip AES-128 operation acceleration engine, true random number generator, one UART, one SPI, watchdog, two 16-bit multi-function timers, one RTC, and 9 ports with multiplexing functions.

For development and debugging, the CMT216xA series chips adopt 1-wire debugging interface, which requires only one single wire connecting to the debugger to download code to PRAM, achieving simple and convenient online debugging.

3.2 Sub-1G Transmission Module

The CMT2160A integrates a high-performance Sub-1G transmitter, which applies simple differential PA architecture and supports automatic antenna tuning function, achieving a low-cost, small sized PCB board carried antenna design with only a few peripheral components required.

The transmitter supports 3 modulation modes, OOK, GFSK and FSK. Appling the fractional phase-locked loop technology, it requires only one 26 MHz crystal oscillator to achieve most of the 27～960 MHz band coverage.

3.3 12-bit High-precision ADC

Embedded with a multi-channel 12-bit high-precision successive approximation ADC along with a buffer based operational amplifier, it can fulfill high-resistance signal conditioning, fit for a variety of sensor acquisition applications.

4 Ordering Information

Table 12. CMT2160A Ordering Information

Model	Description	Packaging	Package Option	Operating Condition	Minimum Ordering Quantity
CMT2160A-ESR [1]	27 - 960 MHz transmitter SoC	SOP14	T&R	1.8 to 3.6 V, - 40 to 85 °C	2500
CMT2160A-ESB [1]	27 - 960 MHz transmitter SoC	SOP14	Tube	1.8 to 3.6 V, - 40 to 85 °C	1000

Notes:

[1]. E refers to extended Industrial product rating, which supports a temperature range from -40 to +85 °C.

S refers to the packaging type SOP14.

R refers to Tape & Reel package type, and the minimum ordering quantity (MOQ) is 2500 pieces.

B refers to Tube package type, and the minimum ordering quantity (MOQ) is 1000 pieces.

Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

5 Packaging Information

The packaging information of the CMT2160A is shown in the below figure.

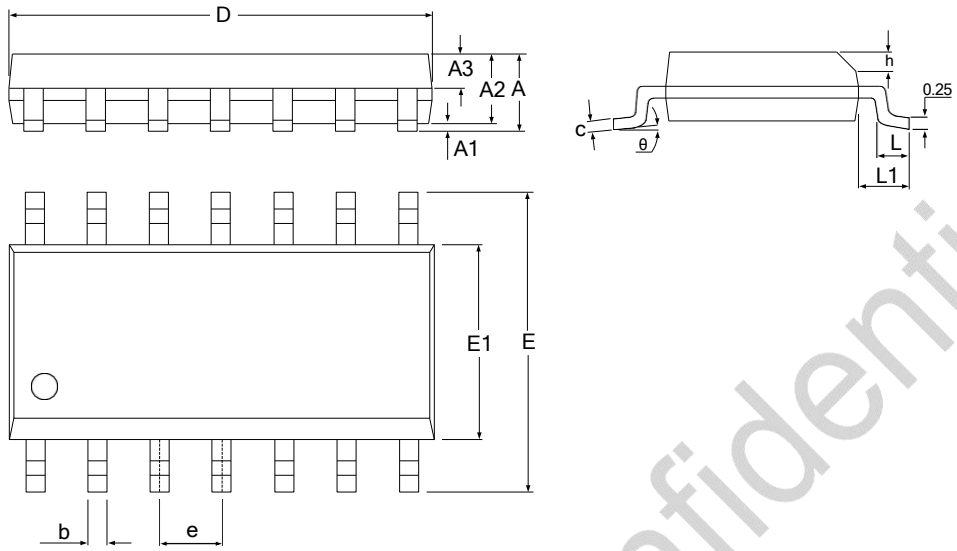


Figure 5. SOP14 Packaging

Table 13. SOP14 Packaging Scale

Symbol	Scale (mm) Maximum		
	Min.	Typ.	Min.
A	-	-	1.75
A1	0.05	-	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	-	0.48
c	0.21	-	0.26
D	8.45	8.65	8.85
E	5.80	6.00	6.20
E1	3.70	3.90	4.10
e	1.27 BSC		
L	0.25	-	0.50
L1	1.05 BSC		
θ	0	-	8°

6 Top Marking

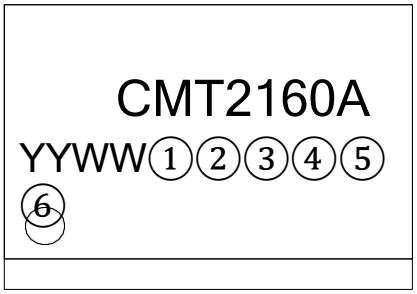


Figure 6. CMT2160A Top Marking

Table 14. CMT2160A Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Size	0.6 mm, align right
Font Width	0.4 mm
Line 1 Marking	CMT2160A refers to model CMT2160A.
Line 2 Marking	YYWW is the date code assigned by the package factory. YY is the last 2 digits of the year. WW is the working week. ①②③④⑤⑥ is the internal tracing code.

7 Related Documents

Table 15. CMT2160A Related Documents

Doc No.	Document Name	Description
AN290	CMT216x User Guide	CMT216xA series chips user guide.
AN280	CMT216xA Low-frequency Receiving Function User Guide	CMT216xA 3D low-frequency receiving function user guide.
AN281	CMT216xA ADC and AFE User Guide	CMT216xA series chip ADC and analog front end user guide.
AN282	CMT216xA API Function Library User Guide	CMT216xA series chip API function library user guide.
AN284	CMT216xA Development Environment Establishment and Debugging	CMT216xA development environment establishment and debugging quick start guide.
AN286	CMT216xA Register Guide	CMT216xA series chip SFR register detail description.

8 Revise History

Table 16. Revise History Records

Version No.	Chapter	Description	Date
0.6	All	Initial version	2019-07-01
0.7	All		2019-09-01
0.8	1	Update Transmitter Specifications	2019-11-01

9 Contacts

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