CMOSTEK

CMT2189D

27-960 MHz OOK/(G)FSK Transmitter SoC

MCU Feature

- High-performance 8051
  - Single-instruction cycle (1T-8051)
  - Up to 24 MIPS
  - 8kB RAM / 8kB OTP
  - Embedded 512-bit EEPROM
  - 12kB ROM (API function library)
  - Single-wire online simulating and debugging interface
- Digital peripheral
  - Embedded AES-128 accelerator engine
  - Truly random number generator
  - 1x UART
  - 1x SPI
  - 1x WDT
  - 1x RTC (internal 32 KHz only)
  - 2x 16 bit multi-functional timer (with PWM/CCP support)
  - 14x GPIO, all supporting level changing interrupt/wake-up
- Analog peripheral
  - Sub-1G transmitter module
  - 12-bit SAR-ADC, 100 ksps, 8-ch
  - Embedded high-speed 3 /12 / 24MHz RC oscillator
  - Embedded low-power 32 kHz RC oscillator
- Code security
  - Embedded multi-level program protection with high confidential performance
  - Series port for programming (S3S interface) with lock function

Application

- Garage door remote control
- Entrance control system remote control
- Wireless remote control in consumer electronics
- Intellegent home auomation
- Home Security
- Active RFID tags
- Wireless sensor network
- WM-Bus T1 mode

Sub-1G Transmitter Feature

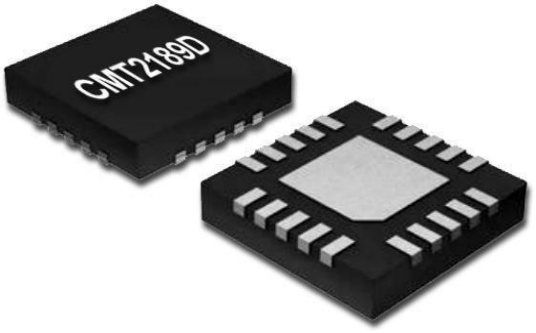
- Operating frequency: 27 ~ 960 MHz
- Demodulation mode: OOK, G/FSK
- Data rate:
  - 0.5 ~ 40 kbps (OOK)
  - 0.5 ~ 200 kbps (G/FSK)
- Output power: +13 dBm (Max.)
- Operating current: 18mA@+13dBm, 433.92MHz, FSK
- Single-ended high-efficient Class E transmitter PA
- PA ramping slope varying according to rate

Low-power Feature

- Operating voltage: 2.0 ~ 3.6 V
- Operating temperature: - 40 ~ + 85 ºC
- Power-off current: 300 nA
- RTC mode: 800 nA

Ordering Information

Part Number	Packaging	MOQ
CMT2189D-EQR	QFN20 T&R	3,000 pcs



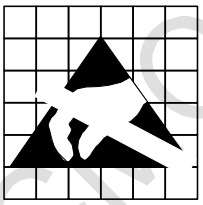
QFN20

4.00 x 4.00 x 0.85 mm

Description

The CMT2189D is a low-power SoC RF transmitter embedded with enhanced 1T-8051 core:

1. The series chips support 27 - 960 MHz, OOK or (G)FSK modulation wireless transmission function.
2. The high-efficient single-ended PA supports adjustable output power ranging in 0 ~ +13 dBm, with +13 dBm transmission consuming merely a power of 18 mA.
3. It supports 8 kB OTP program storage and 12 kB ROM (for storage of API function library).
4. 1-WIRE online simulation function is adopted. Users can download target debugging code directly to on-chip PRAM to run, through the dedicated 1-WIRE debugger, which can achieve quite convenient debugging rather than traditional OTP chip debugging that requires specific simulator with no support of online simulation and results in quite troublesome operations.
5. The support of embedded AES-128 accelerator and truly random number generator (TRNG) as well as 32-bit sequence number (ID) makes it suitable for transmission application scenarios with enciphering requirements, such as remote control and active RFID.
6. It supports dual-clock architecture, with the internal high-speed clock supporting system internal running, and the internal low-power RC oscillator supporting low-power timer based wake-up mode operating.
7. The embedded 12-bit high-precision and high-speed SAR-ADC is fitting for sensors used in wireless acquisition application scenarios.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

Table of Contents

1 Electrical Specifications

V_{DD}= 3.3 V，T_{OP}= 25 °C，F_{RF} = 433.92 MHz, matching to 50 Ω impedance, outputting +10dBm power, if nothing else stated. All measurement results are obtained using the evaluation board CMT2189D-EM if nothing else stated.

1.1 Recommended Operating Conditions

Table 1. Recommended Operating Conditions

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating supply voltage	VDD	Temperature range is -40℃ ~ +85℃	2.0		3.6	V
Operating temperature	T_{OP}		- 40		+ 85	℃
Supply voltage slope			1			mV/us

1.2 Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Condition	Min.	Typ.	Max.
Supply voltage	VDD		-0.3	3.6	V
Interface voltage	VIN		-0.3	VDD + 0.3	V
Junction temperature	TJ		-40	125	℃
Storage temperature	TSTG		-50	150	℃
Soldering temperature	TSDR	Lasts for at least 30 seconds		255	℃
ESD rating[2]		Human body model (HBM)	-2	2	kV
Latch-up current		@ 85℃	-100	100	mA

Notes:

[1]. Exceeding *the Absolute Maximum Ratings* may cause permanent damage to the equipment. This value is a pressure rating and does not imply that the function of the equipment is affected under this pressure condition, but if it is exposed to absolute maximum ratings for extended periods of time, it may affect equipment reliability.

[2]. The CMT2189D is a high performance RF integrated circuit. The operation and assembly of this chip should only be performed on a workbench with good ESD protection.

1.3 Transmitter Specification

Table 3. Transmitter Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	HXOSC connecting 26 MHz crystal oscillator	27		480	MHz
			630		960	MHz
Data rate	DR	OOK	0.5		40	kbps
		(G)FSK	0.5		200	kbps
Output power range	P_{OUT}	Single-ended PA mode	0		+13	dBm
FSK frequency deviation range	F_{DEV}	630 ~ 960 MHz	1		300	kHz
		315 ~ 480 MHz	0.5		150	kHz
		210 ~ 320 MHz	0.33		100	kHz
		160 ~ 240 MHz	0.25		75	kHz
		105 ~ 160 MHz	0.17		50	kHz
Output power step	P_{STEP}			1		dB
Transmission startup time [1] (Startup time)	T_{PLL}	The execution time of API function tx_sym_prepare_for_transmission.		900		uS
FSK transmission current [2]	$I_{DD-315F}$	0 dBm		7.9		mA
		+5 dBm		10.0		mA
		+7 dBm		11.4		mA
		+10 dBm		14.0		mA
		+13 dBm		17.0		mA
	$I_{DD-434F}$	0 dBm		8.0		mA
		+5 dBm		10.3		mA
		+7 dBm		11.8		mA
		+10 dBm		14.3		mA
		+13 dBm		20.6		mA
	$I_{DD-868F}$	0 dBm		9.2		mA
		+5 dBm		12.2		mA
		+7 dBm		13.8		mA
		+10 dBm		17.7		mA
		+13 dBm		23.5		mA
	$I_{DD-915F}$	0 dBm		9.1		mA
		+5 dBm		12.3		mA
		+7 dBm		13.7		mA
		+10 dBm		18.3		mA
		+13 dBm		25.0		mA
OOK transmission current [3]	$I_{DD-434O}$	0 dBm		6.5		mA
		+5 dBm		7.2		mA
		+7 dBm		7.8		mA

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
		+10 dBm		8.5		mA
		+13 dBm		12.0		mA
	$I_{DD-868O}$	0 dBm		6.8		mA
		+5 dBm		8.0		mA
		+7 dBm		8.9		mA
		+10 dBm		10.5		mA
		+13 dBm		13.7		mA
Phase noise	PN_{434}	100 kHz frequency deviation		80		dBc/Hz
		200 kHz frequency deviation		83		dBc/Hz
		400 kHz frequency deviation		91		dBc/Hz
		600 kHz frequency deviation		96		dBc/Hz
		1.2 MHz frequency deviation		105		dBc/Hz
	PN_{868}	100 kHz frequency deviation		-77		dBc/Hz
		200 kHz frequency deviation		-79		dBc/Hz
		400 kHz frequency deviation		-87		dBc/Hz
		600 kHz frequency deviation		-91		dBc/Hz
		1.2 MHz frequency deviation		-100		dBc/Hz
Harmonic output	$H2_{315}$	2nd harmonic @630 MHz, +13 dBm				dBm
	$H3_{315}$	3rd harmonic @945 MHz, +13 dBm				dBm
	$H2_{434}$	2nd harmonic @867.84 MHz, +13 dBm				dBm
	$H3_{434}$	3rd harmonic @1301.76 MHz, +13 dBm				dBm
	$H2_{868}$	2nd harmonic @1736 MHz, +13 dBm				dBm
	$H3_{868}$	3rd harmonic @2604 MHz, +13 dBm				dBm
	$H2_{915}$	2nd harmonic @1830 MHz, +13 dBm				dBm
	$H3_{915}$	3rd harmonic @2745 MHz, +13 dBm				dBm
OOK adjusted extinction ratio				60		dB
Occupied bandwidth	OBW_{315}	-20 dBc bandwidth, RBW = 1kHz, SR = 1.2kbps		6		kHz
	OBW_{434}	-20 dBc bandwidth, RBW = 1kHz, SR = 1.2kbps		7		kHz

Notes:

[1]. This item includes the crystal startup time.

[2]. It includes 8051 core current and HFOSC applies the internal 24 MHz high-speed RC as the clock source.

[3]. Baseband data applies 50% high/low duty cycle.

1.4 Oscillator Specification

Table 4. Oscillator Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit	Parameter
High-frequency crystal oscillator	Crystal frequency [1]	F_{HXOSC}			26		MHz
	Frequency precision [2]				±20		ppm
	Load capacitance	$C_{HX-LOAD}$			15		pF
	Equivalent series resistance	R_{HX-ESR}				60	Ω
	Startup time [3]	t_{HXOSC}			400		us
Internal high-frequency RC oscillator	RC oscillating frequency	F_{HF_RC}		3	24	24	MHz
	Frequency precision [4]				1		%
Internal 32 KHz RC oscillator	Oscillator frequency	F_{LP_RC}			32		kHz
	Frequency precision [4]				1		%

Notes:

[1]. The CMT2189D can directly use an external reference clock to drive the XTAL pin. The peak-to-peak level of the external reference clock is required between 0.3 and 0.7 V.

[2]. It involves:(1) initial tolerance, (2) crystal loading, (3) aging, and (4) temperature changing. The acceptable crystal frequency tolerance is subject to the bandwidth of the receiver and the RF tolerance between the receiver and its paired transmitter.

[3]. This parameter is to a large degree crystal dependent.

[4]. The frequency precision is the value after calibration that is related to environmental factors. Users can call the related calibration API initiatively to have calibration.

1.5 EEPROM Specification

Table 5. EEPROM Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Rewriting time	t_{EE-WR}	Call eeprom_write_words to operate [1]		14		ms/unit
		Call eeprom_set_dec_count to operate [2]		42		ms
Number of programming times		Call eeprom_write_words to operate [1]	10,000	100,000		cycles
		Call eeprom_set_dec_count to operate [2]		1,000,000		cycles

Notes:

[1]. The internal EEPROM is re-written by calling API eeprom_write_words for direct re-writing, and the operation address points to a 2-byte storage unit, namely, each unit is 2 bytes.

[2]. The internal EEPROM is re-written by calling API eeprom_set_dec_count for enhanced re-writing. By applying Balanced Gray Code algorithm, it can endure more than 1,000,000 writing operations. It should be noted that the function is fixed to operating 3 units, namely, this field occupies 6 bytes with only the lower 22 bits data valid in the written value and the read value.

1.6 High-precision ADC Performance Parameter

Table 6. High-precision ADC Performance Parameter Specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	R_{ADC}			12		bit
Effective number of bits	NOEB			10		bit
Conversion input range	V_{AIN}		0		V_{REF}	V
ADC clock frequency	f_{ADC}		0.5	1.0	2.0	MHz
ADC total conversion time Sampling time [1] Successive approximation conversion time [2] Data update time	t_{CONV} t_{SAMP} t_{SAR} t_{UPDATE}		16 2 13 1	16 2 13 1	25 8 16 1	$1/F_{ADC}$
ADC data refresh rate	f_S	F_{ADC} = 1 MHz		62.5		kHz
Stabilization time [3]	t_{STAB}				10	uS
Offset error	E_{OS}	F_{ADC} = 1 MHz		±4		LSB
Gain error	E_G	F_{ADC} = 1 MHz		±4		LSB
Integral nonlinearity error	INL	F_{ADC} = 1 MHz		±3		LSB
Differential nonlinearity error	DNL	F_{ADC} = 1 MHz		±2		LSB
ADC reference voltage Regulator output	V_{REF}			V_{DDA}		V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Bandgap reference External input reference [4]		Input from pin B6	1.0	1.2	V_{DDA}	
Supply voltage range	V_{BAT}		2.0		3.6	V
Operating voltage range	V_{DDA}		2.0	2.2	3.6	V
Operating current	I_{ADC}	V_{DDA} = 2.2 V		220		uA
Power efficiency	P_E			7.6		pJ/Conv
Leakage current	$I_{LEAKAGE}$			2.2		nA

Notes:

[1]. The sampling time can be configured by software. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

[2]. The successive approximation conversion time can be configured by software. See *AN281 CMT216xA ADC and AFE User Guide* or *CMT216xA User Guide* for details.

[3]. The stabilization time refers to the analog circuit stabilization time after power-on, which depends on the system design.

[4]. The external input reference voltage must be at least 1.0 V, otherwise the circuit may not work properly.

1.7 Supply Voltage Detection Specifications

Table 7. Supply Voltage Detection Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Battery measuring error [1]	V_{ERR}		-50		+50	mV
Battery sensor circuit establishing time	t_{STAB}				5	uS

Notes:

[1]. Based on the average of two measurements.

1.8 DC Specifications

Table 8. DC Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Active mode operating current [1] (HFOSC = 24 MHz)	I_{AM_24}	CLK_SYS_DIV=1, F_{SYSCLK}=24 MHz		2.15		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=12 MHz		1.56		mA
		CLK_SYS_DIV=4, F_{SYSCLK}=6 MHz		1.25		mA
		CLK_SYS_DIV=8, F_{SYSCLK}=3 MHz		1.09		mA
		CLK_SYS_DIV=16, F_{SYSCLK}=1.5 MHz		1.00		mA
Active mode operating current (HFOSC = 12 MHz)	I_{AM_12}	CLK_SYS_DIV=1, F_{SYSCLK}=12 MHz		1.22		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=6 MHz		0.91		mA
		CLK_SYS_DIV=4, F_{SYSCLK}=3 MHz		0.75		mA
		CLK_SYS_DIV=8, F_{SYSCLK}=1.5 MHz		0.67		mA
Active mode operating current (HFOSC = 3 MHz)	I_{AM_3}	CLK_SYS_DIV=1, F_{SYSCLK}=3 MHz		0.49		mA
		CLK_SYS_DIV=2, F_{SYSCLK}=1.5 MHz		0.41		mA
Sleep mode (deep sleep)	I_{SDN}	Call sys_shutdown function, then LFOSC module is disabled		300		nA
Sleep mode (RTC)	I_{RTC}	Call sys_shutdown function, then the internal LFOSC module is enabled and the internal LPOSC (32 kHz) is selected.		800		nA
OTP code loading [2]	I_{LOAD}			4.6		mA

Notes:

[1]. The program runs the While(1) loop, and the GPIO has no load.

[2]. Charge Pump is enabled. Refer to register CUS_SYSCTL20 description for more details.

1.9 AC Specifications

Table 9. AC Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
High level output	V_{OH}	Load is 1 kΩ, VDD = 3.3 V	VDD-0.4			V
Low level output	V_{OL}	Load is 1kΩ, VDD = 3.3 V			0.4	V
High level input	VIH	VDD = 3.3 V	0.7*VDD			V
		VDD = 2.0 V	0.7*VDD			V
Low level input	V_{IL}	VDD = 3.3 V			0.2*VDD	V
		VDD = 2.0 V			0.2*VDD	V
Port leakage current	I_{LKG}	VDD = 2.0 V - 3.6 V		TBD		nA

1.10 Typical Performance of High-frequency Transmission

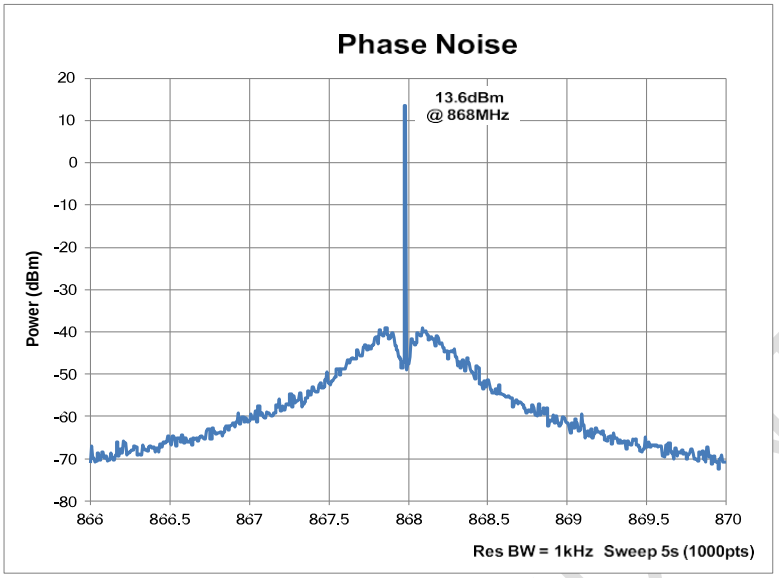


Figure 1. Phase Noise @ F_{RF} = 868 MHz, POUT = +13 dBm, un-modulated

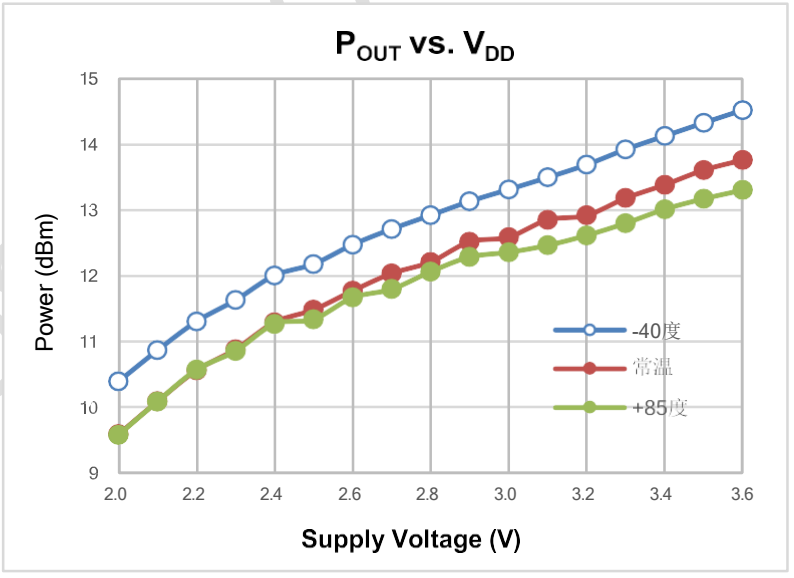


Figure 2. Output Power Vs. Supply Voltage

FRF = 433.92 MHz, POUT = +13 dBm

2 Pin Description

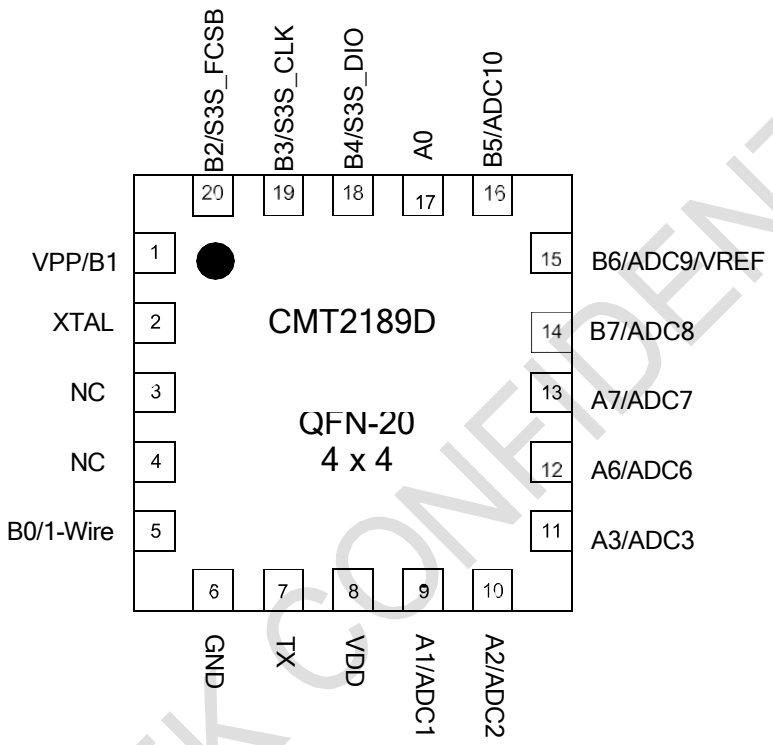


Figure 3. CMT2189D QFN20 Pin Arrangement

Table 10. CMT2189D Pin Description

Pin#	Name	Type		Description
1	VPP/B1	IO	B1	GPIO9, one of the general purpose GPIOs.
		A	VPP	Chip OTP programming VPP, namely 6.5 V voltage input pin
2	XTAL	A		Crystal input pin, connecting to 26 MHz crystal to GND. See Section *1.4 Oscillator* specifications for details.
3	NC	A		Suggest connecting GND.
4	NC	A		Suggest connecting GND.
5	1-Wire/B0	IO	B0	GPIO8, one of the general purpose GPIOs.
		IO	1-Wire	Chip 1-wire debugging line.
6	GND	A		Power supply- input pin.
7	TX	A		High-frequency transmission output pin.
8	VDD	A		Power supply+ input pin.
9	A1/ADC1	IO	A1	GPIO1, one of the general purpose GPIOs.
		A	ADC1	ADC1, ADC sampling channel 1.
10	A2/ADC2	IO	A2	GPIO2, one of the general purpose GPIOs.
		A	ADC2	ADC2, ADC sampling channel 2.
11	A3/ADC3	IO	A3	GPIO3, one of the general purpose GPIOs.
		A	ADC3	ADC3, ADC sampling channel 3.
12	A6/ADC6	IO	A6	GPIO6, one of the general purpose GPIOs.
		A	ADC6	ADC6, ADC sampling channel 6.
13	A7/ADC7	IO	A7	GPIO7, one of the general purpose GPIOs.
		A	ADC7	ADC7, ADC sampling channel 7.
14	B7/ADC8	IO	B7	GPIO15, one of the general purpose GPIOs.
		A	ADC8	ADC8, ADC sampling channel 8.
15	B6/ADC9/VREF	IO	B6	GPIO14, one of the general purpose GPIOs.
		A	ADC9	ADC9, ADC sampling channel 9.
		A	VREF	ADC external reference voltage input.
16	B5/ADC10	IO	B5	GPIO13, one of the general purpose GPIOs.
		A	ADC10	ADC10, ADC sampling channel 10.
17	A0	IO	A0	GPIO0, one of the general purpose GPIOs.
18	B4/S3S_DIO	IO	B4	GPIO12, one of the general purpose GPIOs.
		IO	S3S_DIO	Chip programming bus S3S, namely data programming line.
19	B3/S3S_CLK	IO	B3	GPIO11, one of the general purpose GPIOs.
		IO	S3S_CLK	Chip programming bus S3S, namely programming clock line.
20	B2/S3S_FCSB	IO	B2	GPIO10, one of the general purpose GPIOs.
		IO	S3S_FCSB	Chip programming bus S3S, namely programming chip selection line.

3 Functional Description

Embedded with a Sub-1 GHz OOK / (G)FSK transmitter, the CMT2189D is a high-performance 8051 SoC, suitable for low-power wireless transmission applications in the 27 - 960 MHz band. The series chips integrate the below major modules.

- High-performance 8051 core with enriched peripheral resources.
- Sub-1G OOK / (G) FSK transmission module.
- Multi-channel 12-bit high-precision successive approximation ADC.

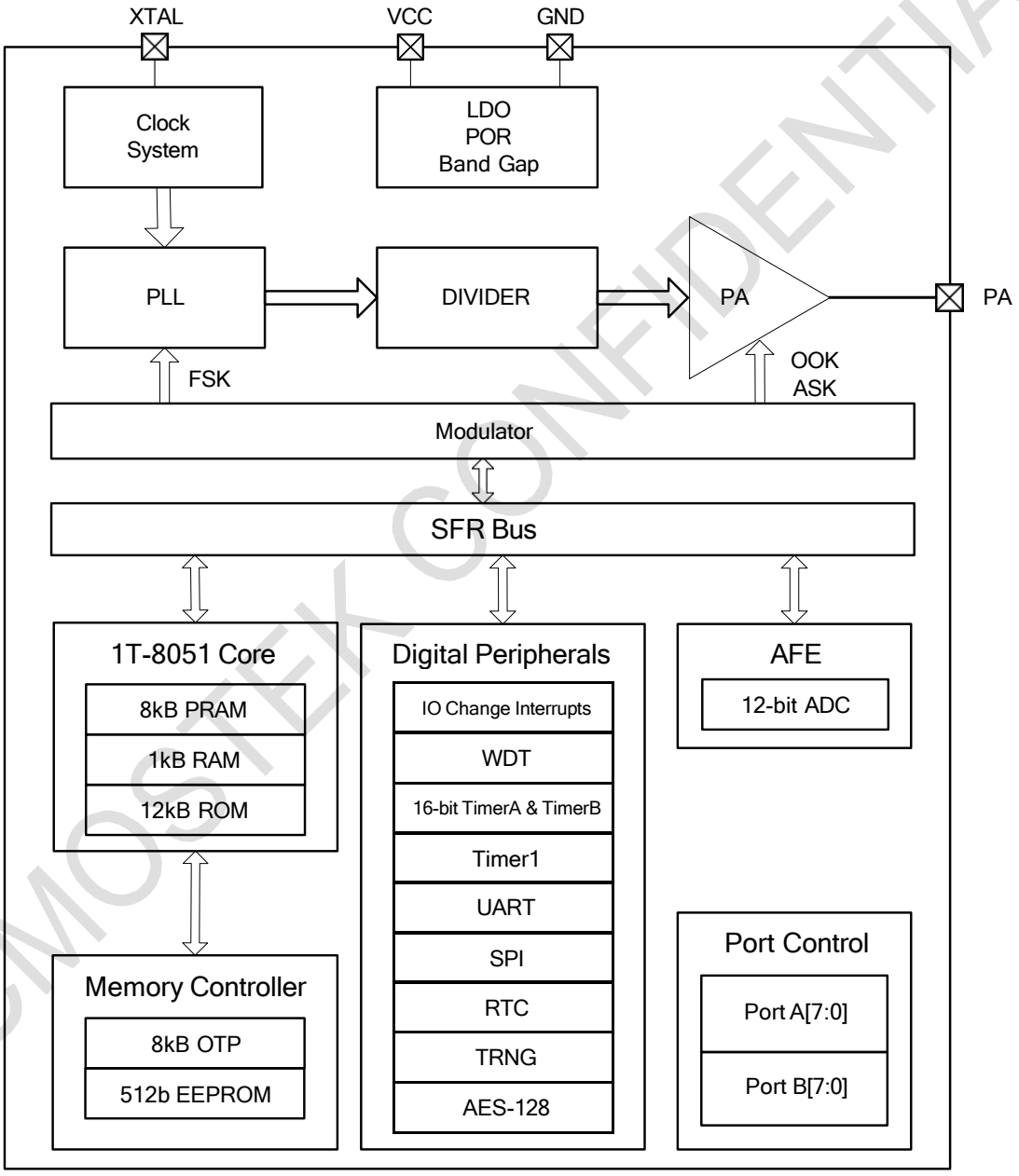


Figure 4. System Block Diagram

3.1 High-performance 8051

Built-in with enhanced 1T-8051 and 24 MHz high-speed RC oscillator, the CMT2189D supports dual-clock operating mode. achieving 24 MIPS high-speed operating. Meanwhile, the low-speed clock is provided by the internal low-speed 32 kHz RC oscillator, serving as the clock source of the low-power RTC.

As for memory architecture, the on-chip 8 kB OTP ROM is for code storage, 8 kB PRAM for code running, 1 kB XRAM for data storage and 512 bits EEPROM for key data storage in case of power loss. Meanwhile, it integrates 12 kB MASK ROM for the storage of API library function of various chip modules.

For digital peripherals, it supports on-chip AES-128 operation acceleration engine, true random number generator, one UART, one SPI, watchdog, two 16-bit multi-function timers, one RTC, and 14 ports with multiplexing functions.

As to development and debugging, the CMT2189D adopts 1-wire debugging interface, which requires only one single wire connecting to the debugger to download code to PRAM, achieving simple and convenient online debugging.

3.2 Sub-1G Single Transmitter

The CMT2189D integrates a high-performance Sub-1G single transmitter which applies single-ended Class E PA architecture with transmission power reaching up to +13 dBm with only a power consumption of 18 mA.

The transmitter supports 3 modulation modes, OOK, GFSK and FSK. Appling the fractional phase-locked loop technology, it requires only one 26 MHz crystal oscillator to achieve most of the 27～960 MHz band coverage.

3.3 12-bit High-precision ADC

Embedded with a multi-channel 12-bit high-precision successive approximation ADC along with a buffer based operational amplifier, it can fulfill high-resistance signal conditioning, fit for a variety of sensor acquisition applications.

4 Ordering Information

Table 11. CMT2189D Ordering Information

Part Number	Description	Packaging	Package Option	Operating Condition	Minimum Ordering Quantity
CMT2189D-EQR [1]	27-960 MHz transmitter SoC	QFN20	T&R	2.0 to 3.6 V -40 to 85℃	3,000

Notes:

[1]. E refers to extended Industrial product rating, which supports a temperature range from -40 to +85 °C.

Q refers to the packaging type QFN20.

R refers to Tape & Reel package type, and the minimum ordering quantity (MOQ) is 3,000 pieces.

Please visit www.cmostek.com for more product/product line information.

Please contact sales@cmostek.comor your local sales representative for sales or pricing requirements.

5 Packaging Information

The packaging information of the CMT2189D is shown in the below figure.

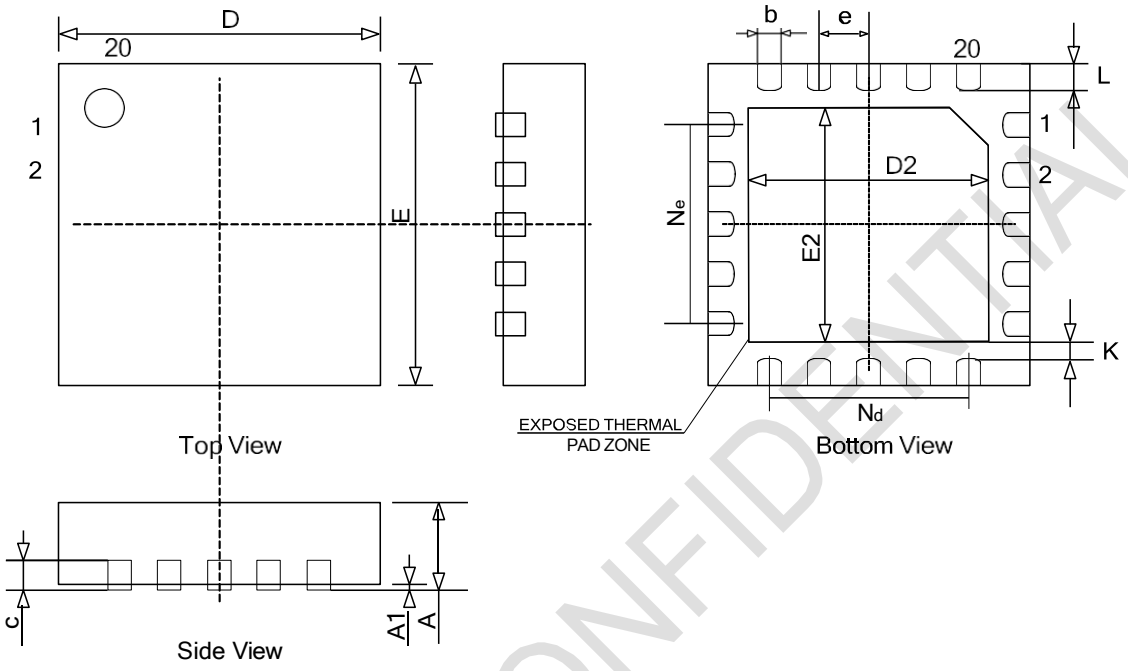


Figure 5. CMT2189D QFN20 Packaging

Table 12. QFN20 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0	0.02	0.05
b	0.20	0.25	0.30
c	0.203 REF		
D	3.90	4.00	4.10
E	3.90	4.00	4.10
Nd	2.00 BSC		
Ne	2.00 BSC		
e	0.50 BSC		
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
L	0.30	0.40	0.50
K	0.15	0.25	0.35

6 Top Marking

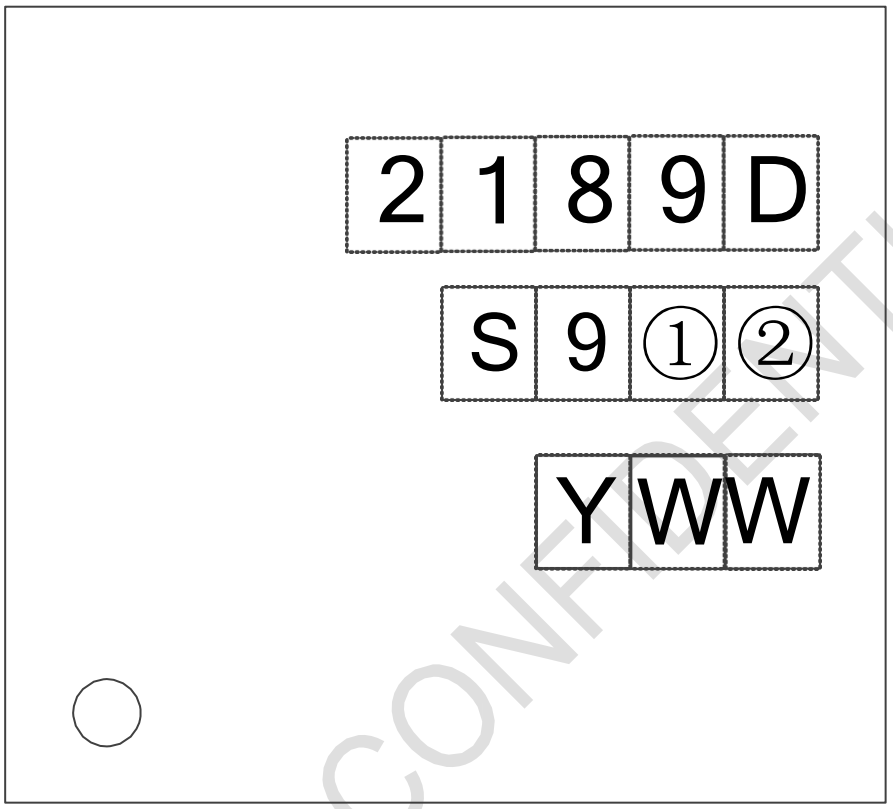


Figure 6. CMT2189D Top Marking

Table 13. CMT2189D Top Marking Information

Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Size	0.5 mm, align right
Font Width	0.4 mm
Line 1 Marking	2189D refers to part number CMT2189D.
Line 2 Marking	S9①② is the internal tracing code.
Line 3 Marking	YWW is the date code assigned by the package factory. Y is the last digit of the year. WW is the working week.

7 Revise History

Table 14. Revise History Records

Version No.	Chapter	Description	Date
0.8	All	Initial version	2020/11/10
0.9	1	Modify the high/low level identification threshold values of input port	2021/09/24
1.0	5	Update some values in packaging size table	2022/01/11

8 Contacts

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