HOPERF

CMT2219B

Ultra Low Power Sub-1GHz RF Receiver

Features

- Frequency range: 127~1020MHz
- Demodulation: OOK, (G)FSK 和(G)MSK
- Data rate: 0.5 ~ 300 kbps
- Sensitivity: -121 dBm 2.0 kbps, F_{RF} = 433.92 MHz
  -111 dBm 50 kbps, F_{RF} = 433.92 MHz
- Voltage range: 1.8 ~3.6 V
- Rx current: 8.5 mA @ 433.92 MHz, FSK (High power mode)
  7.2 mA @ 433.92 MHz, FSK (Low power mode)
- Super Low Power receive mode
- Sleep current: 300 nA, Duty Cycle = OFF
  800 nA, Duty Cycle = ON
- Receiver Features:
  - Fast and stable automatic frequency control (AFC)
  - 3 types of clock data recovery system (CDR)
  - Fast and accurate signal detection (PJD)
- 4-wire SPI interface
- Direct and packet mode supported
- Configurable packet handler and 64-Byte FIFO.
- NRZ, Manchester codec, Whitening codec, Forward Error Correction (FEC)

Descriptions

CMT2219B is an ultra-low power, high performance, OOK (G) FSK RF Receiver suitable for a variety of 140 to 1020 MHz wireless applications. It is part of the CMOSTEK NextGenRF^{TM} RF product line. The product line contains the complete transmitters, receivers and transceivers. The high integration of CMT2219B simplifies the peripheral materials required in the system design. Up to -121 dBm sensitivity optimizes the performance of the application. It supports a variety of packet formats and codec methods to meet the needs of various different applications. In addition, CMT2219B also supports 64-byte Rx FIFO, GPIO and interrupt configuration, Duty-Cycle operation mode, channel sensing, high-precision RSSI, low-voltage detection, power-on reset, low frequency clock output, manual fast frequency hopping, squelch and etc. The features make the application design more flexible and differentiated. CMT2219B operates from 1.8 V to 3.6 V. Only 8.5 mA current is consumed when the sensitivity is -121 dBm, Super-low Power mode can further reduce the chip power consumption.

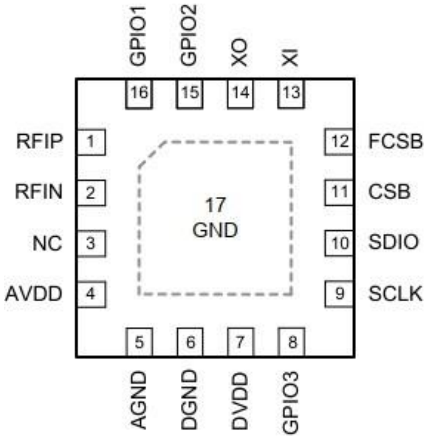
Applications

- Automatic meter reading
- Home security and building automation
- ISM band data communication
- Industrial monitoring and control
- Remote control and security system
- Remote key entry
- Wireless sensor node
- Tag reader

Ordering information

Model	Frequency	Package	MOQ
CMT2219B-EQR	433.92 MHz	QFN16	3,000 pcs
For more information, see Page 33 Table 20.			

QFN16 (3x3)



CMT2218B Top View

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1. Electrical Characteristics

V_{DD}= 3.3 V, T_{OP}= 25 °C, F_{RF} = 433.92 MHz, the sensitivity is measured by receiving a PN9 coded data and matching the impedance to 50Ω under the 0.1% BER standard. Unless otherwise stated, all results are tested on the CMT2219B-EM evaluation board.

1.1 Recommended Operation Condition

Table 1. Recommended operation condition

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Power voltage	V_{DD}		1.8		3.6	V
Operating temperature	T_{OP}		-40		85	℃
Power voltage slope			1			mV/us

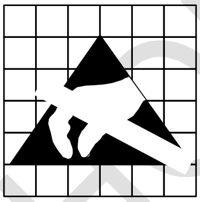
1.2 Absolute Maximum Rating

Table 2. Absolute Maximum Ratings[1]

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}		-0.3	3.6	V
Interface Voltage	V_{IN}		-0.3	V_{DD} +0.3	V
Junction Temperature	T_J		-40	125	℃
Storage Temperature	T_{STG}		-50	150	℃
Soldering Temperature	T_{SDR}	Lasts at least 30 seconds		255	℃
ESD Rating[2]		Human Body Model (HBM)	-2	2	kV
Latch-up Current		@ 85 ℃	-100	100	mA

Notes:

[1]. Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent permanent damage.

1.3 Power Consumption

Table 3. Power consumption specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sleep current	I_{SLEEP}	Sleep mode, sleep timer is off		300		nA
		Sleep mode, sleep timer is on		800		nA
Standby current	$I_{Standby}$	Crystal oscillator is on		1.45		mA
RFS current	I_{RFS}	433 MHz		5.7		mA
		868 MHz		5.8		mA
		915 MHz		5.8		mA
RX current(high power mode)	$I_{Rx\text{-}HP}$	FSK, 433 MHz, 10 kbps,10 kHz F_{DEV}		8.5		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		8.6		mA
		FSK, 915 MHz, 10 kbps,10 kHz F_{DEV}		8.9		mA
RX current (low power mode)	$I_{Rx\text{-}LP}$	FSK, 433 MHz, 10 kbps, 10 kHz F_{DEV}		7.2		mA
		FSK, 868 MHz, 10 kbps, 10 kHz F_{DEV}		7.3		mA
		FSK, 915 MHz, 10 kbps, 10 kHz F_{DEV}		7.6		mA

1.4 Receiver

Table 4. Receiver specification

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR	OOK	0.5		40	kbps
		FSK and GFSK	0.5		300	kbps
Deviation	F_{DEV}	FSK and GFSK	2		200	kHz
Sensitivity @ 433 MHz	$S_{433\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-121		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-116		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power setting）		-115		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-113		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-112		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-111		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-108		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-105		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--103		dBm
Sensitivity @ 868 MHz	$S_{868\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-119		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power setting）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power setting）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-108		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		-99		dBm
Sensitivity	$S_{915\text{-}HP}$	DR = 2.0 kbps, F_{DEV} = 10 kHz		-117		dBm

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
@ 915 MHz		DR = 10 kbps, F_{DEV} = 10 kHz		-113		dBm
		DR = 10 kbps, F_{DEV} = 10 kHz（Low power mode）		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz		-111		dBm
		DR = 20 kbps, F_{DEV} = 20 kHz （Low power mode）		-109		dBm
		DR = 50 kbps, F_{DEV} = 25 kHz		-109		dBm
		DR =100 kbps, F_{DEV} = 50 kHz		-105		dBm
		DR =200 kbps, F_{DEV} = 100 kHz		-102		dBm
		DR =300 kbps, F_{DEV} = 100 kHz		--99		dBm
Saturation Input Signal Level	P_{LVL}				20	dBm
Image Rejection Ratio	IMR	F_{RF}=433 MHz		35		dB
		F_{RF}=868 MHz		33		dB
		F_{RF}=915 MHz		33		dB
RX Channel Bandwidth	BW	RX channel bandwidth	50		500	kHz
Co-channel Rejection Ratio	CCR	DR = 10 kbps, F_{DEV} = 10 kHz; Interference with the same modulation		-7		dB
Adjacent Channel Rejection Ratio	ACR-I	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100 kHz, 200 kHz Channel spacing, interference with the same modulation		30		dB
Alternate Channel Rejection Ratio	ACR-II	DR = 10 kbps, F_{DEV} = 10 kHz; BW=100 kHz, 400 kHzChannel spacing, interference with the same modulation		45		dB
Blocking Rejection Ratio	BI	DR = 10 kbps, F_{DEV} = 10 kHz; ±1 MHz Deviation, continuous wave interference		70		dB
		DR = 10 kbps, F_{DEV} = 10 kHz; ± 2 MHz Deviation, continuous wave interference		72		dB
		DR = 10 kbps, F_{DEV} = 10 kHz; ±10 MHz Deviation, continuous wave interference		75		dB
Input 3rd Order Intercept Point	IIP3	DR = 10 kbps, F_{DEV} = 10 kHz; 1 MHz and 2 MHz Deviation dual tone test, maximum system gain setting.		-25		dBm
RSSI Range	RSSI		-120		20	dBm
More Sensitivity (Typical Configuration)		433.92 MHz, DR = 1.2kbps, F_{DEV} = 5 kHz		-122.9		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 10 kHz		-121.8		dBm
		433.92 MHz, DR = 1.2kbps, F_{DEV} = 20 kHz		-119.5		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 5 kHz		-120.6		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 10 kHz		-120.3		dBm
		433.92 MHz, DR = 2.4kbps, F_{DEV} = 20 kHz		-119.7		dBm
		433.92 MHz, DR = 9.6 kbps, F_{DEV} = 9.6 kHz		-116.0		dBm
		433.92 MHz, DR = 9.6 kbps, FDEV = 19.2 kHz		-116.1		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 10 kHz		-114.2		dBm
		433.92 MHz, DR = 20 kbps, FDEV = 20 kHz		-113.0		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 25 kHz		-110.6		dBm
		433.92 MHz, DR = 50 kbps, FDEV = 50 kHz		-109.0		dBm

		433.92 MHz, DR = 100 kbps, FDEV = 50 kHz		-107.8		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 50 kHz		-103.5		dBm
		433.92 MHz, DR = 200 kbps, FDEV = 100 kHz		-104.3		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 50 kHz		-98.0		dBm
		433.92 MHz, DR = 300 kbps, FDEV = 150 kHz		-101.6		dBm

1.5 Settle Time

Table 5. Settle Time

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Settle time	T_{SLP-RX}	From Sleep to RX		1000		us
	T_{STB-RX}	From Standby to RX		350		us
	T_{RFS-RX}	From RFS to RX		20		us
Note: [1]. $T_{SLP-RX}$is dominated by the crystal oscillator startup time, which depends on its own characteristics.						

1.6 Frequency Synthesizer

Table 6. Frequency Synthesizer Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Frequency range	F_{RF}	Need different matching networks	760		1020	MHz
			380		510	MHz
			190		340	MHz
			127		170	MHz
Frequency resolution	F_{RES}			25		Hz
Frequency tuning time	t_{TUNE}			150		us
Phase noise@ 433 MHz	PN_{433}	10 kHz frequency deviation		-94		dBc/Hz
		100 kHz frequency deviation		-99		dBc/Hz
		500 kHz frequency deviation		-118		dBc/Hz
		1MHz frequency deviation		-127		dBc/Hz
		10 MHz frequency deviation		-134		dBc/Hz
Phase noise@ 868 MHz	PN_{868}	10 kHz frequency deviation		-92		dBc/Hz
		100 kHz frequency deviation		95		dBc/Hz
		500 kHz frequency deviation		-114		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz
Phase noise@ 915 MHz	PN_{915}	10 kHz frequency deviation		-89		dBc/Hz
		100 kHz frequency deviation		-92		dBc/Hz
		500 kHz frequency deviation		-111		dBc/Hz
		1MHz frequency deviation		-121		dBc/Hz
		10 MHz frequency deviation		-130		dBc/Hz

1.7 Crystal Oscillator

Table 7. Crystal Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Crystal frequency[1]	F_{XTAL}			26		MHz
Frequency tolerance[2]	ppm			20		ppm
Load capacitance	C_{LOAD}			15		pF
Equivalent resistance	Rm			60		Ω
Start-up time[3]	t_{XTAL}			400		us

Remarks:

[1]. CMT2219B can use the external reference clock to drive the XIN pin through the coupling capacitor. The peak value of the external clock signal is between 0.3V and 0.7V.

[2]. The value includes (1) initial error; (2) crystal load; (3) aging; and (4) change with temperature. The acceptable crystal frequency tolerance is limited by the receiver bandwidth and the RF frequency offset between the transmitter and the receiver.

[3]. The parameter is largely related to the crystal.

1.8 Low Frequency Oscillator

Table 8. Low Frequency Oscillator Specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Calibration frequency [1]	F_{LPOSC}			32		kHz
Frequency accuracy		After calibration		±1		%
Temperature coefficient [2]				-0.02		%/°C
Supply voltage coefficient [3]				+0.5		%/V
Initial calibration time	$t_{LPOSC-CAL}$			4		ms

Remarks:

[1]. The low frequency oscillator is automatically calibrated to the crystal oscillator frequency at the PUP stage and periodically calibrated at this stage.

[2]. After calibration, the frequency changes with temperature.

[3]. After calibration, the frequency changes with the change of the supply voltage.

1.9 Low Battery Detection

Table 9. Low Battery detection specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Detection accuracy	LBD_{RES}			50		mV

1.10 Digital Interface

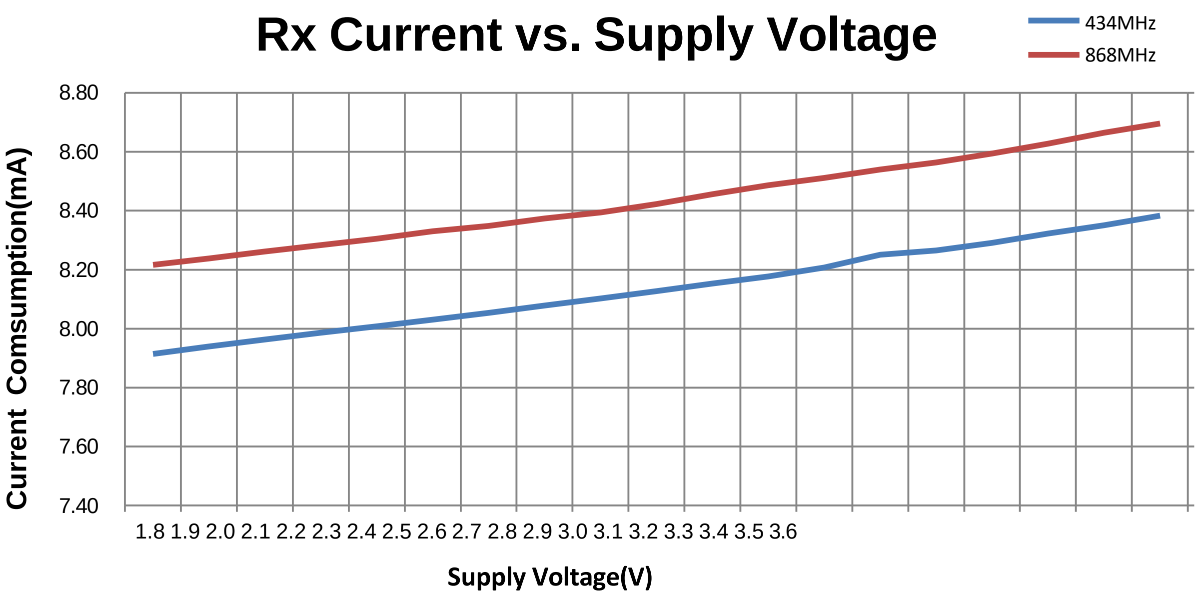
Table 10. Digital interface specifications

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Digital input high level	V_{IH}		0.8			V_{DD}
Digital input low level	V_{IL}				0.2	V_{DD}
Digital output high level	V_{OH}	@I_{OH}= -0.5mA	Vdd-0.4			V
Digital output low level	V_{OL}	@I_{OL}= 0.5mA			0.4	V

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
SCLK Frequency	F_{SCL}				5	MHz
SCLK high time	T_{CH}		50			ns
SCLK low time	T_{CL}		50			ns
SCLK rise time	T_{CR}		50			ns
SCLK fall time	T_{CF}		50			ns

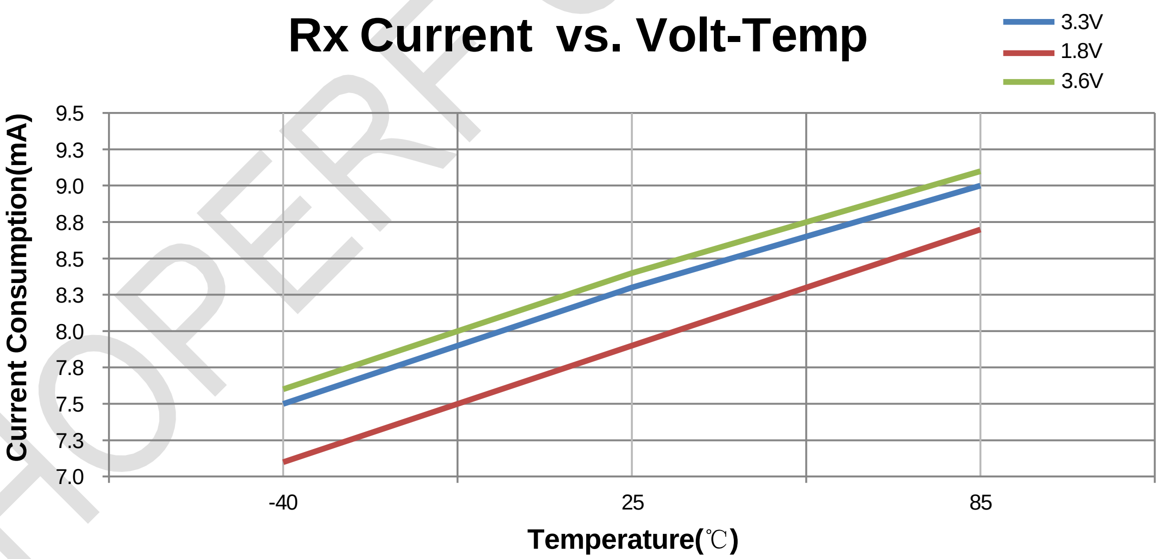
1.11 Figures of Critical Parameters

1.11.1 Rx Current VS. Supply Voltage

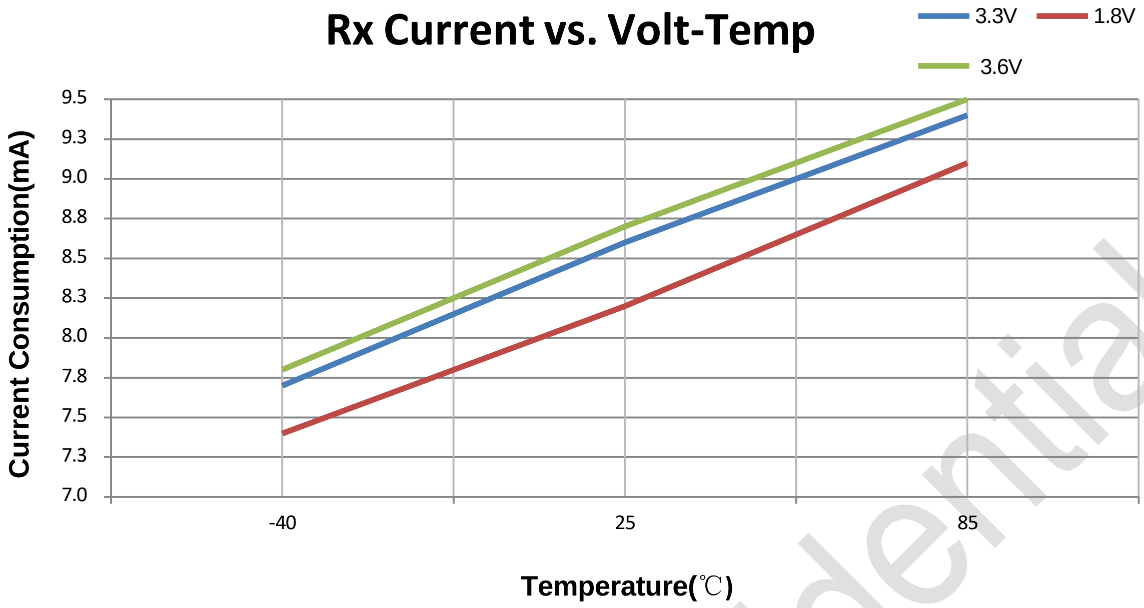


Testing Condition: Freq = 434MHz / 868MHz, Fdev = 10KHz, BR = 10Kbps

1.11.2 Rx Current VS. Voltage Temperature

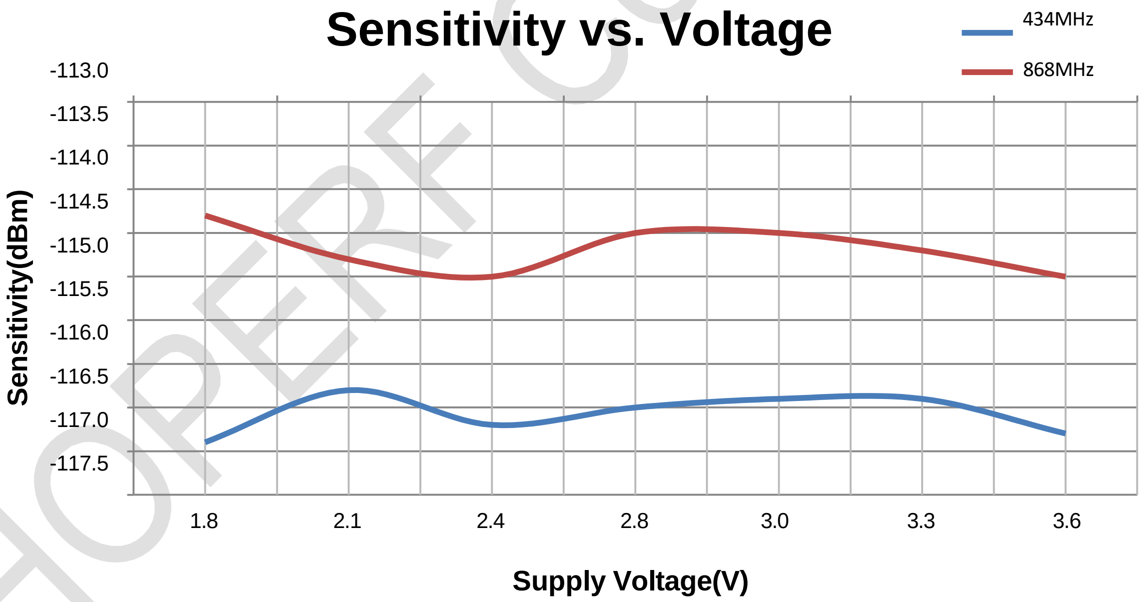


Test Condition: Freq = 434MHz,Fdev = 10KHz, BR = 10Kbps



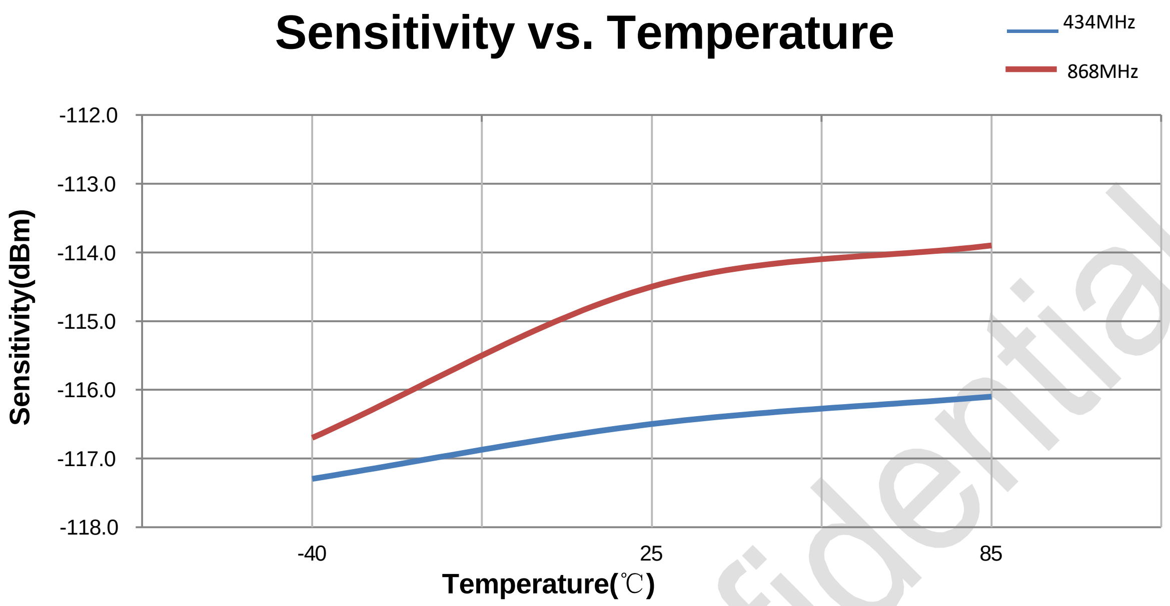
Test Condition: Freq = 868MHz, Fdev = 10KHz, BR = 10Kbps

1.11.3 Sensitivity VS. Voltage



Test Condition: FSK, DEV = 10KHz, BR = 10Kbps

1.11.4 Sensitivity VS. Temperature



Test Condition: FSK, DEV = 10KHz, BR = 10Kbps

2. Pin Descriptions

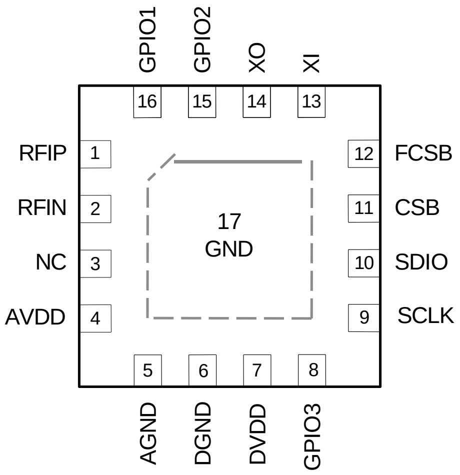
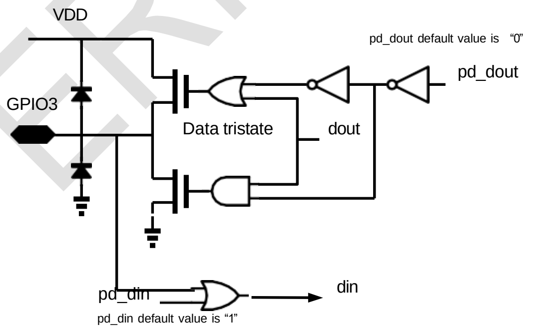
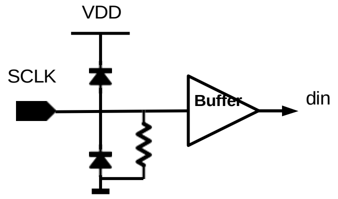
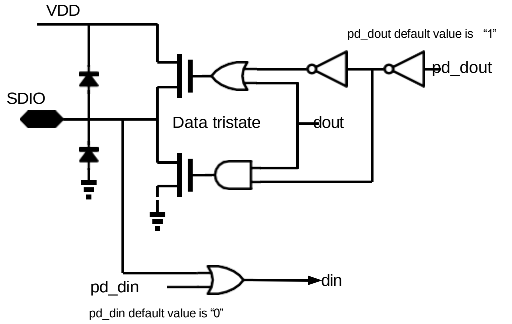
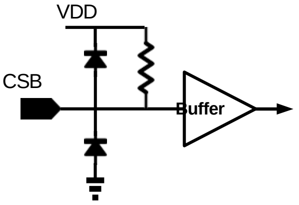
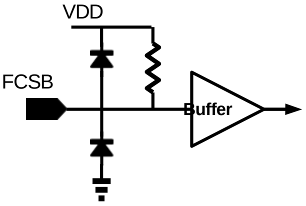
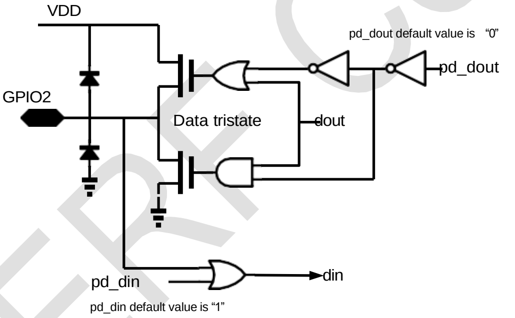
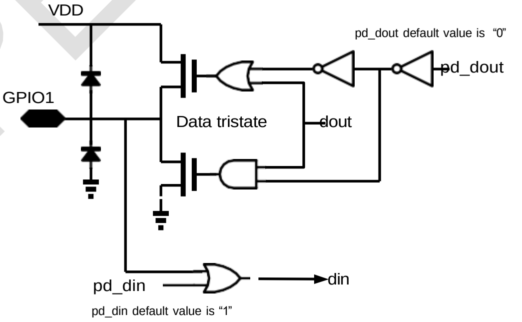


Figure 1. CMT2219B pin arrangements

Table 11. CMT2219B pin descriptions

Pin No.	Name	I/O	Internal IO Schematic	Descriptions
1	RFIP	I		RF signal input P
2	RFIN	I		RF signal input N
3	PA	O		NA
4	AVDD	IO		Analog VDD
5	AGND	IO		Analog GND
6	DGND	IO		Digital GND
7	DVDD	IO		Digital VDD
8[1]	GPIO3	IO		Configured as CLKO, DOUT, INT2, DCLK
9	SCLK	I		SPI clock

10	SDIO	IO		SPI data input and output
11	CSB	I		SPI chip selection bar for register access, active low
12	FCSB	I		SPI chip selection bar for FIFO access, active low
13	XI	I		Crystal circuit input
14	XO	O		Crystal circuit output
15[1]	GPIO2	IO		Configured as INT1, INT2, DOUT, DCLK
16[1]	GPIO1	IO		Configured as DOUT, INT1, INT2, DCLK
17	GND	I		Analog GND. It must be grounded.
Note: [1]. INT1 and INT2 are interrupts. DOUT is demodulated output. DCLK is a demodulation data rate synchronization clock				

3. Typical Application Schematic

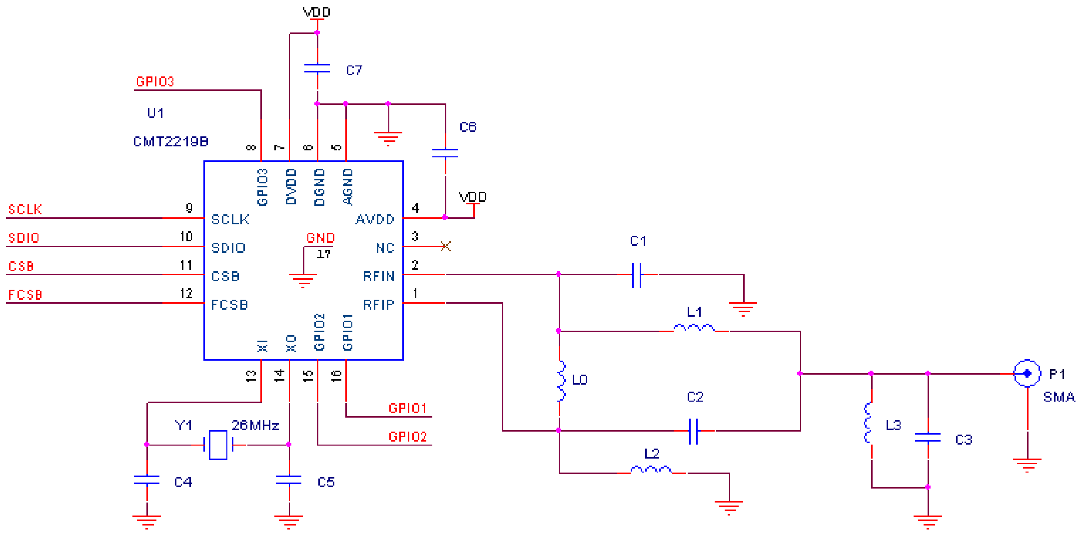


Figure 2. Application schematic diagram

Table 12. Application BOM

No.	Descriptions	Value			Unit	Supplier
		433 MHz	868 MHz	915 MHz		
C1	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C2	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C3	±5%, 0603 NP0, 50 V	4.7	2.2	2.2	pF	
C4	±5%, 0603 NP0, 50 V	24			pF	
C5	±5%, 0603 NP0, 50 V	24			pF	
C6	±5%, 0603 NP0, 50 V	470			pF	
C7	±5%, 0603 NP0, 50 V	0.1			uF	
L0	±5%, 0603 Multilayer chip inductor	68	12	12	nH	Sunlord SDCL
L1	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L2	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
L3	±5%, 0603 Multilayer chip inductor	27	15	12	nH	Sunlord SDCL
Y1	±10 ppm, SMD32*25 mm	26			MHz	EPSON
U1	CMT2219B, Sub-1GHz RF Receiver				-	CMOSTEK

4. Function Descriptions

CMT2219B is an ultra-low power, high performance receiver chip. It supports OOK, (G) FSK and (G) MSK. It is suitable for applications inthe range from 140 to 1020MHz. The product belongs to CMOSTEK NextGenRF^{TM} series. The series includes transmitters, receivers and transceivers and other complete product lines. CMT2219B block diagram is as shown in the following figure.

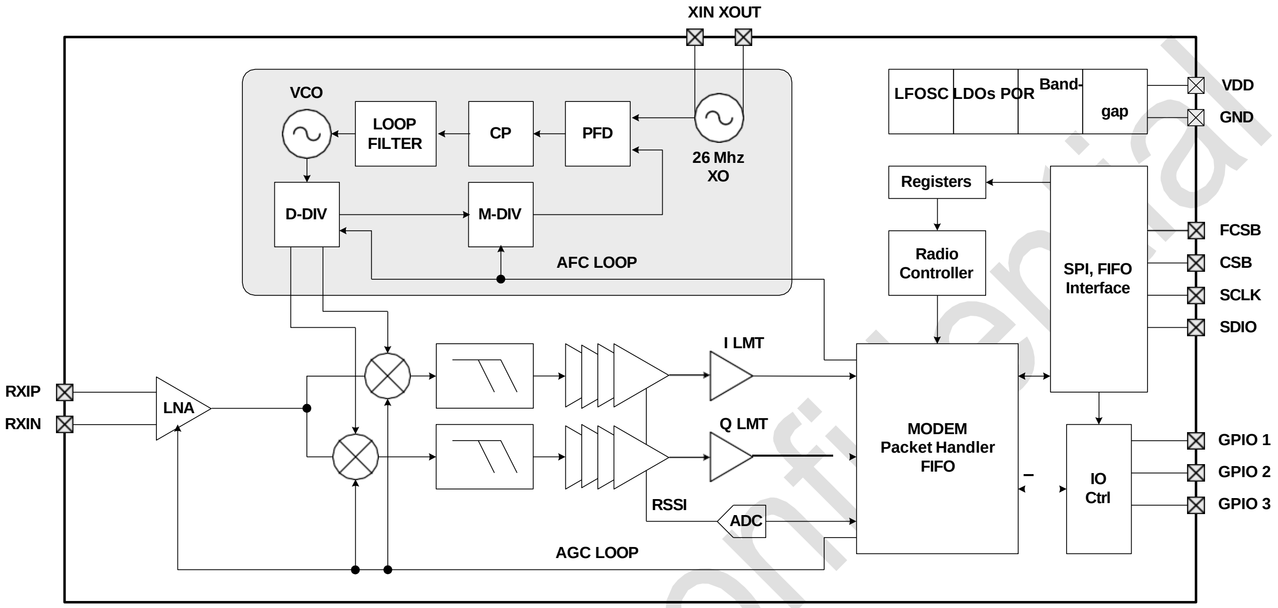


Figure 3. Functional Block Diagram

In the receiver part, the chip uses LNA+MIXER+IFFILTER+LIMITTER+PLL low-IF architecture to achieve the Sub-GHz wireless reception function.

In the receiver system, the analog circuit mixes the RF signal to IF and converts the signal from analog to digital through the Limiter module, then outputs I/Q two single bit signals to the digital circuit for (G) FSK demodulation. At the same time, SARADC will convert the real-time RSSI signal to 8-bit digital signal, and sent them to the digital part for OOK demodulation and other processing. The digital circuit is responsible for mixing the intermediate frequency to zero frequency (Baseband) and performing a series of filtering and decision processing, while AFC and AGC control the analog circuit dynamically, finally the 1-bit original signal is demodulated. After demodulation, the signal will be sent to the decoder to decode and fill in the FIFO, or output to the PAD directly.

The chip provides the SPI communication port. The external MCU can configure the various functions by accessing to the register, control the main state machine, and access to the FIFO.

4.1 Receiver

CMT2219B has a built-in ultra-low power, high performance low-IF OOK, FSK receiver. The RF signal induced by the antenna is amplified by a low noise amplifier, and is converted to an intermediate frequency by an orthogonal mixer. The signal is filtered by the image rejection filter, and is amplified by the limiting amplifier and then sent to the digital domain for digital demodulation. During power on reset (POR) each analog block is calibrated to the internal reference voltage. This allows the chip to remain its best performance at different temperatures and voltages. Baseband filtering and demodulation is done by the digital demodulator. The AGC loop adjust the system gain by the broadband power detector and attenuation network nearby LNA, so as to obtain the best system linearity, selectivity, sensitivity and other performance.

Leveraging CMOSTEK's low power design technology, the receiver consumes only a very low power when it is turned on. The periodic operation mode and wake up function can further reduce the average power consumption of the system in the application with strict requirements of power consumption.

The CMT2219B receiver can operate in direct mode and packet mode. In the direct mode, the demodulator output data can be directly output through the DOUT pin of the chip. DOUT can be assigned to GPIO1/2/3. In the packet mode, the demodulator data output is sent to the data packet handler, get decoded and is filled in the FIFO. MCU can read the FIFO by the SPI interface.

4.2 Auxiliary Blocks

4.2.1 Power-On Reset (POR)

The Power-On Reset circuit detect the change of the VDD power supply, and generate the reset signal for the entire CMT2219B system. After the POR, the MCU must go through the initialization process and re-configure the CMT2219B. There are two circumstances those will lead to the generation of POR.

The first case is a very short and sudden decrease of VDD. The POR triggering condition is, VDD dramatically decreases by 0.9V +/- 20% (e.g. 0.72V – 1.08V) within less than 2 us. To be noticed, it detects a decreasing amplitude of the VDD, not the absolute value of VDD.

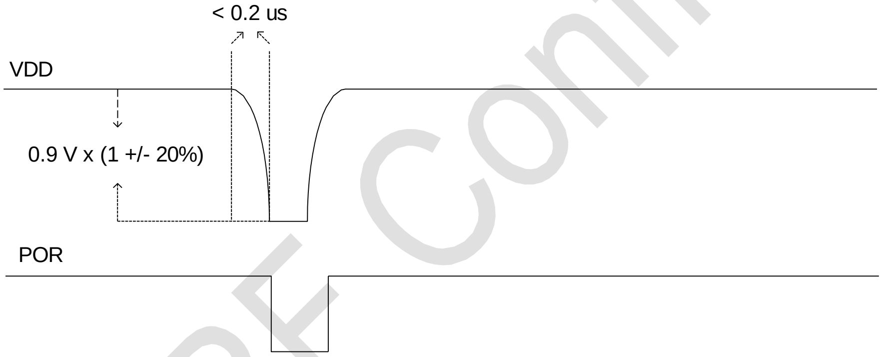


Figure 4. Sudden Decrease of VDD lead to Generation of POR

The second case is, a slow decrease of the VDD. The POR triggering condition is, VDD decreases to 1.45V +/- 20% (e.g. 1.16V – 1.74V) within a time more than or equal to 2 us. To be noticed, it detects an absolute value of VDD, not a decreasing amplitude.

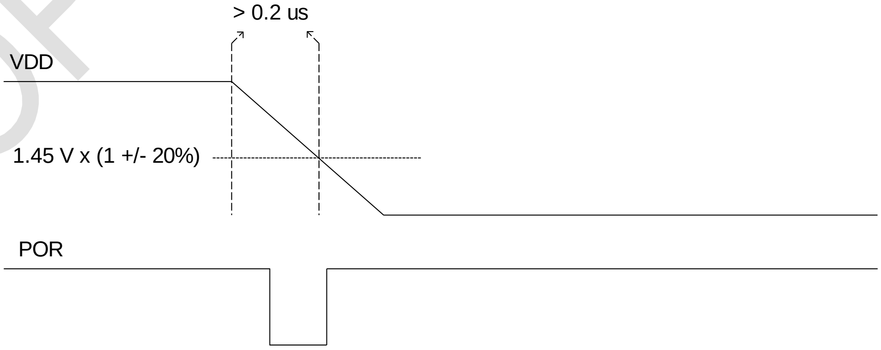


Figure 5. Slow Decrease of VDD lead to Generation of POR

4.2.2 Crystal Oscillator

The crystal oscillator provides a reference clock for the phase locked loop as well as a system clock for the digital circuits. The value of load capacitance depends on the crystal specified CL parameters. The total load capacitance between XI and XO should be equal to CL, in order to make the crystal accurately oscillate at 26 MHz.

$$C_L = \frac{1}{1/C15 + 1/C16} + C_{par} + 2.5pF$$

C15 and C16 are the load capacitance sat both ends of the crystal. Cpar is the parasitic capacitance on the PCB. Each crystal pin has 5pF internal parasitic capacitance, together is equivalent to 2.5pF. The equivalent series resistance of the crystal must be within the specifications so that the crystal can have a reliable vibration. Also, an external signal source can be connected to the XI pin to replace the conventional crystal. The recommended peak value of this clock signal is from 300mV to 700mV. The clock is coupled to XI pin via a blocking capacitor.

4.2.3 Sleep Timer

The CMT2219B integrates a sleep timer driven by 32 kHz low power oscillator (LPOSC). When this function is enabled, the timer wakes the chip from sleep periodically. When the chip operates in a duty cycle mode, the sleep time can be configured from 0.03125 ms to 41922560 ms. Due to the low power oscillator frequency will change with the temperature and voltage drift, it will be automatically calibrated during power on and will be periodically calibrated since then. These calibrations will keep the frequency tolerance of the oscillator within + 1%.

4.2.4 Low Battery Detection

The chip sets up low voltage detection. When the chip is tuned to a certain frequency, the test is performed once. Frequency tuning occurs when the chip jumps from the SLEEP/STBY state to the RFS/RX state. The result can be read by the LBD_VALUE register.

4.2.5 Received Signal Strength Indicator(RSSI)

RSSI is used to evaluate the signal strength inside the channel. The cascaded I/Q logarithmic amplifier amplifies the signal before it is sent to the demodulator. The logarithmic amplifier of I channels and Q channel contains the received signal indicator, in which the DC voltage is generated is proportional to the input signal strength. The output of RSSI is the sum of the values of the two channels' signals. The output has 80dB dynamic range above the sensitivity. After the RSSI output is sampled by the ADC and filtered by a SAR FILTER and a RSSI AVG FILTER. The order of the average filter can be set by RSSI_AVG_MODE<2:0>. The code value is translated into dBm value after filtering. Users can read the register RSSI_CODE<7:0> to obtain the RSSI code value, or RSSI_DBM<7:0> to obtain the dBm value. By setting the register RSSI_DET_SEL<1:0> Users can determine whether the RSSI is output to the MCU in real time, or latched at the instance when the preamble, sync, or the whole packet is received.

Also, CMT2219B allows the user to setup a threshold by RSSI_TRIG_TH<7:0> to compare with the real-time RSSI value. If the RSSI is larger than the threshold it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, ofthe receive time extending condition in the super low power (SLP) mode.

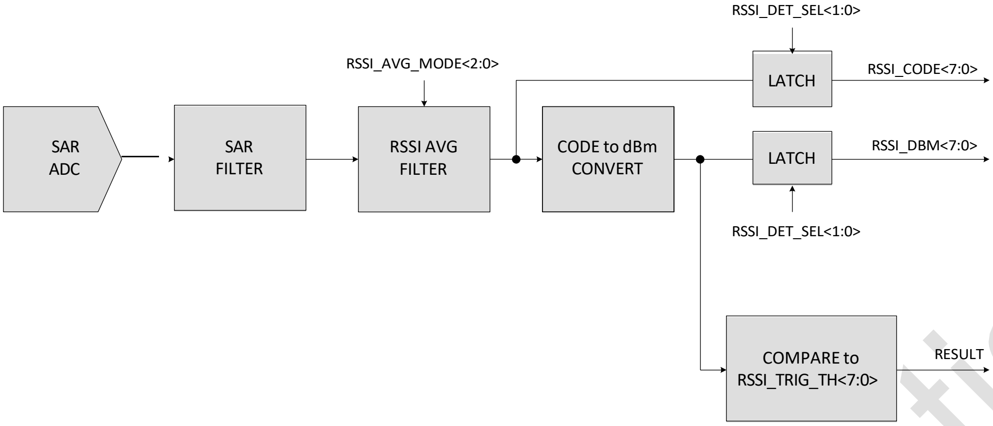


Figure 6. RSSI detection and comparison circuit

CMT2219B has done a certain degree of calibration before delivery. In order to obtain more accurate RSSI measurement results, the user needs to recalibrate the RSSI circuit in their dedicated applications. For further information, please refer to the "AN166-CMT2219BW RSSI Usage Guideline".

4.2.6 Phase Jump Detector（PJD）

PJD is Phase Jump Detector. When the chip is in FSK demodulation, it can automatically observe the phase jump characteristics of the received signal to determine whether it is a wanted signal or an unwanted noise.

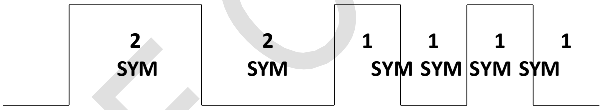


Figure 7. Received signal jump diagram

The PJD mechanism defines that the input signal switching from 0 to 1 or from 1 to 0 is a phase jump. Users can configure the PJD_WIN_SEL<1:0> to determine the number of detected jumps for the PJD to identify a wanted signal. As shown in the above figure, in total 8 symbols are received. But the phase jump only appeared 6 times. Therefore, the number of jumps is not equal to the number of symbols. Only when a preamble is received they are equal. In general, the more jumps are used to identify the signal, the more reliable they result is; the less jumps are used, the faster the result is obtained. If the RX time is set to a relatively short period, it is necessary to reduce the number of jumps to meet the timing requirements. Normally, 4 jumps allow pretty reliable result, e.g. the chip will not mistakenly treat an incoming noise as a wanted signal, and vice versa will not treat a wanted signal as noise.

Detecting the phase jump of a signal, is identical to detect whether the signal has the expected data rate. In fact, at the same time, the PJD will also detect the FSK deviation and see if it is legal, as well as to see if the SNR is over 7 dB. With these three parameters the PJD is able to make a very reliable judgment. If the signal is wanted it outputs logic 1, otherwise outputs logic 0. The output can be used as a source of the RSSI VLD interrupt, or the receive time extending condition in the super low power (SLP) mode. In direct data mode, by setting the DOUT_MUTE register bit to 1, the PJD can mute the FSK demodulated data output while there is not wanted signal received.

The PJD technique is similar to the traditional carrier sense technique, but more reliable. While users combine the RSSI detection and PJD technique, they can precisely identify the status of the current channel.

4.2.7 Automatic Frequency Control (AFC)

The AFC mechanism allows the receiver to minimize the frequency error between the TX and RX in a very short time once a wanted signal comes in. This helps the receiver to maintain its highest sensitivity performance. CMT2219B has the most advanced AFC technology. Compare with the other competitors, within the same bandwidth, CMT2219B can identify larger frequency error, and remove the error in a much shorter time (8-10 symbols).

Normally the frequency error between the TX and RX is caused by the crystal oscillators used in both sides. CMT2219B allows the user to fill in the value of crystal tolerance (in PPM) on RFPDK. Based on the crystal tolerance, the RFPDK will calculate the AFC range while minimizing the receiver bandwidth (to maintain the best performance). Due to the excellent performance of the AFC, it provides a good solution to the crystal aging problem which would lead to more frequency error as time goes by. Therefore, compare to other similar receiver chips, CMT2219B can solve more severe crystal aging problem and effectively extend the life time of the product.

4.2.8 Clock Data Recovery (CDR)

The basic task of a CDR system is to recover the clock signal that is synchronized with the symbol rate, while receiving the data. Not only for decoding inside the chip, but also for outputting the synchronized clock to GPIO for users to sample the data.So CDR's task is simple and important. If the recovered clock frequency is in error with the actual symbol rate, it will cause data acquisition errors at the time of reception.

CMT2219BW has designed three types of CDR systems, as follows:

1. **COUNTING system**–The system is designed for the symbol rates to be more accurate. If the symbol rate is 100% aligned, the unlimited length of 0 can be received continuously without error.

2. **TRACING system** –The system is designed to correct the symbol rate error. It has the tracking function. It can automatically detect the symbol rate transmitted by TX, and adjust quickly the local symbol rate of RX at the same time, so as to minimize the error between them. The system can withstand up to 15.6% or symbol rate error. Other similar products in the industry cannot reach this level.

3. **MANCHESTER system** –This system evolves from the COUNTING system. The basic feature is the same. The only difference is that the system is specially designed for Manchester codec. Special processing can be done when the TX symbol rate has unexpected changes.

4.2.9 Fast Frequency Hopping

The mechanism of fast frequency hopping is, based on the frequency configured on the RFPDFK, for instance 433.92 MHz, during applications the MCU can simply change 1 or 2 registers to quickly switch to another frequency channel. This simplifies the way of change the RX frequency in multiple channels application.

In general, the user can configure FH_OFFSET<7:0>during the chip initialization process. And then in the application, the user can switch the channel by changing FH_CHANNEL<7:0>.

When users need to use the fast frequency hopping, in some particular frequency points, one parameter of the AFC circuit must be re-configured. Please refer to “AN197-CMT2300A-CMT2119B-CMT2219B fast frequency hopping” and “CMT2300A-CMT2219B frequency hopping calculation tool” for more details.

5. Chip Operation

5.1 SPI Interface

The chip communicates with the outside through the 4-wire SPI interface. The CSB is the active-low chip select signal for accessing to the registers. The FCSB is the active-low select signal for accessing to the FIFO. They cannot be set to low at the same time. The SCLK is the serial clock. Its highest speed is 5MHz. The chip itself and the external MCU send the data at the falling edge of SCLK and capture the data at the rising edge of SCLK. The SDA is a bidirectional pin for input and output data. The address and data are transferred starting from the MSB.

When accessing to the registers, CSB is pulled low. A R/W bit is sent first, followed by a 7-bit register address. After the external MCU pulls down the CSB, it must wait for at least half a SCLK cycle, and then send the R/W bit. After the MCU sends out the last falling edge of SCLK, it must wait for at least half a SCLK cycle, and then pull the CSB high.

To be noticed, when reading a register, MCU and CMT2219B will have to switch the direction of their IO (SDIO) between the address bit 0 and the data bit 7. It is required that the MCU switches the IO to input mode before send out the falling edge of the SCLK; CMT2219B should switch the IO to output mode after it has seen the falling edge of the SCLK. This avoids data contention of the SDIO (both of the MCU and CMT2219B set the SDIO to output mode at the same time), which would cause unexpected electrical problem.

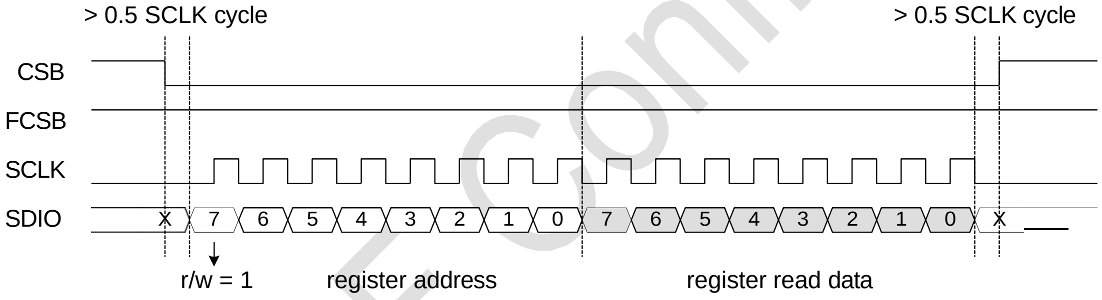


Figure 8. SPI read register timing

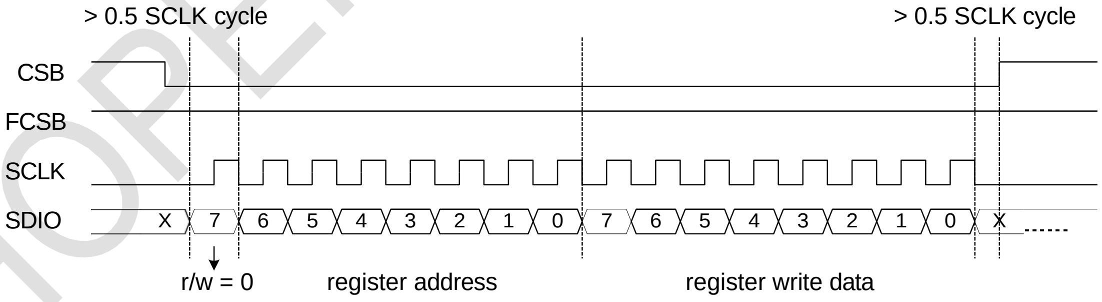


Figure 9. SPI write register timing

5.2 FIFO

The FIFO size can be set to 32-byte or 64-byte. It is used to store the received data. The FIFO can be accessed via the SPI interface. The user can clear FIFO by setting FIFO_CLR_RX to 1.

5.2.1 FIFO Read Operation

When the MCU accesses to the FIFO, the user must first configure a few registers to set the FIFO mode. The details are introduced in the "AN167-CMT2219B FIFO and Data Packet Usage Guideline". Here is the read timing diagram. Note that there is a slight difference in the control of the FCSB for reading the FIFO and the control of the CSB for accessing the register. When the MCU starts to access to the FIFO, FCSB must be pulled down 1-clock cycle at first, and then send the rising edge of SCL. After the last falling edge of SCL is sent, the MCU must wait at least 2 us to pull up the FCSB. Between the adjacent read operations, the FCSB must be pulled high for 4us at least.

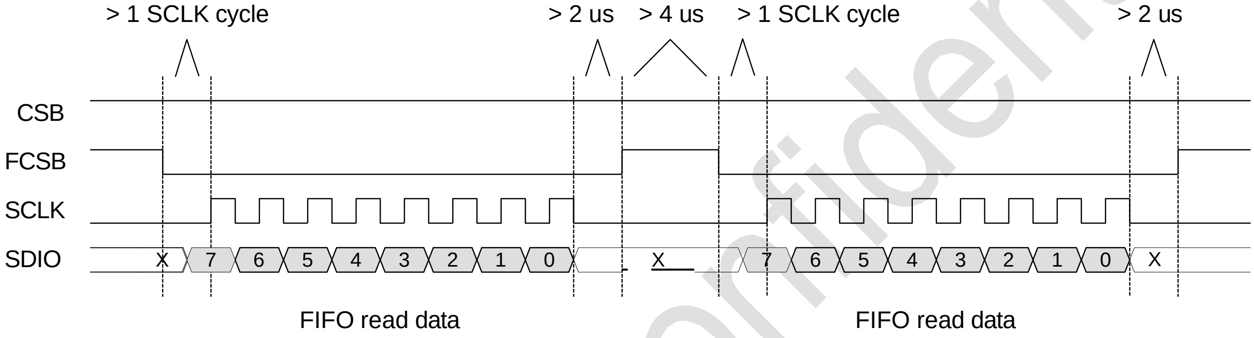


Figure 10. SPI read FIFO timing

5.2.2 FIFO Associated Interrupt

CMT2219B provides rich interrupt sources associated with the FIFO. The interrupt timing for the Rx FIFO is shown below:

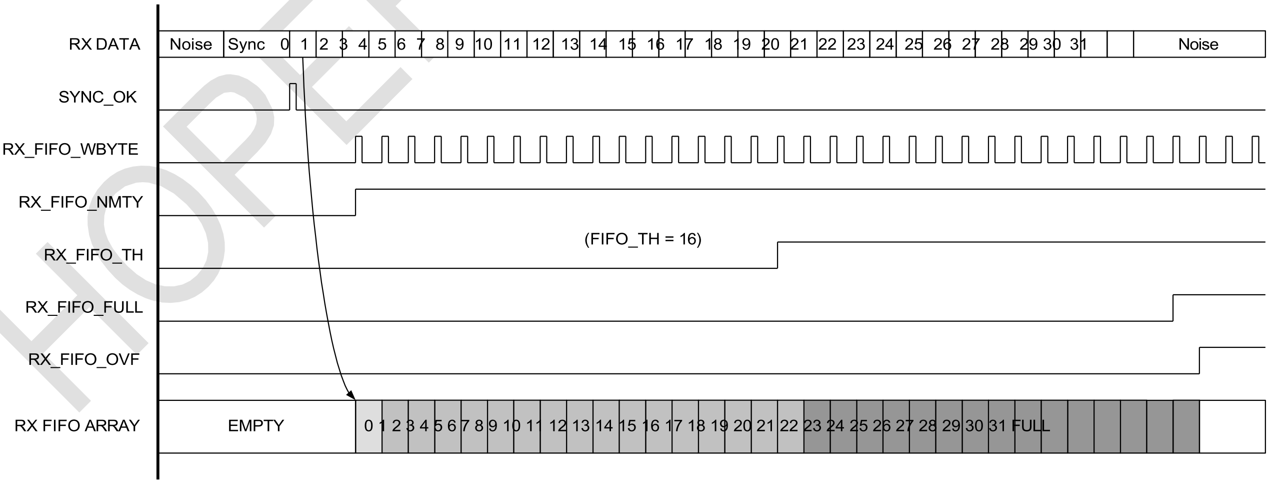


Figure 11. CMT2219B RX FIFO interrupt timing diagram

5.3 Operation State, Timing and Power Consumption

5.3.1 Startup Timing

After the chip VDD is powered up, the chip usually needs to wait about 1ms, then POR will release. After the release of the POR, the crystal will start, the start time is 200 us - 1 ms, depending on the characteristics of the crystal itself. After starting, the user need to wait for the crystal settled, then the system starts working. The default setting is 2.48ms. This time can be modified by writing XTAL_STB_TIME <2:0> afterword (it has to be longer than the crystal inherent settling time). However, if the inherent settling time of the crystal is difficult to observed by the user, the default setting of 2.48 ms is recommended and is able to cover most of the crystals.

The chip remains in the IDLE status until the crystal is settled. After the crystal is settled, the chip will leave the IDLE state and begin to do the calibration of each module. After the calibration is completed, the chip will stay in the SLEEP and wait until the user to initialize the configuration. At any time, as long as the soft reset is performed, the chip will go back to the IDLE and be powered up again.

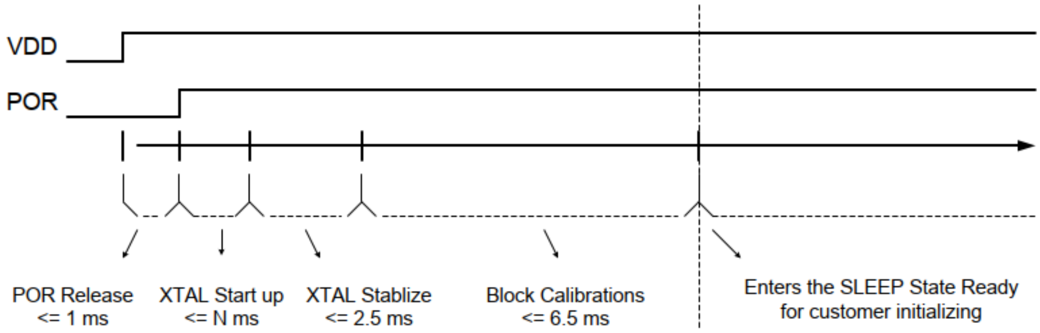


Figure 12. Power on sequence

When the calibration is completed, the chip enters the SLEEP mode. From this time, the MCU can switch the chip to different operating states by setting the register CHIP_MODE_SWT<7:0>.

5.3.2 OperationState

CMT2219B has 5 operation states: IDLE, SLEEP, STBY, RFS and RX, as shown below.

Table 13. CMT2219B state and module open table

State	Binary code	Switch command	Active Blocks	Optional Blocks
IDLE	0000	soft_rst	SPI, POR	None
SLEEP	0001	go_sleep	SPI, POR, FIFO	LFOSC, Sleep Timer
STBY	0010	go_stby	SPI, POR, XTAL, FIFO	CLKO
RFS	0011	go_rfs	SPI, POR, XTAL, PLL, FIFO	CLKO
RX	0101	go_rx	SPI, POR, XTAL, PLL, LNA+MIXER+IF, FIFO	CLKO, RX Timer

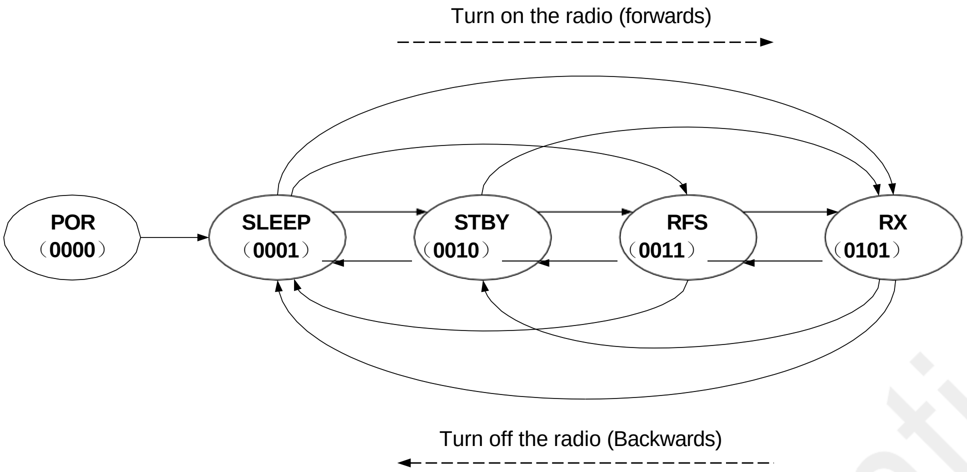


Figure 13. State Switch Diagram

■ SLEEP State

The chip power consumption is the lowest in SLEEP state, and almost all the modules are turned off. SPI is open, the registers of the configuration bank and control bank 1 will be saved, and the contents filled in the FIFO before will remain unchanged. However, the user cannot operate the FIFO and cannot change the contents of the register. If the user opens the wake-up function, the LFOSC and the sleep counter will turn on and start working. The time required to switch from IDLE to SLEEP is the power up time. Switch from other state to SLEEP will be completed immediately.

■ STBY State

In STBY state, the crystal is turned on, the LDO of the digital circuit will also be turned on, the current will be slightly increased, and the FIFO can be operated. The user can choose whether to output CLKO (system clock) to PIN. Because the crystal and LDO is turned on, compared to the SLEEP, the time switching from the STBY to RX will be relatively short. Switching from SLEEP to STBY will be completed after the crystal is turned on and settled. Switching from other state to STBY will be completed immediately.

■ RFS State

RFS is a transition state before switching to RX. Except that the receiver RF module is off, the other modules are turned on, and the current will be larger than STBY. Switching from STBY to RFS probably requires PLL calibration and stability time of 350us. Switching from SLEEP to RFS needs to add the crystal start-up and stability time. Switching from other state to RFS will be completed immediately.

■ RX State

All modules on the receiver will be opened in RX state. Switching from RFS to RX requires only 20us. Switching from STBY to RX needs to add the PLL calibration and settled time of 350 us. Switching from SLEEP to RX needs to add the crystal start-up and settled time.

5.4 GPIO and Interrupt

CMT2219B has 3 GPIO ports. Each GPIO can be configured as a different input or output. CMT2219B has 2 interrupt ports. They can be configured to different GPIO outputs.

Table 14. CMT2219B GPIO

Pin No.	Name	I/O	Function
16	GPIO1	IO	Configured as:DOUT, INT1, INT2, DCLK
15	GPIO2	IO	Configured as:INT1, INT2, DOUT, DCLK
8	GPIO3	IO	Configured as:CLKO, DOUT, INT2, DCLK

Interrupt mapping table is as below. INT1 and INT2 mapping is the same. Take INT1 as an example.

Table 15. CMT2219B interrupt mapping table

Name	INT1_SEL	Descriptions	Clearing methods
RX_ACTIVE	00000	Indicates the chip is entering RX and is already in RX. It is 1 in PLL Tuning and RX state, and it is 0 in the other states.	Auto
RSSI_VLD	00010	Indicates whether the RSSI is active.	Auto
PREAM_OK	00011	Indicates that the Preamble is received successfully.	by MCU
SYNC_OK	00100	Indicates that the Sync Word is received successfully.	by MCU
NODE_OK	00101	Indicates that the Node ID is received successfully.	by MCU
CRC_OK	00110	Indicates that the CRC for the current packet is correct.	by MCU
PKT_OK	00111	Indicates that a packet has been received.	by MCU
SL_TMO	01000	Indicates that the SLEEP counter timed out.	by MCU
RX_TMO	01001	Indicates that the RX counter timed out.	by MCU
RX_FIFO_NMTY	01011	Indicates that the RX FIFO is not empty.	Auto
RX_FIFO_TH	01100	Indicates the number of unread bytes of the RX FIFO is over FIFO TH	Auto
RX_FIFO_FULL	01101	Indicates RX FIFO is full.	Auto
RX_FIFO_WBYTE	01110	Indicates each time a byte is written to the RX FIFO. Itis a pulse.	Auto
RX_FIFO_OVF	01111	indicates RX FIFO is overflow	Auto
STATE_IS_STBY	10011	Indicates that the current state is STBY.	Auto
STATE_IS_FS	10100	Indicates that the current state is RFS.	Auto
STATE_IS_RX	10101	Indicates that the current state is RX.	Auto
LBD	10111	Indicates that low battery is detected (VDD is lower than TH)	Auto
PKT_DONE	11001	Indicates that the current packet has been received, covering 4 possible different situations. 1. The packet is received completely and correctly. 2. Manchester decoding has error. Decoder is automatically reset. 3. NODE ID receiving has error. Decoder is automatically reset. 4. Signal collision occurred. Decoder is not reset, waiting for MCU to response.	by MCU

By default, Interrupt is active high (logic 1 is valid). Users can set the INT_POLAR register bit to 1 to make all interrupts active low (logic 0 is valid).Taking INT1 as an example, the control and sources selection of all the available interrupts is shown below. The control and mapping of INT1 and INT2 are the same.

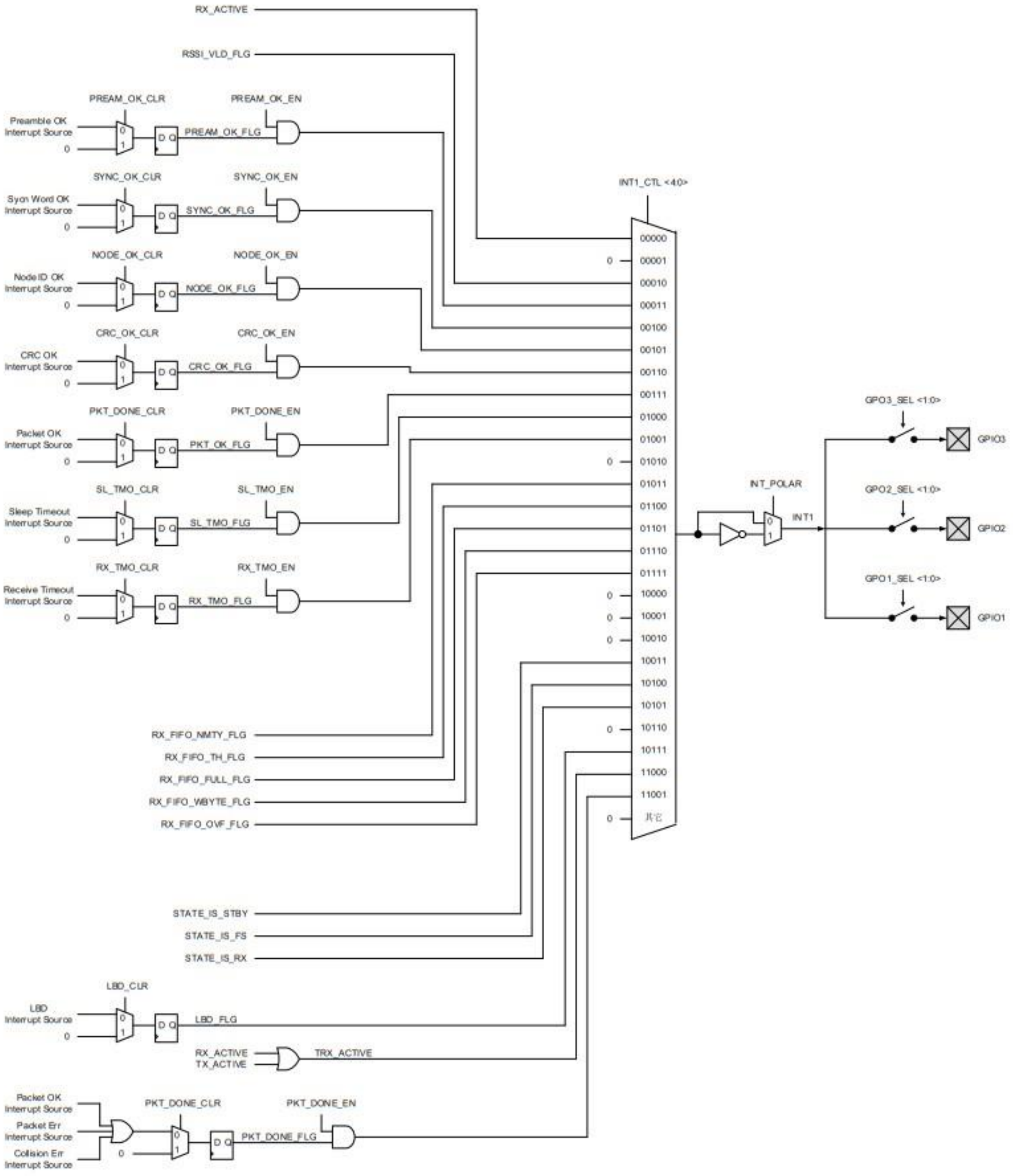


Figure 14. CMT2219B INT1 interrupt mapping diagram

6. Packet Handler

CMT2219B supports direct mode and packet mode:

- Direct Mode – Only supports preamble and sync detection, FIFO does not work, demodulated data sent out from GPIO.
- Packet Mode – Supports all packet formats, demodulated data is stored in FIFO, accessed by SPI.

6.1 Direct Mode

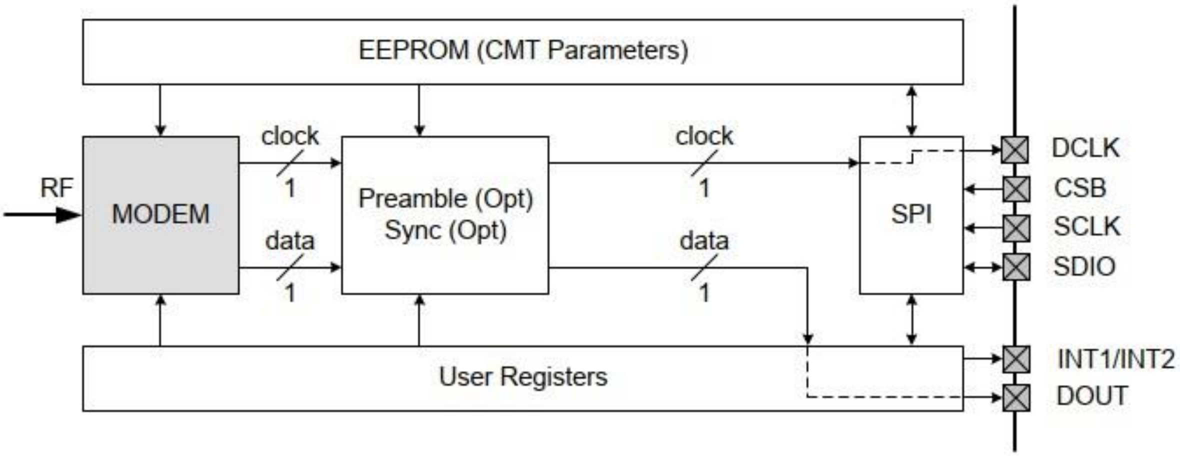


Figure 15. Direct mode data path

In direct mode, the data from the demodulator is sent directly to the external MCU via the DOUT pin. DOUT can be set to GPIO1, 2 or 3.The typical RX direct mode control sequence for the MCU is:

1. Configures GPIOsusing theCUS_IO_SEL register.
2. Configures DATA_MODE = 0.
3. Send thego_rx command.
4. Capture the data from DOUT continuously.
5. Send thego_sleep/go_stby/go_rfs command to stop receiving and save the power.

6.2 Packet Mode

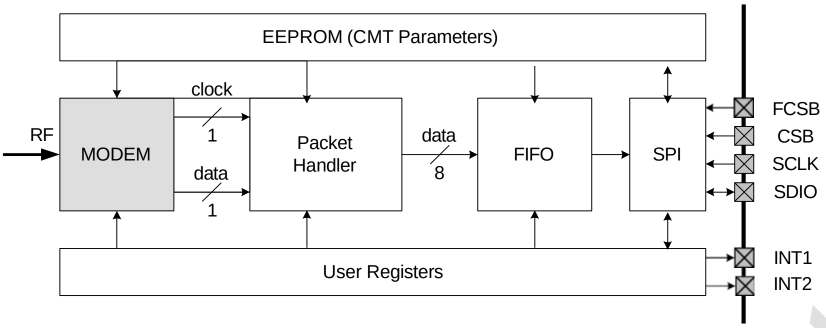


Figure 16. Packet mode data path

The packet handler supports variable packet format (Length in front of the Node ID), variable packet format (Length in the back of the Node ID) and fixed packet format. Each element in the packet supports flexible configurations, as shown below.

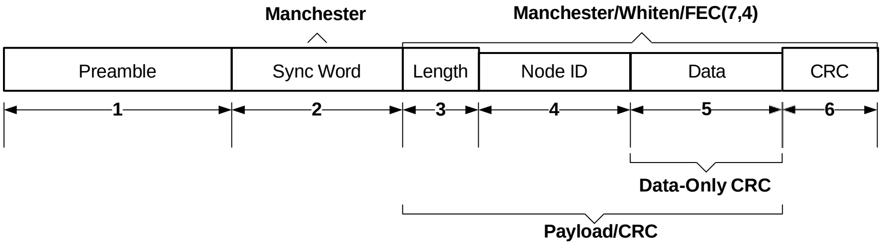


Figure 17. Variable length packet (Length in front of Node ID)

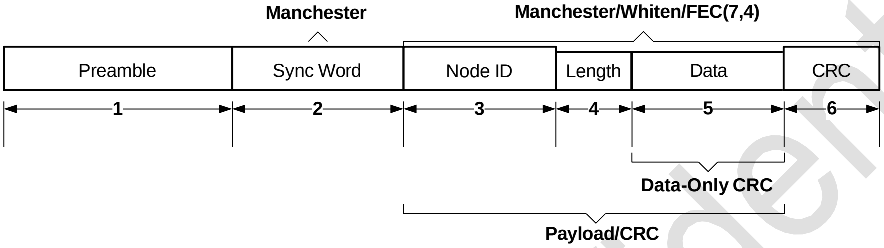


Figure 18. Variable length packet (Length behind Node ID)

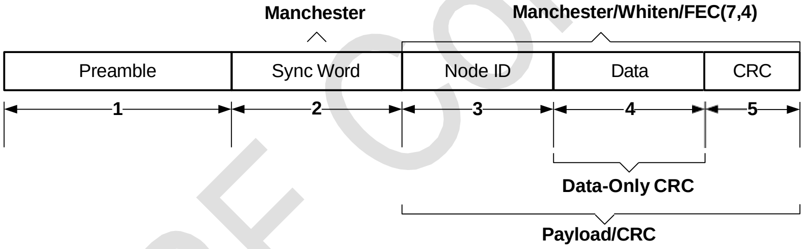


Figure 19. Fixed length packet

In the packet mode, the output data from the demodulator will be transferred to the packet handler for decoding, and then filled in the FIFO. The packet handler provides a variety of decoding mechanisms and options to determine the validity of the data. These can reduce the work load of the MCU. The typical package mode control sequence for the MCU is:

1. Configures GPIO using the CUS_IO_SEL register.
2. Setup the interrupts usingCUS_INT1_CTL, CUS_INT2_CTL and CUS_INT_EN registers.
3. Send thego_rx command.
4. Reads the RX FIFO according to the relevant interrupts.
5. Sends the go_sleep/go_stby/go_rfs command to stop the receiving and save the power.
6. Clears the packet interrupts using CUS_ INT_CLR1 and CUS_INT_CLR2 registers.

CMT2219B has rich configurable hardware resources of FIFO, packet and their interrupts, which makes it compatible with most of the similar RF products in the market. For more details please refer to the interface of RFPDK and “AN167-CMT2219B FIFO and Data Packet Usage Guideline”.

7. Low Power Operation

7.1 Duty CycleOperation Mode

CMT2219B makes the Rx work in duty cycle operation mode to save the power consumption. Among them, the Rx Duty Cycle can be classified into the following 5 modes.

1. Fully manual control
2. Automatic SLEEP wakeup, switch to manual control
3. Automatic SLEEP wakeup, automatically enter to RX, manually exit RX
4. Automatic SLEEP wakeup, manually enter RX, automatically exit RX
5. Fully automatic receive and sleep control

7.2 Supper Low Power (SLP) Receive Mode

CMT2219B provides a set of options to help users achieve supper low power consumption (SLP - Supper Low Power) reception under different application requirements. These options can be used when setting RX_TIMER_EN to 1, e.g. when the Rx timer is enabled. The principle of the SLP mechanism is to shorten the Rx time when there is no wanted signal coming in, and properly extend the Rx time when there is wanted signal detected, so that the power consumption is minimized while the stability of reception is guaranteed.

The traditional short-range wireless receiver generally uses the following basic scheme to achieve low power communication. CMT2219B is also compatible with this scheme, and expands it to 13 more power-saving schemes. The figure below introduces the most basic scheme, which will be enabled when the RX_EXTEND_MODE<3:0> is set to 0.

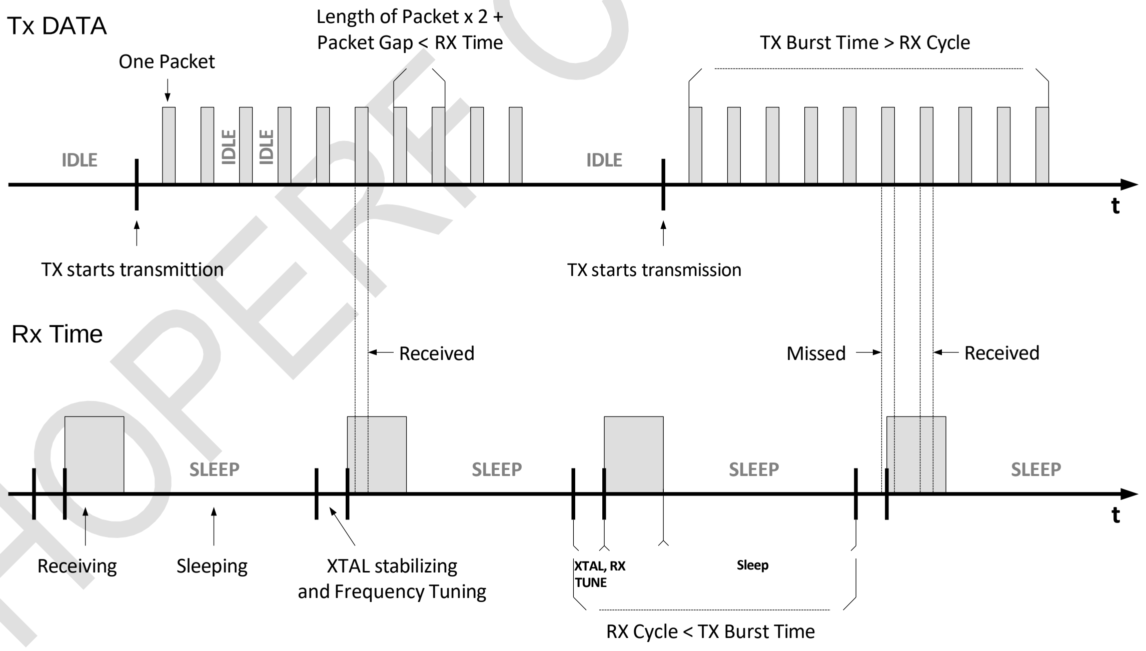


Figure 20. Basic low-power receiver scheme

The traditional low-power communication scheme and the 13-extended low-power schemes are listed in the following table.

Table 16. Low-power receiver mode

No.	Rx Extended Methods	Rx Extended Condition
0	No Rx extension is supported. Exit Rx state as soon as T1 timed out.	None
1	Once meet the Rx extended condition during T1, leave T1 and pass the control authority to MCU.	RSSI_VLD is valid.
2		PREAM_OK is valid.
3		RSSI_VLD and PREAM_OK are valid simultaneously.
4	Once detect RSSI_VLD = 1 during T1, leave T1 and stays in Rx state, exit Rx state until RSSI_VLD = 0.	RSSI_VLD is valid.
5	Once meet the Rx extended condition during T1, switch to T2. Exit Rx as soon as T2 timed out.	RSSI_VLD is valid
6		PREAM_OK is valid
7		RSSI_VLDandPREAM_OK are valid simultaneously.
8		Any one of PREAM_OK or SYNC_OK is valid.
9		Any one of PREAM_OK or NODE_OK is valid.
10		Any one of PREAM_OK or SYNC_OK or NODE_OK is valid.
11	Once meet the Rx extended condition during T1, switch to T2. Leave T2 and pass the control authority to MCU as soon as SYNC is detected, otherwise exit Rx when T2 timed out.	RSSI_VLD is valid.
12		PREAM_OK is valid.
13		RSSI_VLD and PREAM_OK are valid simultaneously.

The T1 and T2 mentioned in the table refer to the RX T1 and the RX T2 time interval that can be set via the registers or RFPDK. The source of RSSI_VLD can be the comparison result of the RSSI or the detection result of the phase jump detector (PJD). For more details, please refer to "AN164-CMT2219BW Low Power Mode Usage Guideline".

7.3 Receiver "Power VS Performance" Configuration

CMT2219B provides a set of registers to select the power consumption and sensitivity performance of the RF frontend circuit. The below table shows how they are configured:

Table 17. Low-power receiver mode

Current Level	RF Performance Level	LMT_VTR<1:0>	MIXER_BIAS<1:0>	LNA_MODE<1:0>	LNA_BIAS<1:0>
Low	Low	2	2	1	1
Medium	Medium	2	2	1	2
High	High	1	2	3	2

8. User Register

CMT2219B is configured by writing in the registers. The following is the register table.

Table 18. CMT2219B Register Table

<table>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x00</td><td>RW</td><td>CUS_CMT1</td><td colspan="8" rowspan="12">User does not need to understand the details, just directly export the register contents from the RFPDK</td><td rowspan="12">CMT Bank</td></tr>
<tr><td>0x01</td><td>RW</td><td>CUS_CMT2</td></tr>
<tr><td>0x02</td><td>RW</td><td>CUS_CMT3</td></tr>
<tr><td>0x03</td><td>RW</td><td>CUS_CMT4</td></tr>
<tr><td>0x04</td><td>RW</td><td>CUS_CMT5</td></tr>
<tr><td>0x05</td><td>RW</td><td>CUS_CMT6</td></tr>
<tr><td>0x06</td><td>RW</td><td>CUS_CMT7</td></tr>
<tr><td>0x07</td><td>RW</td><td>CUS_CMT8</td></tr>
<tr><td>0x08</td><td>RW</td><td>CUS_CMT9</td></tr>
<tr><td>0x09</td><td>RW</td><td>CUS_CMT10</td></tr>
<tr><td>0x0A</td><td>RW</td><td>CUS_CMT11</td></tr>
<tr><td>0x0B</td><td>RW</td><td>CUS_RSSI</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x0C</td><td>RW</td><td>CUS_SYS1</td><td colspan="2">LMT_VTR [1:0]</td><td colspan="2">MIXER_BIAS [1:0]</td><td colspan="2">LNA_MODE [1:0]</td><td colspan="2">LNA_BIAS [1:0]</td><td rowspan="12">System Bank</td></tr>
<tr><td>0x0D</td><td>RW</td><td>CUS_SYS2</td><td>LFOSC_RECAL_EN</td><td>LFOSC_CAL1_EN</td><td>LFOSC_CAL2_EN</td><td>RX_TIMER_EN</td><td>SLEEP_TIMER_EN</td><td>RESV</td><td>RX_DC_EN</td><td>DC_PAUSE</td></tr>
<tr><td>0x0E</td><td>RW</td><td>CUS_SYS3</td><td>SLEEP_BYPASS_EN</td><td colspan="3">XTAL_STB_TIME [2:0]</td><td colspan="2">RESV [1:0]</td><td colspan="2">RX_EXIT_STATE [1:0]</td></tr>
<tr><td>0x0F</td><td>RW</td><td>CUS_SYS4</td><td colspan="8">SLEEP_TIMER_M [7:0]</td></tr>
<tr><td>0x10</td><td>RW</td><td>CUS_SYS5</td><td></td><td colspan="3">SLEEP_TIMER_M [10:8]</td><td colspan="4">SLEEP_TIMER_R [3:0]</td></tr>
<tr><td>0x11</td><td>RW</td><td>CUS_SYS6</td><td colspan="8">RX_TIMER_T1_M [7:0]</td></tr>
<tr><td>0x12</td><td>RW</td><td>CUS_SYS7</td><td></td><td colspan="3">RX_TIMER_T1_M [10:8]</td><td colspan="4">RX_TIMER_T1_R [3:0]</td></tr>
<tr><td>0x13</td><td>RW</td><td>CUS_SYS8</td><td colspan="8">RX_TIMER_T2_M [7:0]</td></tr>
<tr><td>0x14</td><td>RW</td><td>CUS_SYS9</td><td></td><td colspan="3">RX_TIMER_T2_M [10:8]</td><td colspan="4">RX_TIMER_T2_R [3:0]</td></tr>
<tr><td>0x15</td><td>RW</td><td>CUS_SYS10</td><td>COL_DET_EN</td><td>COL_OFS_SEL</td><td>RX_AUTO_EXIT_DIS</td><td>DOUT_MUTE</td><td colspan="4">RX_EXTEND_MODE [3:0]</td></tr>
<tr><td>0x16</td><td>RW</td><td>CUS_SYS11</td><td>PJD_TH_SEL</td><td colspan="2">CCA_INT_SEL [1:0]</td><td colspan="2">RSSI_DET_SEL [1:0]</td><td colspan="3">RSSI_AVG_MODE [2:0]</td></tr>
<tr><td>0x17</td><td>RW</td><td>CUS_SYS12</td><td colspan="2">PJD_WIN_SEL [1:0]</td><td colspan="6">RESV [5:0]</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x18</td><td>RW</td><td>CUS_RF1</td><td colspan="8" rowspan="8">User does not need to understand the details, just directly export the register contents from the RFPDK</td><td rowspan="8">Frequency Bank</td></tr>
<tr><td>0x19</td><td>RW</td><td>CUS_RF2</td></tr>
<tr><td>0x1A</td><td>RW</td><td>CUS_RF3</td></tr>
<tr><td>0x1B</td><td>RW</td><td>CUS_RF4</td></tr>
<tr><td>0x1C</td><td>RW</td><td>CUS_RF5</td></tr>
<tr><td>0x1D</td><td>RW</td><td>CUS_RF6</td></tr>
<tr><td>0x1E</td><td>RW</td><td>CUS_RF7</td></tr>
<tr><td>0x1F</td><td>RW</td><td>CUS_RF8</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x20</td><td>RW</td><td>CUS_RF9</td><td colspan="8" rowspan="24">User does not need to understand the details, just directly export the register contents from the RFPDK</td><td rowspan="24">Data Rate Bank</td></tr>
<tr><td>0x21</td><td>RW</td><td>CUS_RF10</td></tr>
<tr><td>0x22</td><td>RW</td><td>CUS_RF11</td></tr>
<tr><td>0x23</td><td>RW</td><td>CUS_RF12</td></tr>
<tr><td>0x24</td><td>RW</td><td>CUS_FSK1</td></tr>
<tr><td>0x25</td><td>RW</td><td>CUS_FSK2</td></tr>
<tr><td>0x26</td><td>RW</td><td>CUS_FSK3</td></tr>
<tr><td>0x27</td><td>RW</td><td>CUS_FSK4</td></tr>
<tr><td>0x28</td><td>RW</td><td>CUS_FSK5</td></tr>
<tr><td>0x29</td><td>RW</td><td>CUS_FSK6</td></tr>
<tr><td>0x2A</td><td>RW</td><td>CUS_FSK7</td></tr>
<tr><td>0x2B</td><td>RW</td><td>CUS_CDR1</td></tr>
<tr><td>0x2C</td><td>RW</td><td>CUS_CDR2</td></tr>
<tr><td>0x2D</td><td>RW</td><td>CUS_CDR3</td></tr>
<tr><td>0x2E</td><td>RW</td><td>CUS_CDR4</td></tr>
<tr><td>0x2F</td><td>RW</td><td>CUS_AGC1</td></tr>
<tr><td>0x30</td><td>RW</td><td>CUS_AGC2</td></tr>
<tr><td>0x31</td><td>RW</td><td>CUS_AGC3</td></tr>
<tr><td>0x32</td><td>RW</td><td>CUS_AGC4</td></tr>
<tr><td>0x33</td><td>RW</td><td>CUS_OOK1</td></tr>
<tr><td>0x34</td><td>RW</td><td>CUS_OOK2</td></tr>
<tr><td>0x35</td><td>RW</td><td>CUS_OOK3</td></tr>
<tr><td>0x36</td><td>RW</td><td>CUS_OOK4</td></tr>
<tr><td>0x37</td><td>RW</td><td>CUS_OOK5</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x38</td><td>RW</td><td>CUS_PKT1</td><td colspan="5">RX_PREAM_SIZE [4:0]</td><td>PREAM_LENG_UNIT</td><td colspan="2">DATA_MODE [1:0]</td><td rowspan="29">Baseband Bank</td></tr>
<tr><td>0x39</td><td>RW</td><td>CUS_PKT2</td><td colspan="8">RESV [7:0]</td></tr>
<tr><td>0x3A</td><td>RW</td><td>CUS_PKT3</td><td colspan="8">RESV [7:0]</td></tr>
<tr><td>0x3B</td><td>RW</td><td>CUS_PKT4</td><td colspan="8">PREAM_VALUE [7:0]</td></tr>
<tr><td>0x3C</td><td>RW</td><td>CUS_PKT5</td><td>RESV</td><td colspan="3">SYNC_TOL [2:0]</td><td colspan="3">SYNC_SIZE [2:0]</td><td>SYNC_MAN_EN</td></tr>
<tr><td>0x3D</td><td>RW</td><td>CUS_PKT6</td><td colspan="8">SYNC_VALUE [7:0]</td></tr>
<tr><td>0x3E</td><td>RW</td><td>CUS_PKT7</td><td colspan="8">SYNC_VALUE [15:8]</td></tr>
<tr><td>0x3F</td><td>RW</td><td>CUS_PKT8</td><td colspan="8">SYNC_VALUE [23:16]</td></tr>
<tr><td>0x40</td><td>RW</td><td>CUS_PKT9</td><td colspan="8">SYNC_VALUE [31:24]</td></tr>
<tr><td>0x41</td><td>RW</td><td>CUS_PKT10</td><td colspan="8">SYNC_VALUE [39:32]</td></tr>
<tr><td>0x42</td><td>RW</td><td>CUS_PKT11</td><td colspan="8">SYNC_VALUE [47:40]</td></tr>
<tr><td>0x43</td><td>RW</td><td>CUS_PKT12</td><td colspan="8">SYNC_VALUE [55:48]</td></tr>
<tr><td>0x44</td><td>RW</td><td>CUS_PKT13</td><td colspan="8">SYNC_VALUE [63:56]</td></tr>
<tr><td>0x45</td><td>RW</td><td>CUS_PKT14</td><td>RESV</td><td colspan="3">PAYLOAD_LENG [10:8]</td><td>AUTO_ACK_EN</td><td>NODE_LENG_POS_SEL</td><td>PAYLOAD_BIT_ORDER</td><td>PKT_TYPE</td></tr>
<tr><td>0x46</td><td>RW</td><td>CUS_PKT15</td><td colspan="8">PAYLOAD_LENG [7:0]</td></tr>
<tr><td>0x47</td><td>RW</td><td>CUS_PKT16</td><td>RESV</td><td>RESV</td><td>NODE_FREE_EN</td><td>NODE_ERR_MASK</td><td colspan="2">NODE_SIZE [1:0]</td><td colspan="2">NODE_DET_MODE [1:0]</td></tr>
<tr><td>0x48</td><td>RW</td><td>CUS_PKT17</td><td colspan="8">NODE_VALUE [7:0]</td></tr>
<tr><td>0x49</td><td>RW</td><td>CUS_PKT18</td><td colspan="8">NODE_VALUE [15:8]</td></tr>
<tr><td>0x4A</td><td>RW</td><td>CUS_PKT19</td><td colspan="8">NODE_VALUE [23:16]</td></tr>
<tr><td>0x4B</td><td>RW</td><td>CUS_PKT20</td><td colspan="8">NODE_VALUE [31:24]</td></tr>
<tr><td>0x4C</td><td>RW</td><td>CUS_PKT21</td><td>FEC_TYPE</td><td>FEC_EN</td><td>CRC_BYTE_SWAP</td><td>CRC_BIT_INV</td><td>CRC_RANGE</td><td colspan="2">CRC_TYPE [1:0]</td><td>CRC_EN</td></tr>
<tr><td>0x4D</td><td>RW</td><td>CUS_PKT22</td><td colspan="8">CRC_SEED [7:0]</td></tr>
<tr><td>0x4E</td><td>RW</td><td>CUS_PKT23</td><td colspan="8">CRC_SEED [15:8]</td></tr>
<tr><td>0x4F</td><td>RW</td><td>CUS_PKT24</td><td>CRC_BIT_ORDER</td><td>WHITEN_SEED [8]</td><td>WHITEN_SEED_TYPE</td><td colspan="2">WHITEN_TYPE [1:0]</td><td>WHITEN_EN</td><td>MANCH_TYPE</td><td>MANCH_EN</td></tr>
<tr><td>0x50</td><td>RW</td><td>CUS_PKT25</td><td colspan="8">WHITEN_SEED [7:0]</td></tr>
<tr><td>0x51</td><td>RW</td><td>CUS_PKT26</td><td colspan="8">RESV [7:0]</td></tr>
<tr><td>0x52</td><td>RW</td><td>CUS_PKT27</td><td colspan="8">RESV [7:0]</td></tr>
<tr><td>0x53</td><td>RW</td><td>CUS_PKT28</td><td colspan="8">RESV [7:0]</td></tr>
<tr><td>0x54</td><td>RW</td><td>CUS_PKT29</td><td>RESV</td><td colspan="7">FIFO_TH [6:0]</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x55</td><td>RW</td><td>CUS_RESV1</td><td colspan="8" rowspan="10">Reserved field, no needs to write in</td><td rowspan="10">Reserve Bank</td></tr>
<tr><td>0x56</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x57</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x58</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x59</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x5A</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x5B</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x5C</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x5D</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><td>0x5E</td><td>RW</td><td>CUS_RESV1</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x5F</td><td>RW</td><td>CUS_LBD</td><td colspan="8">LBD_TH [7:0]</td><td>LBD Bank</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x60</td><td>RW</td><td>CUS_MODE_CTL</td><td colspan="8">CHIP_MODE_SWT [7:0]</td><td rowspan="11">Control Bank 1</td></tr>
<tr><td>0x61</td><td>RW</td><td>CUS_MODE_STA</td><td colspan="2">RESV [1:0]</td><td>RSTN_IN_EN</td><td>CFG_RETAIN</td><td colspan="4">CHIP_MODE_STA [3:0]</td></tr>
<tr><td>0x62</td><td>RW</td><td>CUS_EN_CTL</td><td colspan="2">RESV [1:0]</td><td>LOCKING_EN</td><td>FIFO_AUTO_CLR_DIS</td><td colspan="4">RESV [3:0]</td></tr>
<tr><td>0x63</td><td>RW</td><td>CUS_FREQ_CHNL</td><td colspan="8">FH_CHANNEL [7:0]</td></tr>
<tr><td>0x64</td><td>RW</td><td>CUS_FREQ_OFS</td><td colspan="8">FH_OFFSET [7:0]</td></tr>
<tr><td>0x65</td><td>RW</td><td>CUS_IO_SEL</td><td colspan="2">RESV [1:0]</td><td colspan="2">GPIO3_SEL [1:0]</td><td colspan="2">GPIO2_SEL [1:0]</td><td colspan="2">GPIO1_SEL [1:0]</td></tr>
<tr><td>0x66</td><td>RW</td><td>CUS_INT1_CTL</td><td colspan="2">RESV [1:0]</td><td>INT_POLAR</td><td colspan="5">INT1_SEL [4:0]</td></tr>
<tr><td>0x67</td><td>RW</td><td>CUS_INT2_CTL</td><td>RESV</td><td>LFOSC_OUT_EN</td><td>RESV</td><td colspan="5">INT2_SEL [4:0]</td></tr>
<tr><td>0x68</td><td>RW</td><td>CUS_INT_EN</td><td>SL_TMO_EN</td><td>RX_TMO_EN</td><td>RESV</td><td>PREAM_OK_EN</td><td>SYNC_OK_EN</td><td>NODE_OK_EN</td><td>CRC_OK_EN</td><td>PKT_DONE_EN</td></tr>
<tr><td>0x69</td><td>RW</td><td>CUS_FIFO_CTL</td><td colspan="3">RESV [2:0]</td><td>FIFO_AUTO_CLR_DIS</td><td colspan="2">RESV [1:0]</td><td>FIFO_MERGE_EN</td><td>RESV</td></tr>
<tr><td>0x6A</td><td>W</td><td>CUS_INT_CLR1</td><td colspan="2">RESV [1:0]</td><td>SL_TMO_FLG</td><td>RX_TMO_FLG</td><td colspan="2">RESV [1:0]</td><td>SL_TMO_CLR</td><td>RX_TMO_CLR</td></tr>
<tr><th>Addr</th><th>R/W</th><th>Name</th><th>Bit 7</th><th>Bit 6</th><th>Bit 5</th><th>Bit 4</th><th>Bit 3</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th><th>Function</th></tr>
<tr><td>0x6B</td><td>W</td><td>CUS_INT_CLR2</td><td colspan="2">RESV [1:0]</td><td>LBD_CLR</td><td>PREAM_OK_CLR</td><td>SYNC_OK_CLR</td><td>NODE_OK_CLR</td><td>CRC_OK_CLR</td><td>PKT_DONE_CLR</td><td rowspan="7">Control Bank 2</td></tr>
<tr><td>0x6C</td><td>W</td><td>CUS_FIFO_CLR</td><td colspan="5">RESV [4:0]</td><td>FIFO_RESTORE</td><td>FIFO_CLR_RX</td><td>RESV</td></tr>
<tr><td>0x6D</td><td>R</td><td>CUS_INT_FLAG</td><td>LBD_FLG</td><td>COL_ERR_FLG</td><td>PKT_ERR_FLG</td><td>PREAM_OK_FLG</td><td>SYNC_OK_FLG</td><td>NODE_OK_FLG</td><td>CRC_OK_FLG</td><td>PKT_OK_FLG</td></tr>
<tr><td>0x6E</td><td>R</td><td>CUS_FIFO_FLAG</td><td>RESV</td><td>RX_FIFO_FULL_FLG</td><td>RX_FIFO_NMTY_FLG</td><td>RX_FIFO_TH_FLG</td><td>RX_FIFO_OVF_FLG</td><td colspan="3">RESV [2:0]</td></tr>
<tr><td>0x6F</td><td>R</td><td>CUS_RSSI_CODE</td><td colspan="8">RSSI_CODE [7:0]</td></tr>
<tr><td>0x70</td><td>R</td><td>CUS_RSSI_DBM</td><td colspan="8">RSSI_DBM [7:0]</td></tr>
<tr><td>0x71</td><td>R</td><td>CUS_LBD_RESULT</td><td colspan="8">LBD_RESULT [7:0]</td></tr>
</table>

From the above table, it can be seen that the address range is from 0x00 to 0x71, which can be divided into 3 main banks for better understanding. They are: Configuration bank (including 7 sub-banks), Control Bank1, and Control Bank 2. For the 3 banks the address is continuous. They are all accessed via the SPI bus. They have different functionalities and design purposes, which are shown in the below table:

Table 19. Description of Register Banks

Address	Bank Name		Bank Name in the RFPDKExport File	Functionality
0x00-0x0B	Configuration Bank (RFPDK export the register values）	CMT Bank	CMT Bank	Users do not change them.
0x0C-0x17		System Bank	System Bank	Mainly relates to low power mode.
0x18-0x1F		Frequency Bank	Frequency Bank	To setup the RX frequencies.
0x20-0x37		Data Rate Bank	Data Rate Bank	To setup data rate, deviation, bandwidths and other related parameters.
0x38-0x54		Baseband Bank	Baseband Bank	To setup packet format and some FIFO features.
0x55-0x5E		Reserve Bank	Reserve Bank	No needs to write in.
0x5F		LBD Bank	LBD Bank	Store the LBD threshold
0x60-0x6A	Control Bank 1（Set by MCU in application, not generated by RFPDK）		--	To setup chip working state, frequency hopping, GPIOs and interrupts control.
0x6B-0x71	Control Bank 1（Set by MCU in application, not generated by RFPDK）		--	To read interrupt flags and RSSI value, control the FIFO.

To simplify the operation, users should firstly setup all the desired parameters on the RFPDK, export the register contents to the HEX file, and use it to initialize the CMT2219B. For the CMT Bank, Frequency Bank, and the Data Rate Bank, users do not need to study the details of the registers. Instead, these register configurations totally rely on the RFPDK. For System Bank and Baseband Bank, users must study the details in order to play with them in different applications. Meanwhile, for Control Bank 1 and 2, users must also understand the meaning of each register.

CMOSTEK provides a series Application Notes (AN) for the users to study how to play with the chip, how to configure the parameters on RFPDK, how to use each register, and other notable application skills. Users can start their learning from reading “AN161 CMT2219BW Quick Start Guide”, which provides step-by-step guidance and leads the users to read other documents.

9. Ordering Information

Table 20. CMT2219B ordering information

Part Number	Descriptions	Packaging	Packing	Condition	MOQ
CMT2219B-EQR[1]	CMT2219B, Ultra Low Power Sub-1GHz RF Receiver	QFN16 (3x3)	Tape& Reel	1.8 to 3.6V, -40 to 85℃	3,000

Note:

[1]. "E" represents extended industrial grade.The temperature range is from -40 to +85.
"Q" represents QFN16 packaging.
"R" represents tape &reel packing. MOQ is 3000pcs.

For more information about product, please visitwww.hoperf.com.
For purchasing or price requirements, please contactsales@hoperf.com or local sales representative.

10. Packaging Information

CMT2219B packaging is QFN16 (3x3). The packaging information is as below.

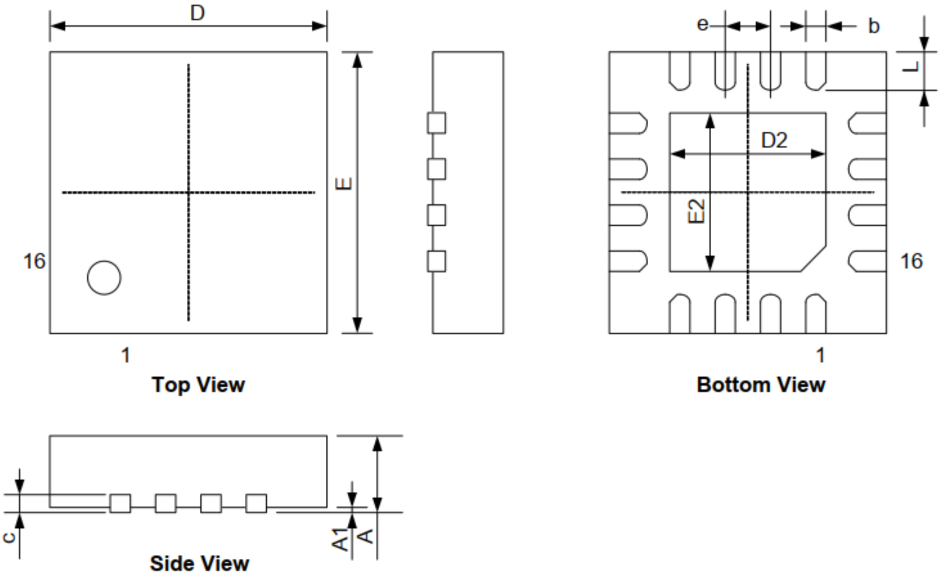


Figure 21. 16-Pin QFN 3x3 packaging

Table 21. 16-Pin QFN 3x3 Packaging Size

Symbol	Size (mm)	
	Min.	Max.
A	0.7	0.8
A1	—	0.05
b	0.18	0.30
c	0.18	0.25
D	2.90	3.10
D2	1.55	1.75
e	0.50 BSC	
E	2.90	3.10
E2	1.55	1.75
L	0.35	0.45

11. Top Marking

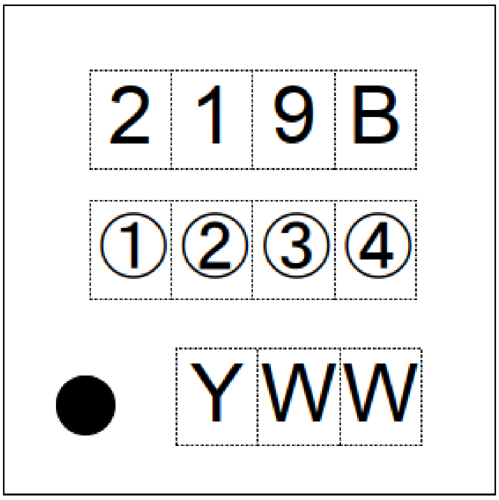


Figure 22. CMT2219B top marking

Table 22. CMT2219B top marking description

Marking method	Laser
Pin 1 mark	Circle diameter = 0.3 mm
Font size	0.5 mm, right aligned.
Line 1 marking	219B represents model CMT2219B
Line 2 marking	①②③④ **represents the** internal tracking coding
Line 3 marking	Date code is assigned by assembly factory. Y represents the last digit of the year. WW represents working week.

12. Document Change List

Table 23. Document Change List

Rev. No.	Chapter	Change Descriptions	Date
Preliminary	All	Preliminary version for internal verification	2017-08-07
0.2	5	Change some descriptions	2017-08-15
0.3	All	Change some descriptions	2017-08-18
0.4	3	Added ROM list	2017-09-04
0.5	All	Full update	2018-01-08
0.6	All	Change some descriptions	2018-01-15
0.7	4.2.7	Remove reference document AN196	2020-09-14
0.8	1.4	Change the Unit of Co-channel rejection，Adjacent channel rejection， Blocking，Image Rejection from dBc to dB.	2023-05-19

13. Contact Information

Shenzhen Hope Microelectronics Co., Ltd.