

## ICL7660S, ICL7660A

### Super Voltage Converters

FN3179  
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The ICL7660S and ICL7660A Super Voltage Converters are monolithic CMOS voltage conversion ICs that guarantee significant performance advantages over other similar devices. They are direct replacements for the industry standard ICL7660 offering an **extended** operating supply voltage range up to 12V, with **lower** supply current. A **Frequency Boost pin** has been incorporated to enable the user to achieve lower output impedance despite using smaller capacitors. All improvements are highlighted in the "Electrical Specifications" section on page 3. **Critical parameters are guaranteed over the entire commercial and industrial temperature ranges.**

The ICL7660S and ICL7660A perform supply voltage conversions from positive to negative for an input range of 1.5V to 12V, resulting in complementary output voltages of -1.5V to -12V. Only two non-critical external capacitors are needed, for the charge pump and charge reservoir functions. The ICL7660S and ICL7660A can be connected to function as a voltage doubler and will generate up to 22.8V with a 12V input. They can also be used as a voltage multipliers or voltage dividers.

Each chip contains a series DC power supply regulator, RC oscillator, voltage level translator, and four output power MOS switches. The oscillator, when unloaded, oscillates at a nominal frequency of 10kHz for an input supply voltage of 5.0V. This frequency can be lowered by the addition of an external capacitor to the "OSC" terminal, or the oscillator may be over-driven by an external clock.

The "LV" terminal may be tied to GND to bypass the internal series regulator and improve low voltage (LV) operation. At medium to high voltages (3.5V to 12V), the LV pin is left floating to prevent device latchup.

In some applications, an external Schottky diode from  $V_{OUT}$  to CAP- is needed to guarantee latchup free operation (see Do's and Don't's section on page 8).

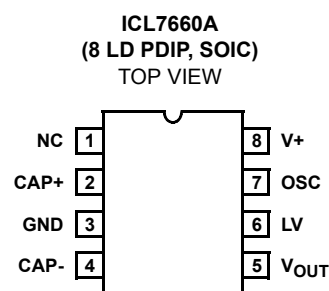
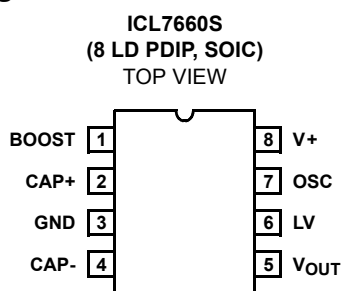
### Features

- Guaranteed Lower Max Supply Current for All Temperature Ranges
- Wide Operating Voltage Range: 1.5V to 12V
- 100% Tested at 3V
- Boost Pin (Pin 1) for Higher Switching Frequency
- Guaranteed Minimum Power Efficiency of 96%
- Improved Minimum Open Circuit Voltage Conversion Efficiency of 99%
- Improved SCR Latchup Protection
- Simple Conversion of +5V Logic Supply to  $\pm 5V$  Supplies
- Simple Voltage Multiplication  $V_{OUT} = (-)nV_{IN}$
- Easy to Use; Requires Only Two External Non-Critical Passive Components
- Improved Direct Replacement for Industry Standard ICL7660 and Other Second Source Devices
- Pb-Free Available (RoHS Compliant)

### Applications

- Simple Conversion of +5V to  $\pm 5V$  Supplies
- Voltage Multiplication  $V_{OUT} = \pm nV_{IN}$
- Negative Supplies for Data Acquisition Systems and Instrumentation
- RS232 Power Supplies
- Supply Splitter,  $V_{OUT} = \pm V_S$

### Pin Configurations



## Ordering Information

PART NUMBER (NOTE 3)	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ICL7660SCBA (Note 1)	7660 SCBA	0 to +70	8 Ld SOIC	M8.15
ICL7660SCBAZ (Notes 1, 2)	7660 SCBAZ	0 to +70	8 Ld SOIC (Pb-free)	M8.15
ICL7660SCPA	7660S CPA	0 to +70	8 Ld PDIP	E8.3
ICL7660SCPAZ (Note 2)	7660S CPAZ	0 to +70	8 Ld PDIP (Pb-free; Note 4)	E8.3
ICL7660SIBA (Note 1)	7660 SIBA	-40 to +85	8 Ld SOIC	M8.15
ICL7660SIBAZ (Notes 1, 2)	7660 SIBAZ	-40 to +85	8 Ld SOIC (Pb-free)	M8.15
ICL7660SIPA	7660 SIPA	-40 to +85	8 Ld PDIP	E8.3
ICL7660SIPAZ (Note 2)	7660S IPAZ	-40 to +85	8 Ld PDIP (Pb-free; Note 4)	E8.3
ICL7660ACBA (Note 1)	7660ACBA	0 to 70	8 Ld SOIC (N)	M8.15
ICL7660ACBAZA (Notes 1, 2)	7660ACBAZ	0 to 70	8 Ld SOIC (N) (Pb-free)	M8.15
ICL7660ACPA	7660ACPA	0 to 70	8 Ld PDIP	E8.3
ICL7660ACPAZ (Note 2)	7660ACPAZ	0 to 70	8 Ld PDIP (Pb-free; Note 4)	E8.3
ICL7660AIBA (Note 1)	7660AIBA	-40 to 85	8 Ld SOIC (N)	M8.15
ICL7660AIBAZA (Notes 1, 2)	7660AIBAZ	-40 to 85	8 Ld SOIC (N) (Pb-free)	M8.15

### NOTES:

1. Add "-T\*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ICL7660S](#), [ICL7660A](#). For more information on MSL, please see Tech Brief [TB363](#).
4. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in reflow solder processing applications.

**Absolute Maximum Ratings**

Supply Voltage	+13.0V
LV and OSC Input Voltage (Note 5)	
V+ < 5.5V	-0.3V to V+ + 0.3V
V+ > 5.5V	V+ -5.5V to V+ +0.3V
Current into LV (Note 5)	
V+ > 3.5V	.20μA
Output Short Duration	
V <sub>SUPPLY</sub> ≤ 5.5V	Continuous

**Operating Conditions**

Temperature Range	
ICL7660SI, ICL7660AI	-40°C to +85°C
ICL7660SC, ICL7660AC	0°C to +70°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

**NOTES:**

5. Connecting any terminal to voltages greater than V+ or less than GND may cause destructive latchup. It is recommended that no inputs from sources operating from external supplies be applied prior to "power up" of ICL7660S and ICL7660A.
6. θ<sub>JA</sub> is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief [TB379](#) for details.
7. For θ<sub>JC</sub>, the "case temp" location is taken at the package top center.
8. Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in reflow solder processing applications.

**Thermal Information**

Thermal Resistance (Typical, Notes 6, 7)	θ <sub>JA</sub> (°C/W)	θ <sub>JC</sub> (°C/W)
8 Ld PDIP*	110	59
8 Ld Plastic SOIC	160	48
Storage Temperature Range	-65°C to +150°C	
Pb-free reflow profile	see link below	
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

\*Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in reflow solder processing applications.

**Electrical Specifications** ICL7660S and ICL7660A, V+ = 5V, T<sub>A</sub> = +25°C, OSC = Free running (see Figure 12, "ICL7660S Test Circuit" on page 7 and Figure 13 "ICL7660A Test Circuit" on page 7), unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Supply Current (Note 11)	I+	R <sub>L</sub> = ∞, +25°C	-	80	160	μA
		0°C < T <sub>A</sub> < +70°C	-	-	180	μA
		-40°C < T <sub>A</sub> < +85°C	-	-	180	μA
		-55°C < T <sub>A</sub> < +125°C	-	-	200	μA
Supply Voltage Range - High (Note 12)	V <sub>+H</sub>	R <sub>L</sub> = 10k, LV Open, T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>	3.0	-	12	V
Supply Voltage Range - Low	V <sub>+L</sub>	R <sub>L</sub> = 10k, LV to GND, T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub>	1.5	-	3.5	V
Output Source Resistance	R <sub>OUT</sub>	I <sub>OUT</sub> = 20mA	-	60	100	Ω
		I <sub>OUT</sub> = 20mA, 0°C < T <sub>A</sub> < +70°C	-	-	120	Ω
		I <sub>OUT</sub> = 20mA, -25°C < T <sub>A</sub> < +85°C	-	-	120	Ω
		I <sub>OUT</sub> = 20mA, -55°C < T <sub>A</sub> < +125°C	-	-	150	Ω
		I <sub>OUT</sub> = 3mA, V+ = 2V, LV = GND, 0°C < T <sub>A</sub> < +70°C	-	-	250	Ω
		I <sub>OUT</sub> = 3mA, V+ = 2V, LV = GND, -40°C < T <sub>A</sub> < +85°C	-	-	300	Ω
Oscillator Frequency (Note 10)	f <sub>OSC</sub>	C <sub>OSC</sub> = 0, Pin 1 Open or GND	5	10	-	kHz
		C <sub>OSC</sub> = 0, Pin 1 = V+	-	35	-	kHz
Power Efficiency	P <sub>EFF</sub>	R <sub>L</sub> = 5kΩ	96	98	-	%
		T <sub>MIN</sub> < T <sub>A</sub> < T <sub>MAX</sub> R <sub>L</sub> = 5kΩ	95	97	-	-
Voltage Conversion Efficiency	V <sub>OUTEFF</sub>	R <sub>L</sub> = ∞	99	99.9	-	%

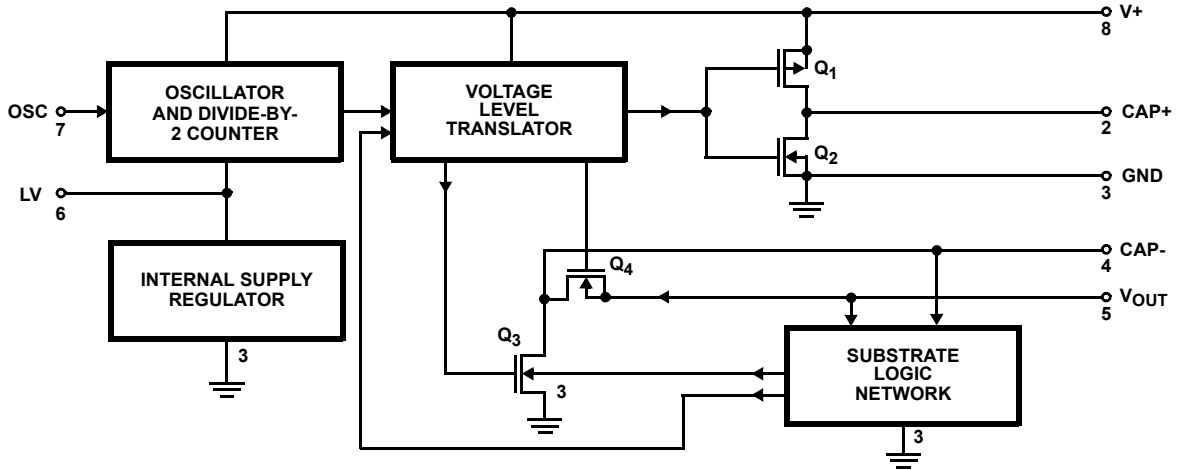
**Electrical Specifications** ICL7660S and ICL7660A,  $V_+ = 5V$ ,  $T_A = +25^\circ\text{C}$ , OSC = Free running (see Figure 12, "ICL7660S Test Circuit" on page 7 and Figure 13 "ICL7660A Test Circuit" on page 7), unless otherwise specified. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNITS
Oscillator Impedance	$Z_{OSC}$	$V_+ = 2V$	-	1	-	$M\Omega$
		$V_+ = 5V$	-	100	-	$k\Omega$
<b>ICL7660A, <math>V_+ = 3V</math>, <math>T_A = 25^\circ\text{C}</math>, OSC = Free running, Test Circuit Figure 13, unless otherwise specified</b>						
Supply Current (Note 13)	I+	$V_+ = 3V$ , $R_L = \infty$ , $+25^\circ\text{C}$	-	26	100	$\mu\text{A}$
		$0^\circ\text{C} < T_A < +70^\circ\text{C}$	-	-	125	$\mu\text{A}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	-	-	125	$\mu\text{A}$
Output Source Resistance	$R_{OUT}$	$V_+ = 3V$ , $I_{OUT} = 10\text{mA}$	-	97	150	$\Omega$
		$0^\circ\text{C} < T_A < +70^\circ\text{C}$	-	-	200	$\Omega$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	-	-	200	$\Omega$
Oscillator Frequency (Note 13)	$f_{OSC}$	$V_+ = 3V$ (same as 5V conditions)	5.0	8	-	$\text{kHz}$
		$0^\circ\text{C} < T_A < +70^\circ\text{C}$	3.0	-	-	$\text{kHz}$
		$-40^\circ\text{C} < T_A < +85^\circ\text{C}$	3.0	-	-	$\text{kHz}$

## NOTES:

9. Parameters with MIN and/or MAX limits are 100% tested at  $+25^\circ\text{C}$ , unless otherwise specified. Temperature limits established by characterization and are not production tested.
10. In the test circuit, there is no external capacitor applied to pin 7. However, when the device is plugged into a test socket, there is usually a very small but finite stray capacitance present, on the order of 5pF.
11. The Intersil ICL7660S and ICL7660A can operate without an external diode over the full temperature and voltage range. This device will function in existing designs that incorporate an external diode with no degradation in overall circuit performance.
12. All significant improvements over the industry standard ICL7660 are highlighted.
13. Derate linearly above  $50^\circ\text{C}$  by  $5.5\text{mW}/^\circ\text{C}$ .

### Functional Block Diagram



### Typical Performance Curves

See Figure 12, "ICL7660S Test Circuit" on page 7) and Figure 13 "ICL7660A Test Circuit" on page 7

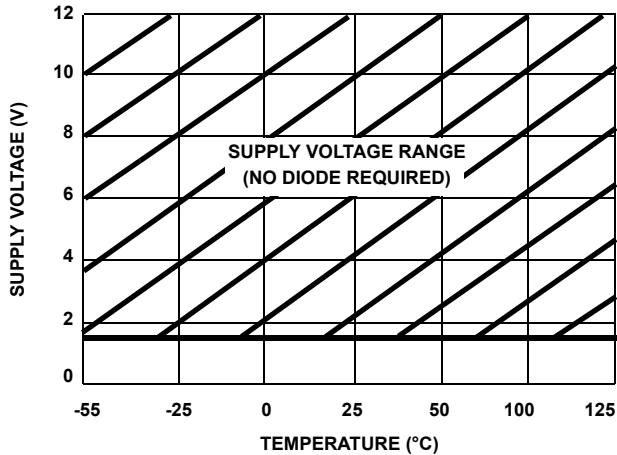


FIGURE 1. OPERATING VOLTAGE AS A FUNCTION OF TEMPERATURE

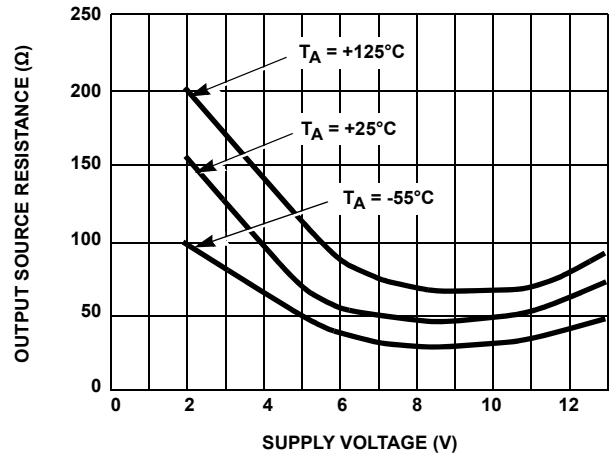


FIGURE 2. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF SUPPLY VOLTAGE

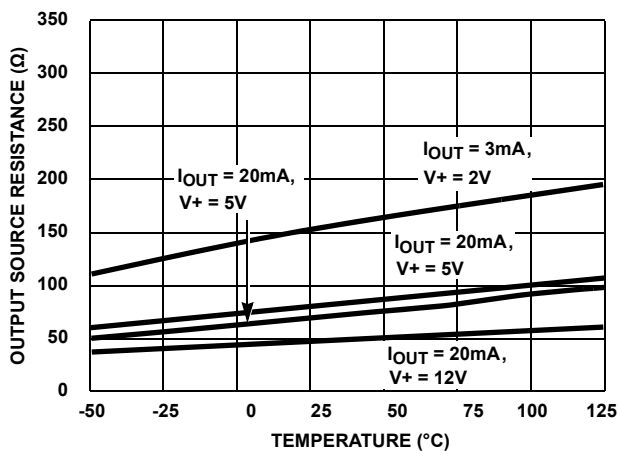


FIGURE 3. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF TEMPERATURE

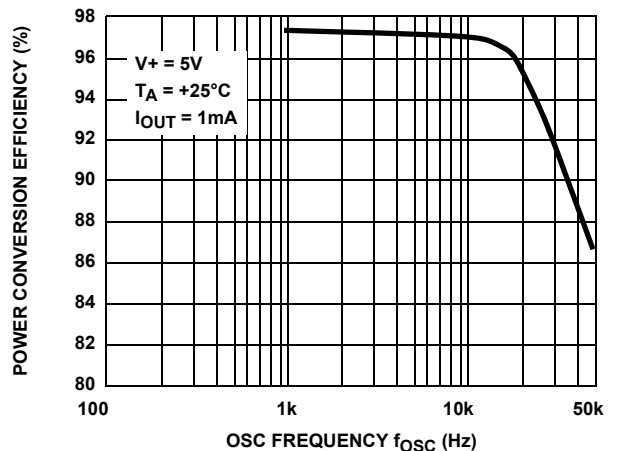


FIGURE 4. POWER CONVERSION EFFICIENCY AS A FUNCTION OF OSCILLATOR FREQUENCY

### Typical Performance Curves

See Figure 12, "ICL7660S Test Circuit" on page 7) and Figure 13 "ICL7660A Test Circuit" on page 7 (Continued)

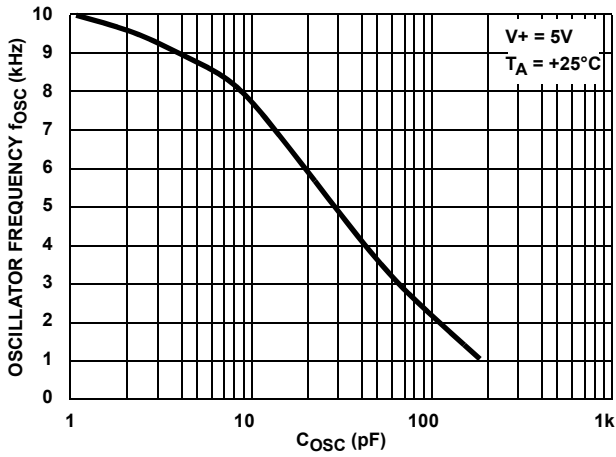


FIGURE 5. FREQUENCY OF OSCILLATION AS A FUNCTION OF EXTERNAL OSCILLATOR CAPACITANCE

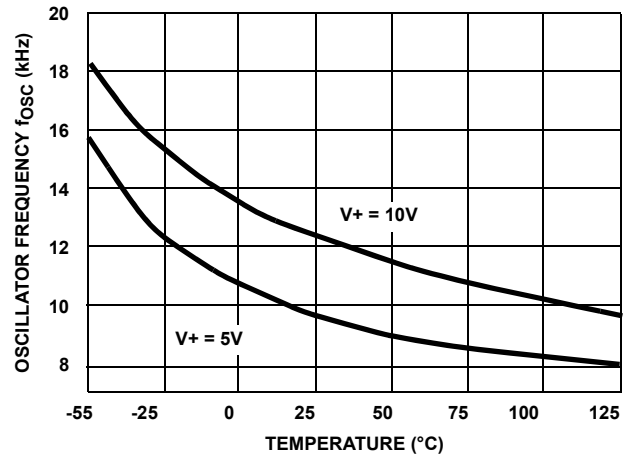


FIGURE 6. UNLOADED OSCILLATOR FREQUENCY AS A FUNCTION OF TEMPERATURE

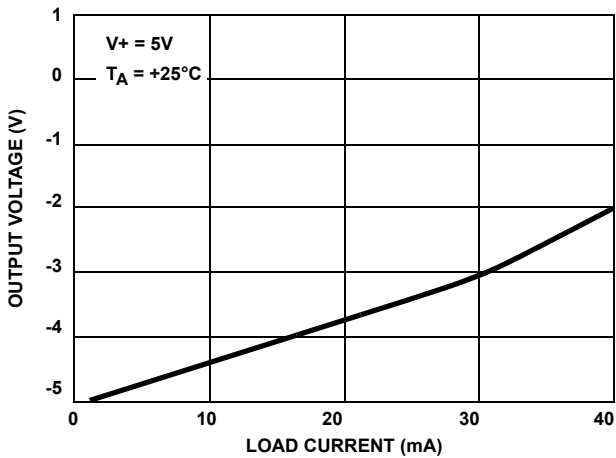


FIGURE 7. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

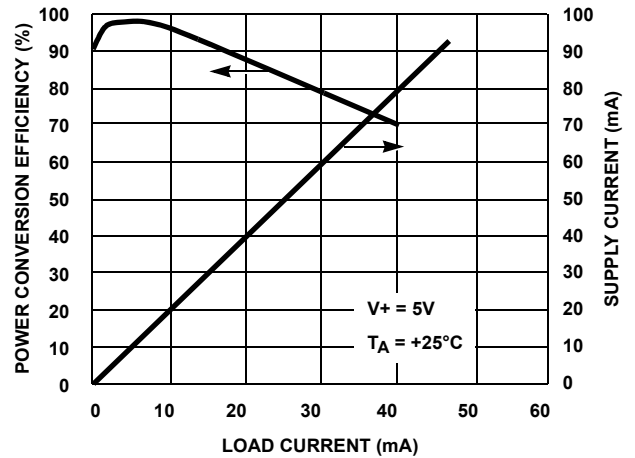


FIGURE 8. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

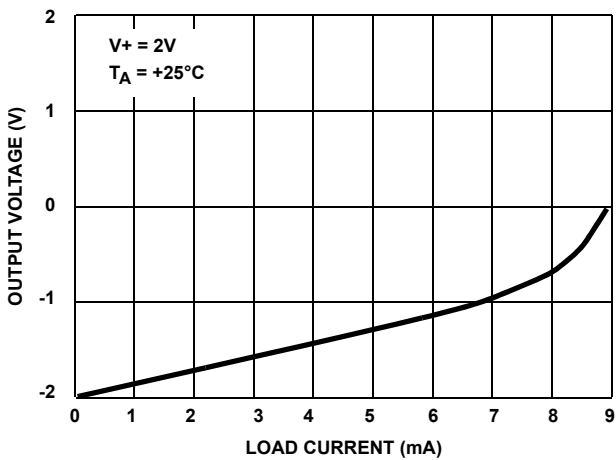


FIGURE 9. OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT CURRENT

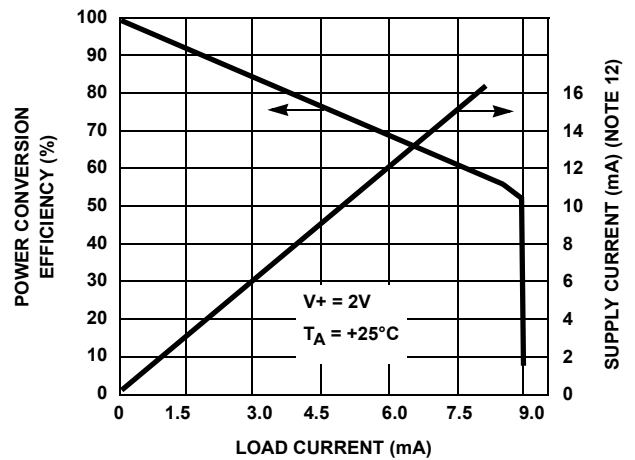
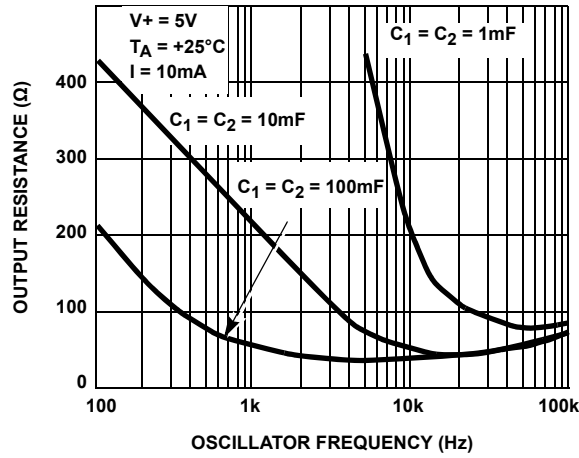


FIGURE 10. SUPPLY CURRENT AND POWER CONVERSION EFFICIENCY AS A FUNCTION OF LOAD CURRENT

**Typical Performance Curves**

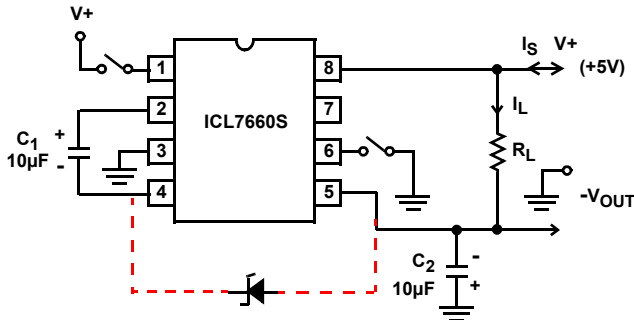
See Figure 12, "ICL7660S Test Circuit" on page 7) and Figure 13 "ICL7660A Test Circuit" on page 7 (Continued)



**FIGURE 11. OUTPUT SOURCE RESISTANCE AS A FUNCTION OF OSCILLATOR FREQUENCY**

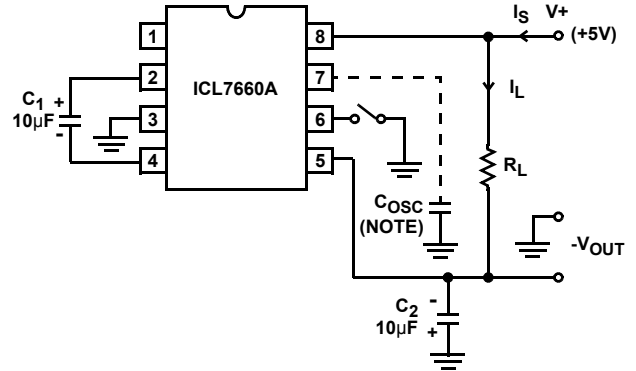
NOTE:

14. These curves include, in the supply current, that current fed directly into the load  $R_L$  from the  $V^+$  (see Figure 12). Thus, approximately half the supply current goes directly to the positive side of the load, and the other half, through the ICL7660S and ICL7660A, goes to the negative side of the load. Ideally,  $V_{OUT} \approx 2V_{IN}$ ,  $I_S \approx 2I_L$ , so  $V_{IN} \times I_S \approx V_{OUT} \times I_L$ .



NOTE: For large values of  $C_{OSC}$  ( $>1000\text{pF}$ ), the values of  $C_1$  and  $C_2$  should be increased to  $100\mu\text{F}$ .

**FIGURE 12. ICL7660S TEST CIRCUIT**



NOTE: For large values of  $C_{OSC}$  ( $>1000\text{pF}$ ) the values of  $C_1$  and  $C_2$  should be increased to  $100\mu\text{F}$ .

**FIGURE 13. ICL7660A TEST CIRCUIT**

## Detailed Description

The ICL7660S and ICL7660A contain all the necessary circuitry to complete a negative voltage converter, with the exception of two external capacitors, which may be inexpensive 10 $\mu$ F polarized electrolytic types. The mode of operation of the device may best be understood by considering Figure 14, which shows an idealized negative voltage converter. Capacitor  $C_1$  is charged to a voltage,  $V_+$ , for the half cycle, when switches  $S_1$  and  $S_3$  are closed. (Note: Switches  $S_2$  and  $S_4$  are open during this half cycle). During the second half cycle of operation, switches  $S_2$  and  $S_4$  are closed, with  $S_1$  and  $S_3$  open, thereby shifting capacitor  $C_1$  to  $C_2$  such that the voltage on  $C_2$  is exactly  $V_+$ , assuming ideal switches and no load on  $C_2$ . The ICL7660S and ICL7660A approach this ideal situation more closely than existing non-mechanical circuits.

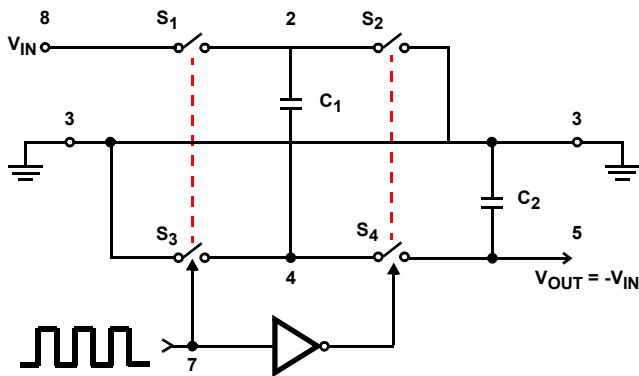


FIGURE 14. IDEALIZED NEGATIVE VOLTAGE CONVERTER

In the ICL7660S and ICL7660A, the four switches of Figure 14 are MOS power switches;  $S_1$  is a P-Channel device; and  $S_2$ ,  $S_3$  and  $S_4$  are N-Channel devices. The main difficulty with this approach is that in integrating the switches, the substrates of  $S_3$  and  $S_4$  must always remain reverse biased with respect to their sources, but not so much as to degrade their "ON" resistances. In addition, at circuit start-up, and under output short circuit conditions ( $V_{OUT} = V_+$ ), the output voltage must be sensed and the substrate bias adjusted accordingly. Failure to accomplish this would result in high power losses and probable device latch-up.

This problem is eliminated in the ICL7660S and ICL7660A by a logic network that senses the output voltage ( $V_{OUT}$ ) together with the level translators, and switches the substrates of  $S_3$  and  $S_4$  to the correct level to maintain necessary reverse bias.

The voltage regulator portion of the ICL7660S and ICL7660A is an integral part of the anti-latchup circuitry; however, its inherent voltage drop can degrade operation at low voltages. Therefore, to improve low voltage operation, the "LV" pin should be connected to GND, thus disabling the regulator. For supply voltages greater than 3.5V, the LV terminal must be left open to ensure latchup-proof operation and to prevent device damage.

## Theoretical Power Efficiency Considerations

In theory, a voltage converter can approach 100% efficiency if certain conditions are met:

1. The drive circuitry consumes minimal power.
2. The output switches have extremely low ON resistance and virtually no offset.
3. The impedance of the pump and reservoir capacitors are negligible at the pump frequency.

The ICL7660S and ICL7660A approach these conditions for negative voltage conversion if large values of  $C_1$  and  $C_2$  are used. **ENERGY IS LOST ONLY IN THE TRANSFER OF CHARGE BETWEEN CAPACITORS IF A CHANGE IN VOLTAGE OCCURS.** The energy lost is defined as shown in Equation 1:

$$E = \frac{1}{2}C_1(V_1^2 - V_2^2) \quad (\text{EQ. 1})$$

where  $V_1$  and  $V_2$  are the voltages on  $C_1$  during the pump and transfer cycles. If the impedances of  $C_1$  and  $C_2$  are relatively high at the pump frequency (see Figure 14) compared to the value of  $R_L$ , there will be a substantial difference in the voltages,  $V_1$  and  $V_2$ . Therefore it is not only desirable to make  $C_2$  as large as possible to eliminate output voltage ripple, but also to employ a correspondingly large value for  $C_1$  in order to achieve maximum efficiency of operation.

## Do's and Don'ts

1. Do not exceed maximum supply voltages.
2. Do not connect LV terminal to GND for supply voltage greater than 3.5V.
3. Do not short circuit the output to  $V^+$  supply for supply voltages above 5.5V for extended periods; however, transient conditions including start-up are okay.
4. When using polarized capacitors, the + terminal of  $C_1$  must be connected to pin 2 of the ICL7660S and ICL7660A, and the + terminal of  $C_2$  must be connected to GND.
5. If the voltage supply driving the ICL7660S and ICL7660A has a large source impedance (25 $\Omega$  to 30 $\Omega$ ), then a 2.2 $\mu$ F capacitor from pin 8 to ground may be required to limit the rate of rise of input voltage to less than 2V/ $\mu$ s.
6. If the input voltage is higher than 5V and it has a rise rate more than 2V/ $\mu$ s, an external Schottky diode from  $V_{OUT}$  to CAP- is needed to prevent latchup (triggered by forward biasing Q4's body diode) by keeping the output (pin 5) from going more positive than CAP- (pin 4).
7. User should ensure that the output (pin 5) does not go more positive than GND (pin 3). Device latch-up will occur under these conditions. To provide additional protection, a 1N914 or similar diode placed in parallel with  $C_2$  will prevent the device from latching up under these conditions, when the load on  $V_{OUT}$  creates a path to pull up  $V_{OUT}$  before the IC is active (anode pin 5, cathode pin 3).



## Typical Applications

### Simple Negative Voltage Converter

The majority of applications will undoubtedly utilize the ICL7660S and ICL7660A for generation of negative supply voltages. Figure 15 shows typical connections to provide a negative supply where a positive supply of +1.5V to +12V is available. Keep in mind that pin 6 (LV) is tied to the supply negative (GND) for supply voltage below 3.5V.

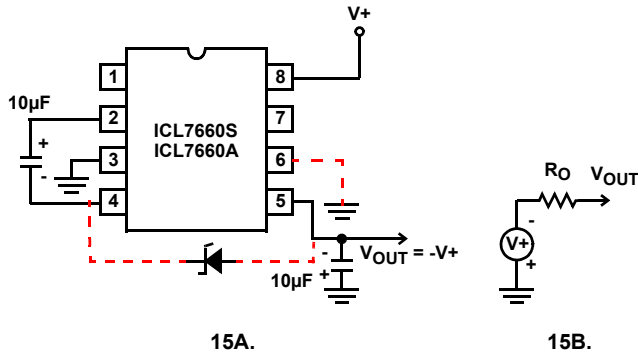


FIGURE 15. SIMPLE NEGATIVE CONVERTER AND ITS OUTPUT EQUIVALENT

The output characteristics of the circuit in Figure 15 can be approximated by an ideal voltage source in series with a resistance as shown in Figure 15B. The voltage source has a value of  $-(V_+)$ . The output impedance ( $R_O$ ) is a function of the ON resistance of the internal MOS switches (shown in Figure 14), the switching frequency, the value of  $C_1$  and  $C_2$ , and the ESR (equivalent series resistance) of  $C_1$  and  $C_2$ . A good first order approximation for  $R_O$  is shown in Equation 2:

$$R_0 \cong 2((R_{SW1} + R_{SW3} + ESR_{C1}) + 2(R_{SW2} + R_{SW4} + ESR_{C1})) \frac{1}{f_{PUMP} \times C_1} + ESR_{C2} \quad (\text{EQ. 2})$$

$$f_{PUMP} = \frac{f_{OSC}}{2} \quad (R_{SWX} = \text{MOSFET Switch Resistance})$$

Combining the four  $R_{SWX}$  terms as  $R_{SW}$ , we see in Equation 3 that:

$$R_0 \cong 2xR_{SW} + \frac{1}{f_{PUMP} \times C_1} + 4xESR_{C1} + ESR_{C2} \quad (\text{EQ. 3})$$

$R_{SW}$ , the total switch resistance, is a function of supply voltage and temperature (see the output source resistance graphs, Figures 2, 3, and 11), typically  $23\Omega$  at  $+25^\circ\text{C}$  and 5V. Careful selection of  $C_1$  and  $C_2$  will reduce the remaining terms, minimizing the output impedance. High value capacitors will reduce the  $1/(f_{PUMP} \times C_1)$  component, and low ESR capacitors will lower the ESR term. Increasing the oscillator frequency will reduce the  $1/(f_{PUMP} \times C_1)$  term, but may have the side effect of a net increase in output impedance when  $C_1 > 10\mu\text{F}$  and is not long enough to fully

charge the capacitors every cycle. Equation 4 shows a typical application where  $f_{OSC} = 10\text{kHz}$  and  $C = C_1 = C_2 = 10\mu\text{F}$ :

$$R_0 \cong 2x23 + \frac{1}{5 \times 10^3 \times 10 \times 10^{-6}} + 4xESR_{C1} + ESR_{C2} \quad (\text{EQ. 4})$$

$$R_0 \cong 46 + 20 + 5 \times ESR_C$$

Since the ESRs of the capacitors are reflected in the output impedance multiplied by a factor of 5, a high value could potentially swamp out a low  $1/f_{PUMP} \times C_1$  term, rendering an increase in switching frequency or filter capacitance ineffective. Typical electrolytic capacitors may have ESRs as high as  $10\Omega$ .

### Output Ripple

ESR also affects the ripple voltage seen at the output. The peak-to-peak output ripple voltage is given by Equation 5:

$$V_{RIPPLE} \cong \left( \frac{1}{2 \times f_{PUMP} \times C_2} + 2ESR_{C2} \times I_{OUT} \right) \quad (\text{EQ. 5})$$

A low ESR capacitor will result in a higher performance output.

### Paralleling Devices

Any number of ICL7660S and ICL7660A voltage converters may be paralleled to reduce output resistance. The reservoir capacitor,  $C_2$ , serves all devices, while each device requires its own pump capacitor,  $C_1$ . The resultant output resistance is approximated in Equation 6:

$$R_{OUT} = \frac{R_{OUT}(\text{of ICL7660S})}{n(\text{number of devices})} \quad (\text{EQ. 6})$$

### Cascading Devices

The ICL7660S and ICL7660A may be cascaded as shown to produce larger negative multiplication of the initial supply voltage. However, due to the finite efficiency of each device, the practical limit is 10 devices for light loads. The output voltage is defined as shown in Equation 7:

$$V_{OUT} = -n(V_{IN}) \quad (\text{EQ. 7})$$

where  $n$  is an integer representing the number of devices cascaded. The resulting output resistance would be approximately the weighted sum of the individual ICL7660S and ICL7660A  $R_{OUT}$  values.

### Changing the ICL7660S and ICL7660A Oscillator Frequency

It may be desirable in some applications, due to noise or other considerations, to alter the oscillator frequency. This can be achieved simply by one of several methods.

By connecting the Boost Pin (Pin 1) to  $V_+$ , the oscillator charge and discharge current is increased and, hence, the oscillator frequency is increased by approximately 3.5 times. The result is a decrease in the output impedance and ripple.

This is of major importance for surface mount applications where capacitor size and cost are critical. Smaller capacitors, such as 0.1µF, can be used in conjunction with the Boost Pin to achieve similar output currents compared to the device free running with  $C_1 = C_2 = 10\mu\text{F}$  or  $100\mu\text{F}$ . (see Figure 11).

Increasing the oscillator frequency can also be achieved by overdriving the oscillator from an external clock, as shown in Figure 16. In order to prevent device latchup, a 1kΩ resistor must be used in series with the clock output. In a situation where the designer has generated the external clock frequency using TTL logic, the addition of a 10kΩ pull-up resistor to V+ supply is required. Note that the pump frequency with external clocking, as with internal clocking, will be one-half of the clock frequency. Output transitions occur on the positive going edge of the clock.

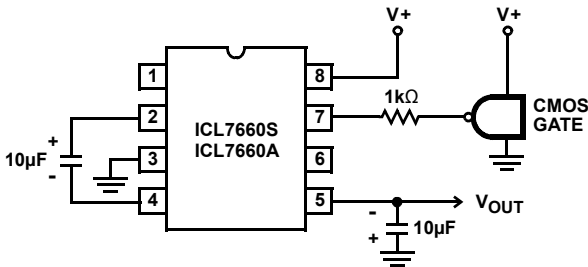


FIGURE 16. EXTERNAL CLOCKING

It is also possible to increase the conversion efficiency of the ICL7660S and ICL7660A at low load levels by lowering the oscillator frequency. This reduces the switching losses, and is shown in Figure 17. However, lowering the oscillator frequency will cause an undesirable increase in the impedance of the pump ( $C_1$ ) and reservoir ( $C_2$ ) capacitors; this is overcome by increasing the values of  $C_1$  and  $C_2$  by the same factor by which the frequency has been reduced. For example, the addition of a 100pF capacitor between pin 7 (OSC and V+) will lower the oscillator frequency to 1kHz from its nominal frequency of 10kHz (a multiple of 10), and thereby necessitate a corresponding increase in the value of  $C_1$  and  $C_2$  (from 10µF to 100µF).

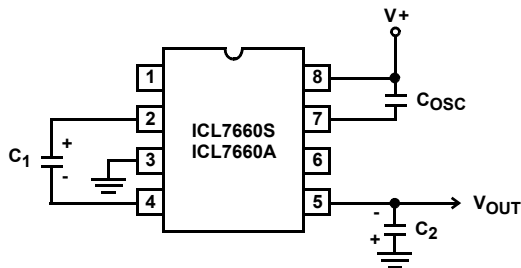
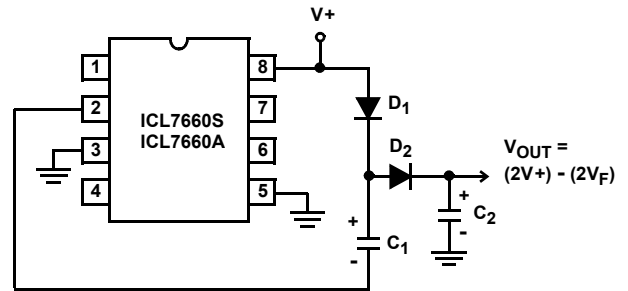


FIGURE 17. LOWERING OSCILLATOR FREQUENCY

**Positive Voltage Doubling**

The ICL7660S and ICL7660A may be employed to achieve positive voltage doubling using the circuit shown in Figure 18. In this application, the pump inverter switches of the ICL7660S and ICL7660A are used to charge  $C_1$  to a voltage level of  $V+ - V_F$ , where  $V+$  is the supply voltage and  $V_F$  is the forward voltage on  $C_1$ , plus the supply voltage ( $V+$ ) is applied through diode  $D_2$  to capacitor  $C_2$ . The voltage thus created on  $C_2$  becomes  $(2V+) - (2V_F)$  or twice the supply voltage minus the combined forward voltage drops of diodes  $D_1$  and  $D_2$ .

The source impedance of the output ( $V_{OUT}$ ) will depend on the output current, but for  $V+ = 5\text{V}$  and an output current of 10mA, it will be approximately 60Ω.



NOTE:  $D_1$  AND  $D_2$  CAN BE ANY SUITABLE DIODE.

FIGURE 18. POSITIVE VOLTAGE DOUBLER

**Combined Negative Voltage Conversion and Positive Supply Doubling**

Figure 19 combines the functions shown in Figure 15 and Figure 18 to provide negative voltage conversion and positive voltage doubling simultaneously. This approach would be suitable, for example, for generating +9V and -5V from an existing +5V supply. In this instance, capacitors  $C_1$  and  $C_3$  perform the pump and reservoir functions, respectively, for negative voltage generation, while capacitors  $C_2$  and  $C_4$  are pump and reservoir, respectively, for the doubled positive voltage. There is a penalty in this configuration which combines both functions, however, in that the source impedances of the generated supplies will be somewhat higher, due to the finite impedance of the common charge pump driver at pin 2 of the device.

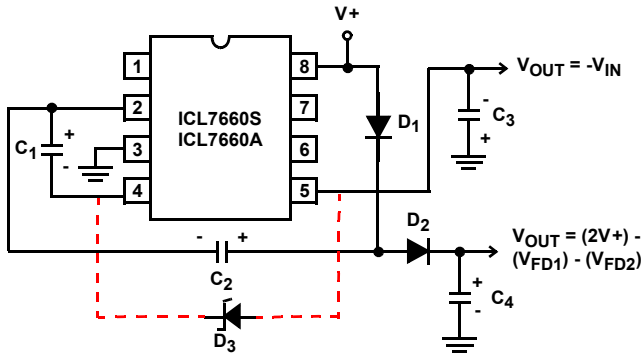


FIGURE 19. COMBINED NEGATIVE VOLTAGE CONVERTER AND POSITIVE DOUBLER

**Voltage Splitting**

The bidirectional characteristics can also be used to split a high supply in half, as shown in Figure 20. The combined load will be evenly shared between the two sides, and a high value resistor to the LV pin ensures start-up. Because the switches share the load in parallel, the output impedance is much lower than in the standard circuits, and higher currents can be drawn from the device. By using this circuit, and then the circuit of Figure 15, +15V can be converted, via +7.5 and -7.5, to a nominal -15V, although with rather high series output resistance (~250Ω).

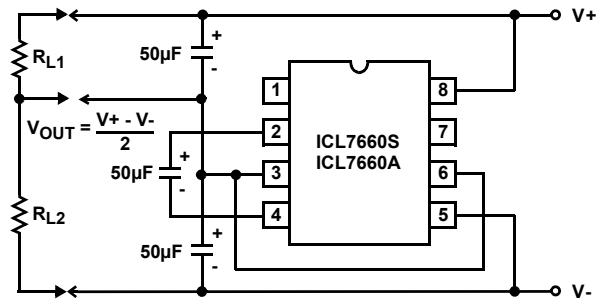


FIGURE 20. SPLITTING A SUPPLY IN HALF

**Regulated Negative Voltage Supply**

In some cases, the output impedance of the ICL7660S and ICL7660A can be a problem, particularly if the load current varies substantially. The circuit of Figure 21 can be used to overcome this by controlling the input voltage, via an ICL7611 low-power CMOS op amp, in such a way as to maintain a nearly constant output voltage. Direct feedback is inadvisable, since the ICL7660S's and ICL7660A's output does not respond instantaneously to change in input, but only after the switching delay. The circuit shown supplies enough delay to accommodate the ICL7660S and ICL7660A, while maintaining adequate feedback. An increase in pump and storage capacitors is desirable, and the values shown provide an output impedance of less than 5Ω to a load of 10mA.

**Other Applications**

Further information on the operation and use of the ICL7660S and ICL7660A may be found in application note [AN051](#), "Principles and Applications of the ICL7660 CMOS Voltage Converter".

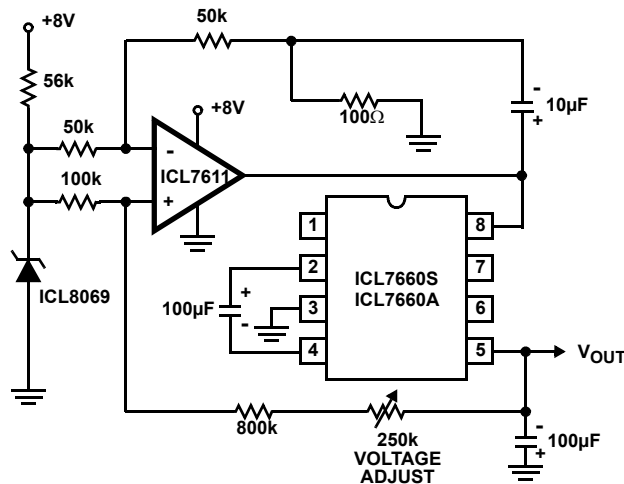
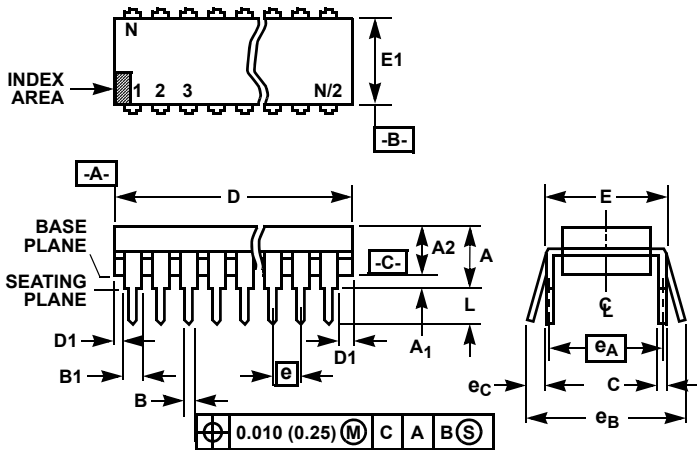


FIGURE 21. REGULATING THE OUTPUT VOLTAGE

## Dual-In-Line Plastic Packages (PDIP)



**NOTES:**

- Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
- Dimensioning and tolerancing per ANSI Y14.5M-1982.
- Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
- Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
- D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
- E and  $e_A$  are measured with the leads constrained to be perpendicular to datum  $-C-$ .
- $e_B$  and  $e_C$  are measured at the lead tips with the leads unconstrained.  $e_C$  must be zero or greater.
- B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
- N is the maximum number of terminal positions.
- Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

### E8.3 (JEDEC MS-001-BA ISSUE D) 8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
$e_A$	0.300 BSC		7.62 BSC		6
$e_B$	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

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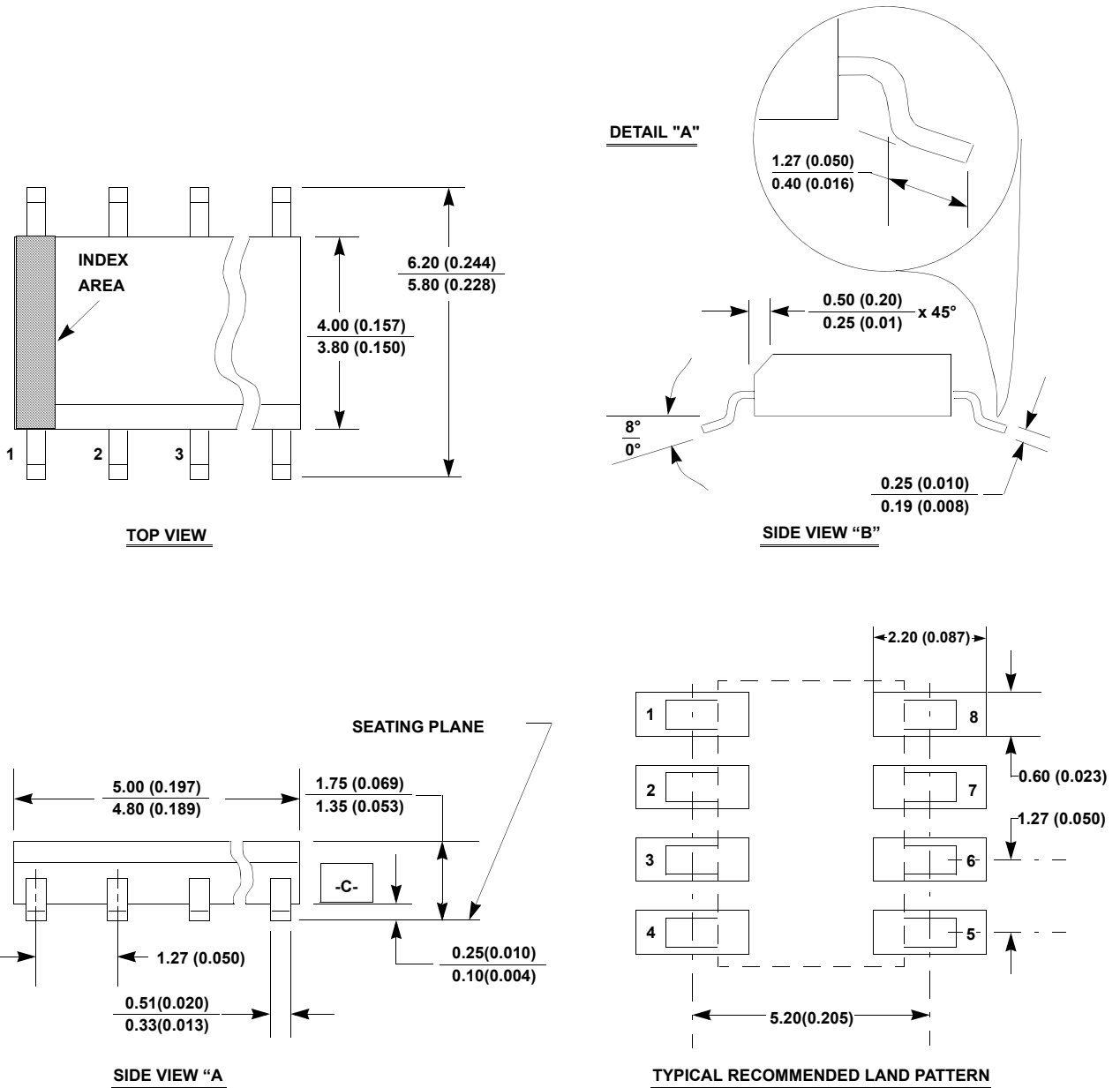
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# Package Outline Drawing

## M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 1/12



**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.