REIDITE ELECTRONICS

XIPHOS Series

Industrial System-on-Module

Family Overview Datasheet

Open-frame (XIPHOS-X1 / XIPHOS-X2)

Phantom Forge® encapsulated (XIPHOS-X3 / XIPHOS-X4)

Figure 1: Product variants: open-frame (XIPHOS-X1/XIPHOS-X2) and Phantom Forge® encapsulated (XIPHOS-X3/XIPHOS-X4).

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CE

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1 Release evolution

The following table lists document releases and their dates.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2025-02-02	Release 1.0 for distribution.

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2 Overview

The XIPHOS family is an industrial embedded computing platform aimed at control, communications, and signal processing applications in demanding environments. All modules share a base architecture with an STM32H7 microcontroller, a Lattice FPGA, and an integrated Ethernet PHY.

XIPHOS is engineered as a robust industrial processor for harsh environments where reliability, deterministic behavior, and long-term availability are critical. The combination of a high-performance MCU with a low-power uFPGA provides both real-time control and adaptable hardware acceleration, enabling specialized interfaces, timing, and data-path customization without redesigning the core platform.

The family is designed to scale across performance and protection classes while maintaining a consistent software and electrical interface, simplifying reuse across product lines and reducing time to qualification.

XIPHOS has passed **CE marking** homologation for industrial deployment. **All variants are RoHS free.**

All variants share the **same pinout and software baseline**, allowing upgrades from XIPHOS-X1 to XIPHOS-X4 without breaking firmware compatibility. The MCU + FPGA approach provides an industrial alternative to Linux-based SoCs where deterministic timing and low complexity are required.

From a system integrator perspective, XIPHOS balances deterministic control with hardware flexibility. The MCU handles real-time control loops, safety supervision, and communication stacks, while the FPGA provides timing-critical logic, protocol adaptation, and custom I/O. This division enables long-life, low-maintenance deployments without the overhead of a full Linux platform.

This document covers the family as a whole. Model-level specifications are provided in the *XIPHOS Models Datasheet*.

3 System architecture

Every XIPHOS module is built around the same core architecture: a high-performance microcontroller (MCU) for application and communication logic, a small FPGA for timing-critical or protocol-specific hardware, and an integrated Ethernet PHY for robust networking. This combination delivers deterministic real-time behaviour and hardware flexibility without the complexity of a Linux-based SoC, making XIPHOS suitable for industrial automation, motor control, and connectivity-heavy edge applications.

3.1 Core elements

The main processor is the STM32H735IGT from STMicroelectronics (), an ARM Cortex-M7 device running at up to 550 MHz with dual-bank Flash, hardware crypto, and a rich set of peripherals. The industrial processor executes the main application stack, deterministic control loops, and communication protocols (Ethernet, USB, CAN FD). The Lattice iCE40 UltraPlus FPGA (ICE40UP5K-SG48I) sits alongside the MCU and implements timing-critical or protocol-specific logic: protocol adaptation, pulse generation, custom I/O expansion, or glue logic for legacy interfaces. By offloading these tasks to the FPGA, the MCU is freed to focus on application and connectivity, while the FPGA ensures deterministic signal timing and precise control loops. Connectivity is completed by an integrated Ethernet PHY, so the module can be connected directly to an Ethernet network without an external PHY on the carrier board.

- **Main MCU:** STM32H735IGT (ARM Cortex-M7 up to 550 MHz).
- **FPGA:** Lattice iCE40 UltraPlus (ICE40UP5K-SG48I) for hardware acceleration and programmable I/O.
- **Connectivity:** Integrated Ethernet PHY for robust networking.

The STM32H735IGT provides a robust real-time core with deterministic interrupt handling, cache acceleration, and rich connectivity. The FPGA is used as an adaptable hardware fabric for I/O conditioning, state machines, and hardware handshake logic, enabling integration with legacy protocols and custom interfaces. This partitioning allows system designers to add specialised functionality without introducing a separate external coprocessor.

3.2 Common interfaces

All I/O is brought out to two 100-pin board-to-board connectors (Hirose FX11LA-100/10, J1 and J2), providing a consistent electrical and mechanical interface across the full XIPHOS-X1–XIPHOS-X4 range. The available interfaces include general-purpose digital and analogue signals (SPI, I^2C, UART, GPIO) and industrial connectivity (Ethernet via RMII or RGMII depending on carrier design, USB 2.0 OTG, CAN FD). Clock and reset signals are provided for synchronous system design. Interfaces are routed to the connector strips for clean mechanical integration and predictable signal mapping across variants, simplifying carrier-board design and allowing one carrier to support all XIPHOS variants.

- SPI, I^2C, UART, GPIO
- Ethernet, USB, CAN FD
- Ethernet RMII/RGMII (variant dependent)
- Industrial clock and reset

Designers should treat high-speed interfaces (Ethernet, USB, clock lines) as controlled-impedance signals and follow standard routing practices to minimise EMI and signal integrity issues. The shared pinout across all variants allows one carrier board to cover the full XIPHOS-X1–XIPHOS-X4 range.

4 Programming and debug

The MCU and FPGA are programmed using the official toolchains provided by their manufacturers.

4.1 MCU (STM32H735IGT)

- **Recommended interfaces:** SWD / JTAG (ST-LINK, J-Link, OpenOCD).
- **Bootloader options:** USB-DFU, UART, SPI, CAN (internal ROM).
- **Tooling:** STM32CubeIDE / STM32CubeMX, GCC ARM + GDB.

The MCU can be updated in the field without JTAG access using the built-in bootloader, while the external 8 MB Flash complements the 1 MB internal Flash.

Production updates can be staged through the bootloader, validated at startup, and rolled back if needed. This supports field maintenance without opening the enclosure or exposing debug connectors.

4.2 FPGA (iCE40UP5K-SG48I)

- **Development programming:** JTAG.
- **Production configuration:** bitstream loaded by the MCU at boot.
- **Toolchains:** Lattice iCEcube2 / Radiant, or open-source Yosys + nextpnr + IceStorm.

The FPGA can be configured persistently or loaded on each boot depending on the application workflow.

In typical deployments, the MCU verifies the FPGA bitstream integrity and loads it during boot, enabling secure and version-controlled hardware functions.

5 Phantom Forge® technology

REIDITE® Phantom Forge® is a packaging technology designed to improve environmental protection and thermal robustness while making the module difficult to access or tamper with. It is used on the XIPHOS-X3 and XIPHOS-X4 variants of XIPHOS, which are intended for demanding industrial or outdoor-like environments where open-frame assemblies would be at risk from humidity, dust, vibration, or mechanical shock.

In encapsulated versions, the assembly is overmoulded with a protective layer that provides mechanical damping, moisture ingress protection, and improved resistance to ionising radiation and harsh electromagnetic fields. This enables operation in aggressive industrial atmospheres, wash-down scenarios, or outdoor installations where dust and water exposure are a concern. The technology supports an extended industrial temperature range and improves system stability in extreme industrial and field conditions. Variant selection depends on thermal conditions, vibration, and the required protection level for the application: open-frame variants (XIPHOS-X1, XIPHOS-X2) for controlled or enclosed environments, and Phantom Forge® variants (XIPHOS-X3, XIPHOS-X4) when environmental or mechanical stress justifies encapsulation.

- **XIPHOS-X1 / XIPHOS-X2:** unencapsulated (open-frame) versions.
- **XIPHOS-X3 / XIPHOS-X4:** encapsulated versions with Phantom Forge®.

Figure 2: Phantom Forge® encapsulated module (XIPHOS-X3 / XIPHOS-X4).

6 Key features

XIPHOS combines a high-performance ARM Cortex-M7 microcontroller with a Lattice iCE40 UltraPlus FPGA and an integrated Ethernet PHY in a compact module. This hybrid architecture delivers deterministic real-time behaviour and hardware flexibility without the complexity of a Linux-based SoC. The MCU runs the application stack, control loops, and communication protocols; the FPGA handles timing-critical logic, protocol adaptation, and custom I/O. **Industrial Ethernet** is provided on-module with an integrated PHY, so the carrier board does not need an external PHY for basic networking. Optional secure boot and remote update support enable in-field maintenance and reduced downtime.

The family scales across memory and packaging: open-frame variants (XIPHOS-X1, XIPHOS-X2) for controlled environments, and Phantom Forge® encapsulated variants (XIPHOS-X3, XIPHOS-X4) for harsh or outdoor-like conditions. All variants share the same pinout and software baseline, so one carrier board and one firmware baseline can cover the full range. The extended **industrial temperature range** (from **-40 °C** up to **85 °C**, **125 °C**, or **140 °C** depending on variant) and robust design for vibration, EMI, and harsh environments make XIPHOS suitable for long-life industrial deployments. FreeRTOS and other RTOSes are commonly used; watchdog-based recovery and hardware-assisted diagnostics support resilient operation and faster fault isolation.

The following list summarises the main platform capabilities. Detailed MCU and FPGA specifications, pinout, and programming flows are provided in the models datasheet.

- Hybrid MCU + FPGA architecture.
- Industrial Ethernet with integrated PHY.
- Secure boot and remote update support (optional).
- Scalability by memory and packaging.
- Extended industrial temperature range (variant dependent).
- Deterministic timing and configurable data paths via FPGA logic.
- Robust design for vibration, EMI, and harsh environmental conditions.
- Consistent pinout and software baseline across the family.
- Hardware-assisted diagnostics for faster fault isolation.
- Supported RTOS: FreeRTOS.
- Watchdog-based recovery for resilient operation.
- **RoHS free** (all variants).

7 Target applications

- Industrial automation and process control
- Robotics and mechatronic systems
- Industrial communications and gateways
- Monitoring and data acquisition

The platform is well suited for edge systems requiring deterministic behavior, precise timing, and protocol adaptation, especially where mechanical and environmental robustness are key design constraints.

Typical deployments include factory controllers, transport monitoring units, energy management systems, and industrial gateways that require deterministic latency and long-life availability.

8 Comparison table

The following table provides a side-by-side comparison of the four XIPHOS variants. It summarises the main differences in packaging (Phantom Forge®), memory (PSRAM), and operating temperature so that the right model can be selected for each application. All variants share the same MCU, FPGA, and pinout.

RoHS free: all XIPHOS models.

TBD: to be defined based on the final configuration of each variant.

9 Manufacturing and packaging

XIPHOS is designed, developed, and assembled in Spain. Assembly is performed in qualified environments with controlled processes to minimize residues that could affect downstream industrial systems or sensitive applications. **All XIPHOS modules are RoHS free.**

Feature	XIPHOS-X1	XIPHOS-X2	XIPHOS-X3	XIPHOS-X4
Phantom Forge®	No	No	Yes	Yes
MCU (model)	STM32H735IGT	STM32H735IGT	STM32H735IGT	STM32H735IGT
MCU Flash (int.)	1 MB (ECC)	1 MB (ECC)	1 MB (ECC)	1 MB (ECC)
MCU SRAM (int.)	~564 KB	~564 KB	~564 KB	~564 KB
PSRAM (external)	None	32 MB	None	32 MB
Flash (external)	8 MB	8 MB	8 MB	8 MB
Lattice FPGA (model)	ICE40UP5K-SG48I	ICE40UP5K-SG48I	ICE40UP5K-SG48I	ICE40UP5K-SG48I
Ethernet PHY	Integrated	Integrated	Integrated	Integrated
Min temperature	-40 °C	-40 °C	-40 °C	-40 °C
Max temperature	85 °C	125 °C	140 °C	140 °C

Table 1: Comparison of XIPHOS-X1, XIPHOS-X2, XIPHOS-X3, and XIPHOS-X4.

Process control includes ESD protection, particulate monitoring, and clean handling procedures. This reduces the risk of contamination in precision systems and ensures repeatable assembly quality over long production runs.

9.1 Packaging

Units are supplied in protective retail boxes for low-volume orders. For higher volumes, modules can be shipped in individual plastic trays to ensure handling protection and production-line compatibility.

Packaging is designed to prevent connector damage and maintain traceability throughout the logistics chain.

10 Quality and reliability

The XIPHOS platform is intended for long-life industrial deployments where stability and predictable behavior are essential. The architecture favors component selection with extended availability and established supply chains, and the design prioritizes signal integrity, EMC resilience, and thermal margin.

Typical reliability-oriented characteristics include:

- Conservative clocking and power distribution for margin and longevity.
- Robust reset and watchdog strategies for fault recovery.
- EMC-conscious layout practices to reduce susceptibility and emissions.
- Support for environmental protection through Phantom Forge® encapsulation.

Qualification activities focus on repeatability, thermal cycling, and vibration stress. Designs are validated to sustain extended operation in industrial environments with minimal drift and consistent electrical behavior.

10.1 Certifications and protection

The XIPHOS family has passed **CE marking** homologation and is designed for industrial compliance requirements. **All XIPHOS modules are RoHS free.** It is specified for vibration and temperature certification (per applicable standards), and the encapsulated variants meet **IP66** protection for dust and water ingress resistance.

11 Block diagram

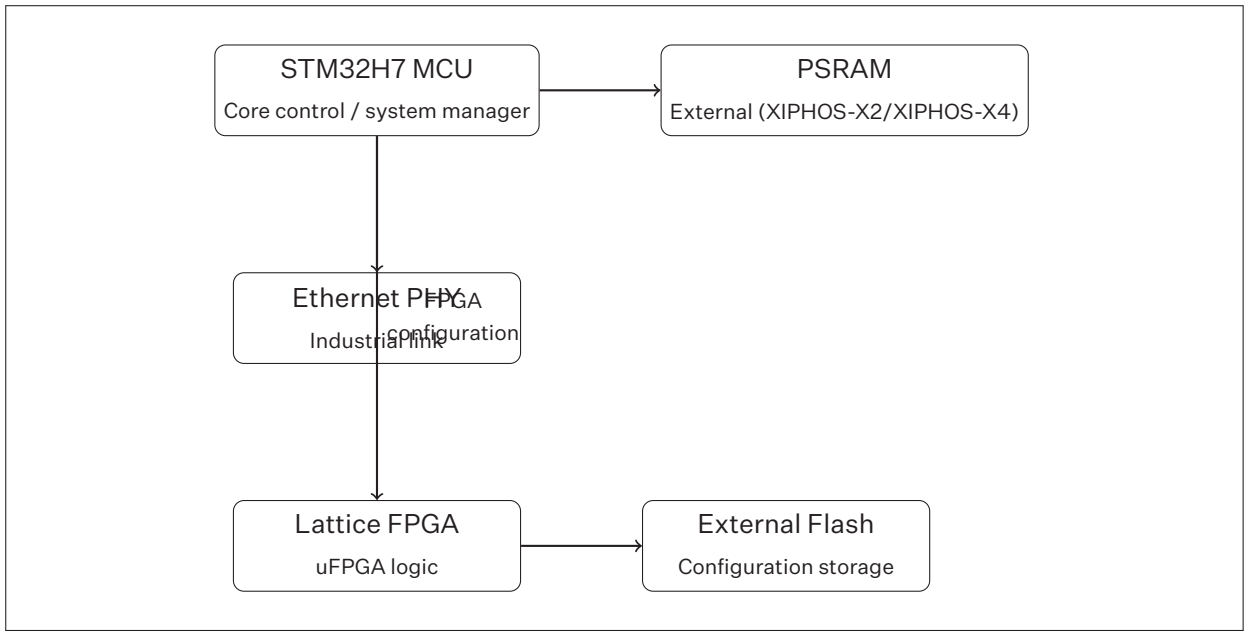

Figure 3: Reference architecture for the XIPHOS family.

The STM32H7 MCU is connected to external PSRAM for expanded working memory on XIPHOS-X2/XIPHOS-X4 variants and acts as the system manager. The MCU configures and loads the Lattice FPGA at startup. The FPGA interfaces to an external Flash device used for firmware and configuration storage. The Ethernet PHY is connected directly to the MCU for industrial network connectivity.

12 Identification and ordering

Available variants are grouped by packaging and internal capabilities. Detailed specifications are provided in the models document.

Ordering should consider the required thermal envelope, protection level, and memory expansion. XIPHOS-X2 and XIPHOS-X4 variants include additional external RAM to support larger data sets or protocol stacks.

XIPHOS-X1	No Phantom Forge®, base configuration
XIPHOS-X2	No Phantom Forge®, expanded configuration
XIPHOS-X3	With Phantom Forge®, base configuration
XIPHOS-X4	With Phantom Forge®, expanded configuration

13 Revision history

The following table records document changes.

Table 2: Revision history.

Version	Date	Changes
v0.1	2025-01-22	Initial draft of document structure.
v1.0	2025-02-02	Release 1.0 for distribution.

14 Disclaimer

This document is released as version 1.0 for distribution. For the latest revisions and product updates, refer to the REIDITE Electronics website. REIDITE Electronics reserves the right to make changes without notice.